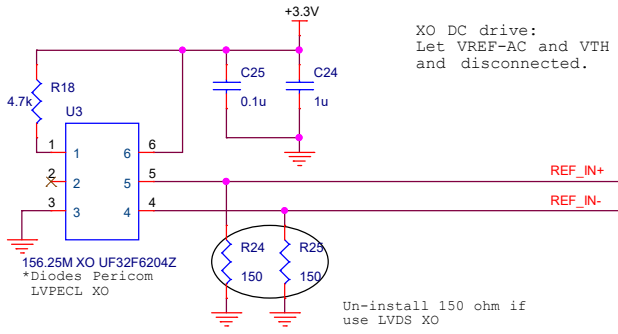
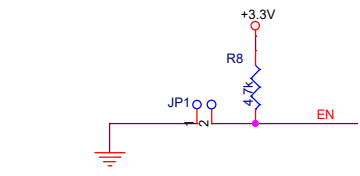


XO AC drive:
Connect VREF-AC and VTH together with 0.1uF to recover the DC bias for the IC input.



XO DC drive:
Let VREF-AC and VTH be floating and disconnected.

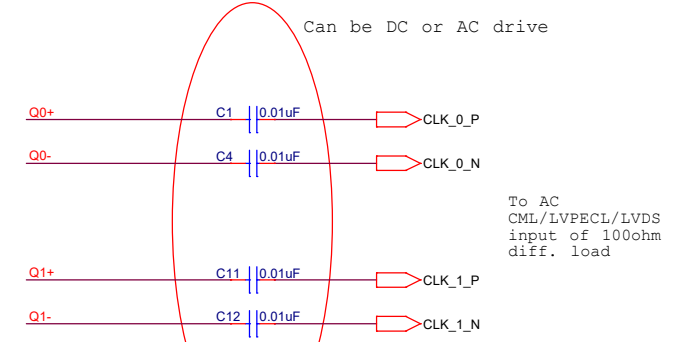


Set REF_SEL logic in R8/JP1

EN	Function
0	Disable
1	Enable

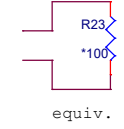
App Note:

1. IC has internal 100ohm diff. termination.
2. Each VDD pin needs 0.1u +1uF decoupling close to pin. (e.g.: VDD,...etc)
3. VDD uses small R=1~2 ohm or FB(ferrite bead)+C=10uF filtering for better DC/DC ripple noise rejection
4. When in DC input drive , leave VREF-AC and VTH pins open.
5. When in AC input drive ,VREF-AC and VTH are used.
6. Q0 to Q1 are CML output
7. CML app. uses AC coupling drive, if need DC coupling drive check datasheet of output DC level.
8. Connect EPAD in >=4 vias to GND plane



Check RX ASIC if internal termination.

RX input



Title		
PI6C5946002 Application Schematic		
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B	Diodes Inc. Clock IC Application Engineering	1.0
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