

Device setting:

Input CLK_SEL_[1,0]

0	0	XTAL
0	1	CLK_0
1	X	CLK_1

OpModeA/B[1,0]

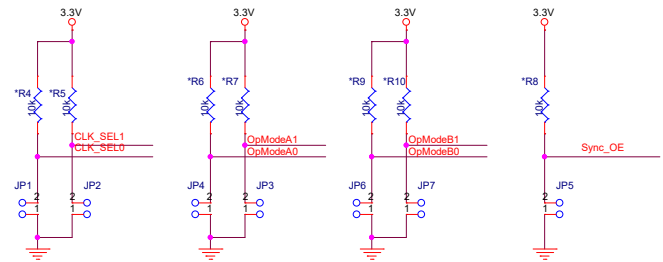
0	0	LVPECL
0	1	LVDS
1	0	HCSL
1	1	Hi-Z

Sync_OE:

Set Sync_OE logic in R8/JP5

Set "0" for Ref_out disabled

Set "1" for Ref_out enabled



Title			PI6C49S1504 Application Circuit
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App Note:

1. Select CLK0, CLK1 or XTAL as input ;
- 2.1 Each VDD pin needs 0.1u +1uF decoupling close to pin. (e.g.: VDD, VDDO, ...etc)
- 2.2 VDD/VCC 3.3V use small R=1~2 ohm or FB(ferrite bead)+C=10uF filtering for better DC/DC ripple noise rejection
3. LVPECL Output: Place 150ohm pull-down in comp. side close to pin <=300mil.
- HCSL Output: Place serial 33 ohm and 50ohm pull-down in comp. side close to pin <=300mil.
4. Suggest to use DC coupling in LVPECL/LVDS drive input clock with 100ohm cross at input pins <200mil; HCSL drive input clock without 100 ohm cross at input pins.
5. when in AC input drive either just use 100ohm cross to bias balance
6. Put 475 ohm resistor closed to IREF Pin