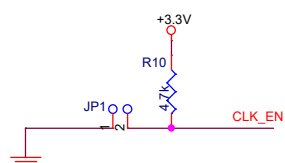
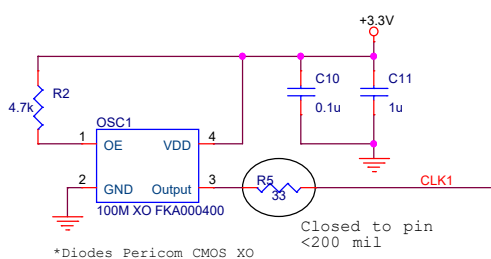
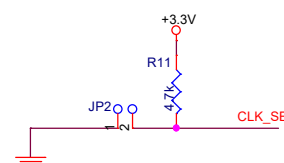


Closed to IC<300 mil



CLK_EN:
Set CLK_EN logic in R10/JP1:
0: Disable
1: Enable



CLK_SEL:
Set CLK_SEL logic in R11/JP2:
0: CLK0 is Input
1: CLK1 is Input

App Note:

1. Select CLK0 or CLK1 as input ;
- 2.1 Each VDD pin needs 0.1u +1uF decoupling close to pin. (e.g.: VDD..etc)
- 2.2 VCC uses small R=1~2 ohm or FB(ferrite bead)+C=10uF filtering for better DC/DC ripple noise rejection
3. Place serial 33 ohm and 49.9 ohm pull-down in comp. side close to pin <=300mil.
4. Put 475 ohm resistor closed to IREF Pin

Title		
P16C4931504-04 Application Schematic		
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B	Diodes Inc. Clock IC Application Engineering	1.0
Date: Monday, October 07, 2024		
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