



App Note:

1. Each VDD pin needs 0.1u +1uF decoupling close to pin. (e.g.: VDD, VDDO...etc)
2. VDD use small R=1~2 ohm or FB(ferrite bead)+C=10uF filtering for better DC/DC ripple noise rejection
3. Suggest to use DC coupling in LVDS drive input clock with 100ohm corss at input pins <200mil;
4. when in AC input drive either just use 100ohm cross to bias balance
5. Q0 to Q5 are LVDS (1.2V+/- 200mV) output, can do DC to LVDS drive, or AC to drive other diff. input

DC or AC drive, check RX ASIC if internal termination.

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