



Device setting:

Input CLK_SEL_[1,0]:

0 0
 0 1
 1 X

CLK_0
 CLK_1
 XTAL

refOUTen:

Set "0" for REFOut disabled
 Set "1" for REFOut enabled

App Note:

1. Select CLK0, CLK1 or XTAL as input ;
- 2.1 Each VDD pin needs 0.1u +1uF decoupling close to pin. (e.g.: VDD, VDDOA, VDDOB...etc)
- 2.2 VDD/VDDREF use small R=1~2 ohm or FB(ferrite bead)+C=10uF filtering for better DC/DC ripple noise rejection
3. Suggest to use DC coupling in LVDS drive input clock with 100ohm corss at input pins <200mil;
4. when in AC input drive either just use 100ohm cross to bias balance
5. Connect e_Pad in 4 to 6 vias to GND plane

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