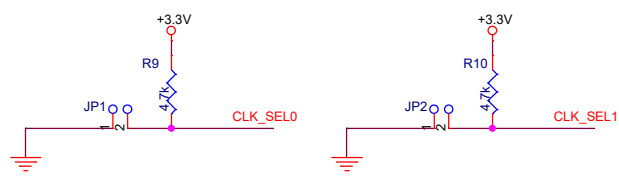
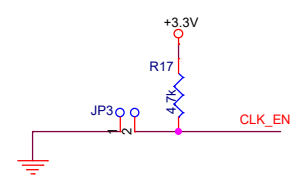


- App Note:
1. Select XTAL or CLK0 or CLK1 as input ;
 - 2.1 Each VDD pin needs 0.1u +1uF decoupling close to pin. (e.g.: VDD, ...etc)
 - 2.2 VDD uses small R=1~2 ohm or FB(ferrite bead)+C=10uF filtering for better DC/DC ripple noise rejection
 3. Place 150ohm pull-down in comp. side close to pin <=300mil.
 4. Suggest to use DC coupling in LVPECL/LVDS drive input clock with 100ohm corss at input pins <200mil;
 5. Crystal routing in comp. side, keep C1 and C2 GND close as possible.



Set CLK_SEL logic in R9/JP1/R10/JP2

CLK_SEL1	CLK_SEL0	Function
0	0	XTAL is Input
0	1	CLK0 is Input
1	X	CLK1 is Input



Set CLK_EN logic in R17/JP3

CLK_EN	Q[0:5]	nQ[0:5]
0	Disabled; LOW	Disabled; HIGH
1	Enabled	Enabled

