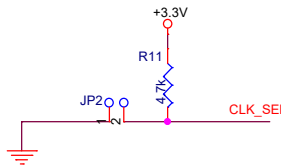


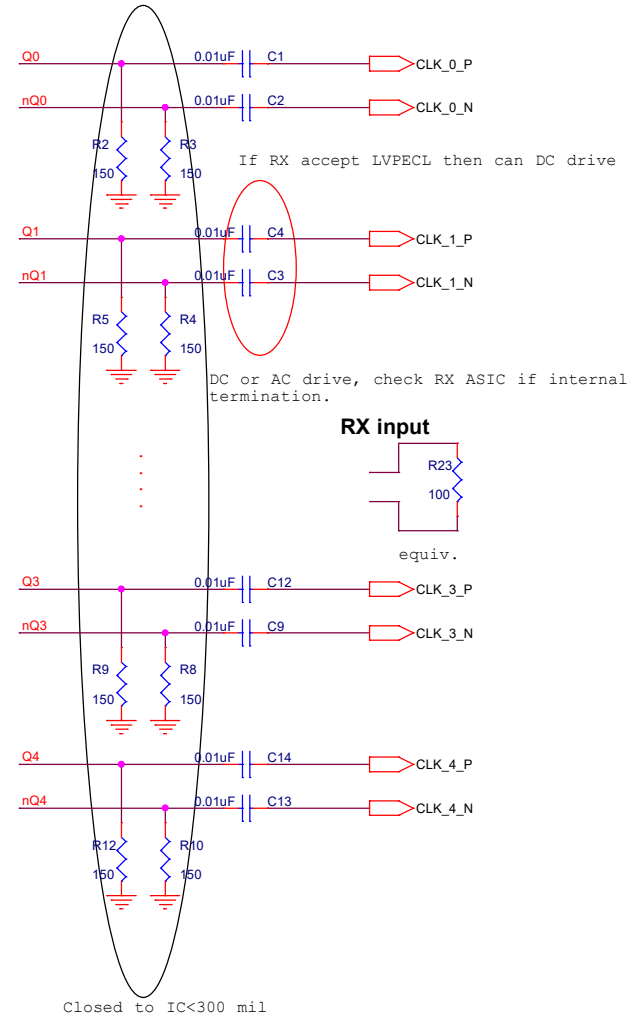
nEN:
Set nEN logic in R28/JP1:

nEN	Function
1	All output Disable
0	All output Enable



CLK_SEL:
Set CLK_SEL logic in R11/JP2:

CLK_SEL	Function
0	CLK0 is Input
1	CLK1 is Input



App Note:

1. Select CLK0 or CLK1 as input ;
2. Each VDD pin must have 0.1uF decoupling cap.; better has 1u more;
3. Place 150ohm pull-down in comp. side close to pin <=300mil.
4. Suggest to use DC coupling in LVPECL/LVDS drive input clock with 100ohm corss at input pins <200mil;
5. when in AC input drive either just use 100ohm cross to bias balance

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