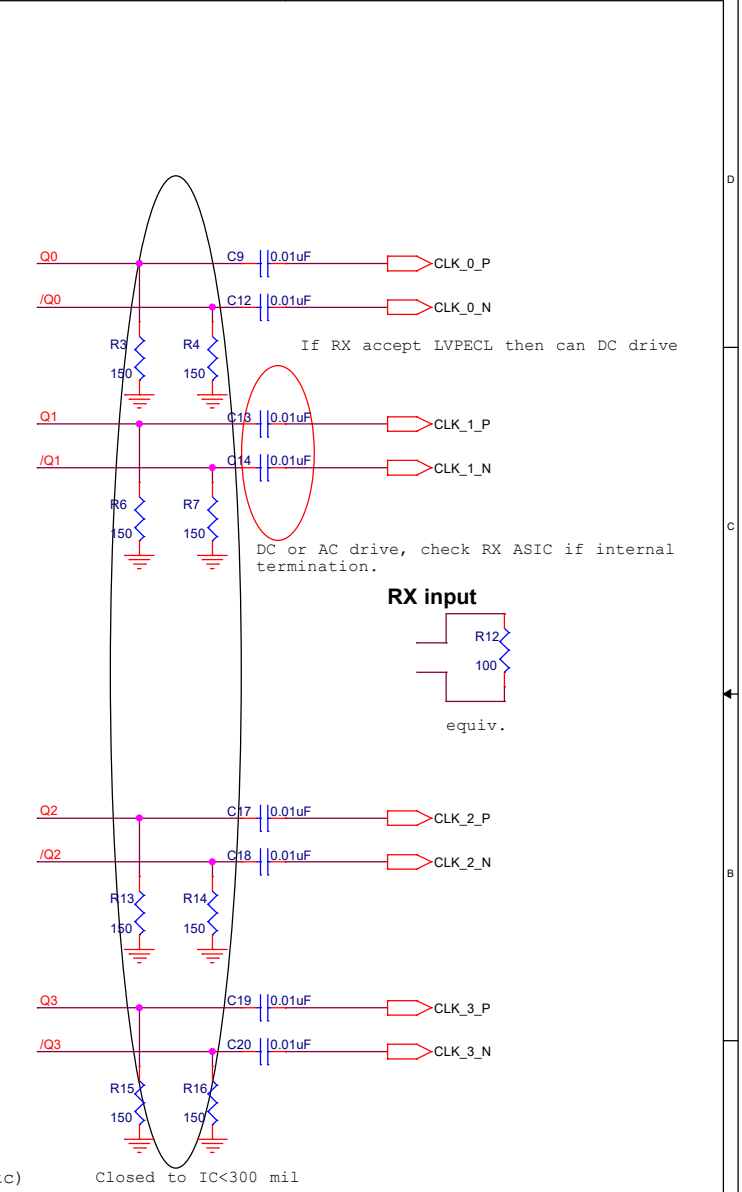


**CLK\_EN:**  
Set CLK\_EN logic in R10/JP1:  
0: Disable  
1: Enable

**CLK\_SEL:**  
Set CLK\_SEL logic in R11/JP2:  
0: CLK is Input  
1: Xtal is Input

- App Note:
1. Select CLK or Xtal as input ;
  - 2.1 Each VCC pin needs 0.1u +1uF decoupling close to pin. (e.g.: VCC..etc)
  - 2.2 VCC uses small R=1~2 ohm or FB(ferrite bead)+C=10uF filtering for better DC/DC ripple noise rejection
  3. Place 150ohm pull-down in comp. side close to pin <=300mil.
  4. Suggest to use DC coupling in LVPECL/LVDS drive input clock with 100ohm corss at input pins <200mil;
  5. Crystal routing in comp. side, keep C1 and C2 GND close as possible.



Title		
PI6C4911504-03 Application Schematic		
Size B	Document Number Diodes Inc. Clock IC Application Engineering	Rev 1.0
Date: Friday, October 11, 2024		
Sheet 1 of 1		