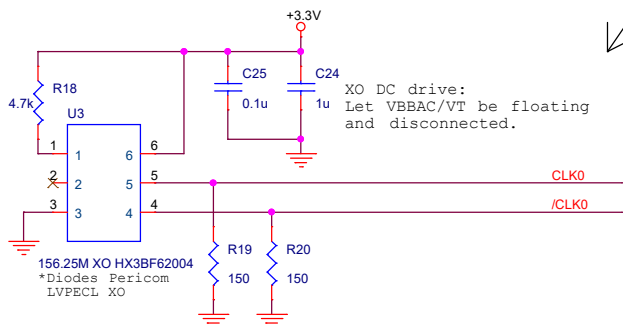
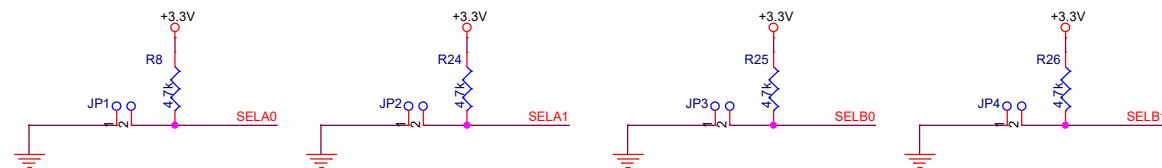


XO AC drive:  
Connect VBBAC and VT together with 0.1uF.



XO DC drive:  
Let VBBAC/VT be floating  
and disconnected.

Un-install 150 ohm if  
use LVDS XO



#### SELA[1:0]:

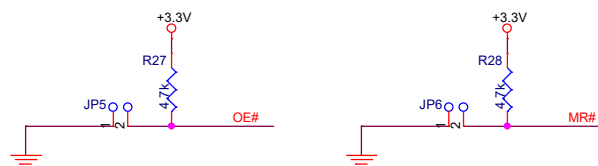
Set Output A Divide Function in R8/JP1/R24/JP2

00: Divide by 1  
01: Divide by 2  
10: Divide by 4  
11: Divide by 8

#### SELB[1:0]:

Set Output B Divide Function in R25/JP3/R26/JP4

00: Divide by 1  
01: Divide by 2  
10: Divide by 4  
11: Divide by 8



#### OE#:

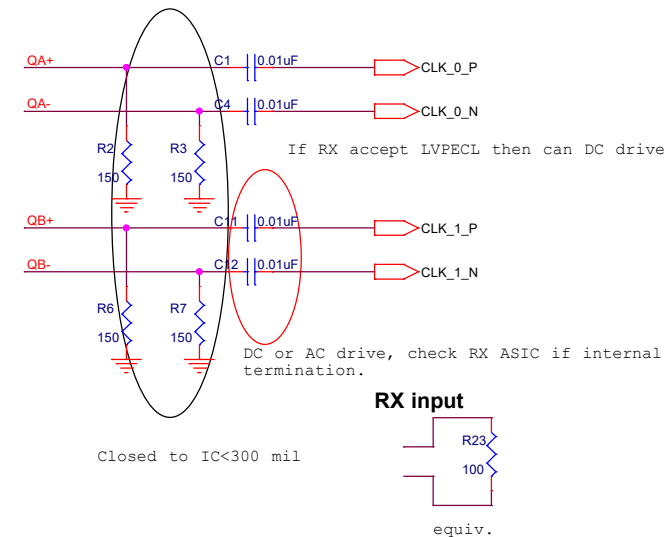
Set OE# logic in R27/JP5

0: Enable  
1: Disable

#### MR#:

Set MR# logic in R28/JP6

0: Rest  
1: Enable



If RX accept LVPECL then can DC drive

DC or AC drive, check RX ASIC if internal  
termination.

#### RX input

equiv.

#### App Note:

1. Each VDD pin needs 0.1u +1uF decoupling close to pin. (e.g.: VDD, VDDO...etc)
2. VDD uses small R=1~2 ohm or FB(ferrite bead)+C=10uF filtering for better DC/DC ripple noise rejection
3. Place 150ohm pull-down in comp. side close to pin <=300mil.
4. Suggest to use DC coupling in LVPECL/LVDS drive input clock with 100ohm corss at input pins <200mil;
5. When in AC input drive ,VBB/VT is used.

Title		
PI6C4911502D Application Schematic		
Size B	Document Number Diodes Inc. Clock IC Application Engineering	Rev 1.0
Date: Friday, October 11, 2024		
Sheet 1 of 1		