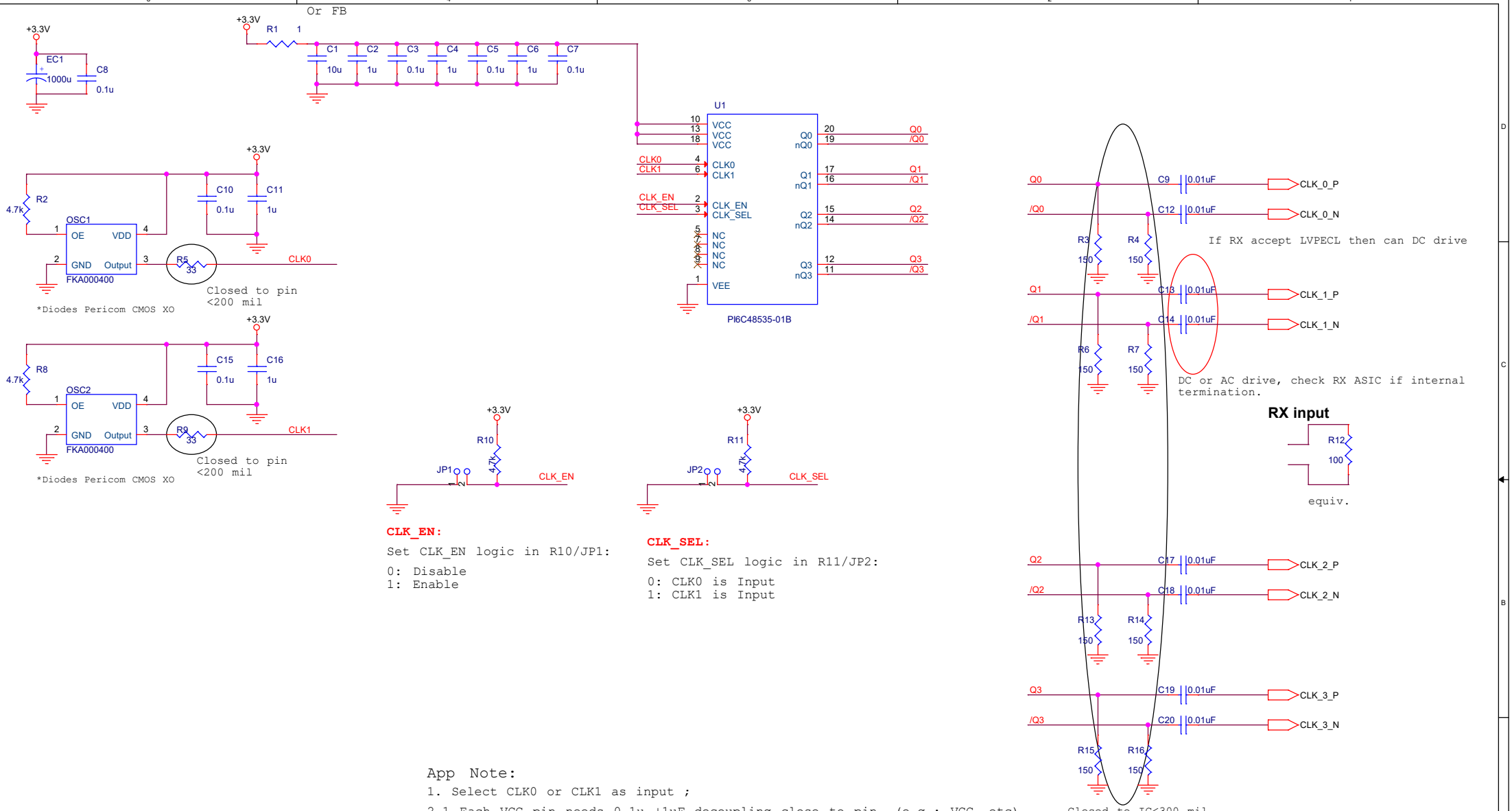

App Note:

1. Select CLK0 or CLK1 as input ;

2.1 Each VCC pin needs 0.1u +1uF decoupling close to pin. (e.g.: VCC..etc)

2.2 VCC uses small R=1~2 ohm or FB(ferrite bead)+C=10uF filtering for better DC/DC ripple noise rejection

3. Place 150ohm pull-down in comp. side close to pin <=300mil.

4. Suggest to use DC coupling in LVPECL/LVDS drive input clock with 100ohm corss at input pins <200mil;

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