PI6C5913004 Lowest Output Jitter Buffer IC
Ensuring Performance in 40GE/100GE Designs

Why Lower Jitter

High-gigabit data rate Serdes requires lower jitter reference clock due to the fact that higher data rate's bit period of UI is shorter. For example, 1GE data rate allows 0.5UI jitter, which translates to bit period of 400ps. The same 0.5UI jitter in 100GE data rate translates to only 4ps, which is 100 times shorter as shown in Figure 1. Pericom's Ultra Low Jitter 156.25M XO paired with PI6C5913004 can provide <=0.1ps lowest jitter reference clock with a good margin to guarantee today's 40GE/100GE zero Bit Error Rate (BER) designs. In contrast, Broadcom 100GE PHY specification requires 0.3ps jitter.

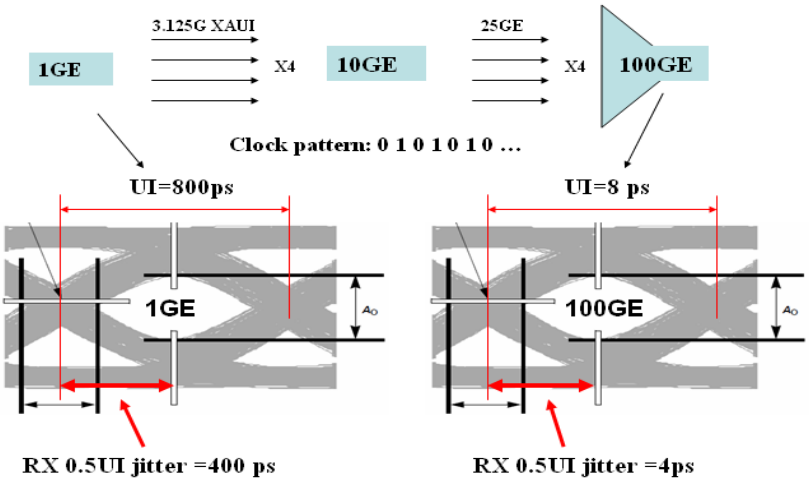

Figure. 1. 1GE to 100GE data bit period UI time

Due to the fact that 100GE optical module's costs remains high, four 25GE modules are used as a compromise. IEEE specifies Wavelength Division for 100GE standard in four wavelength 25GE modules, equivalent to one 100GE module as shown in Figure 2. PI6C5913004 is a perfect solution with the lowest additive jitter 2:4 clock buffer IC to fit this design in 16 pin TQFN as shown in Figure 3.

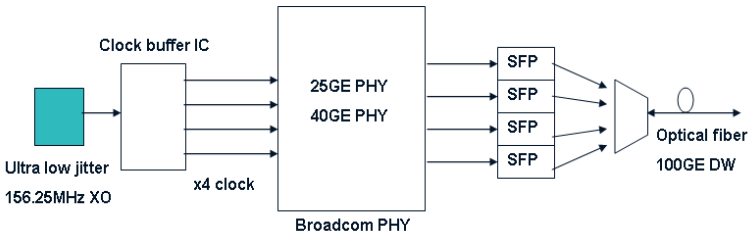

Figure. 2. 156.25MHz clock for 100GE WD solution

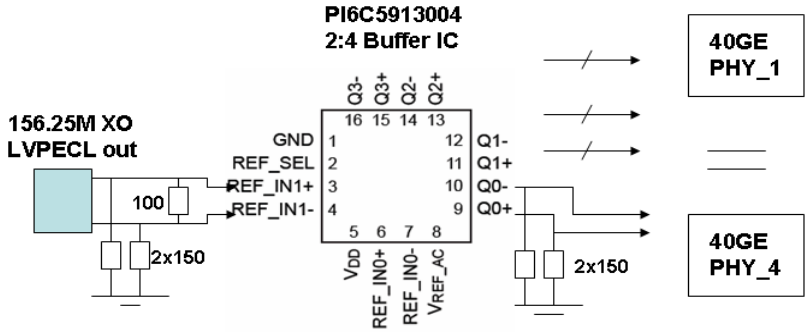

Figure. 3. PI6C5913004 buffer IC of x4 156.25MHz

PI6C5913004 is a high performance clock buffer with the lowest output jitter that can keep XO input jitter to drive 40GE/100GE PHY due to its lowest additive jitter. This buffer output jitter 0.1ps phase noise plot is shown on Figure. 4.

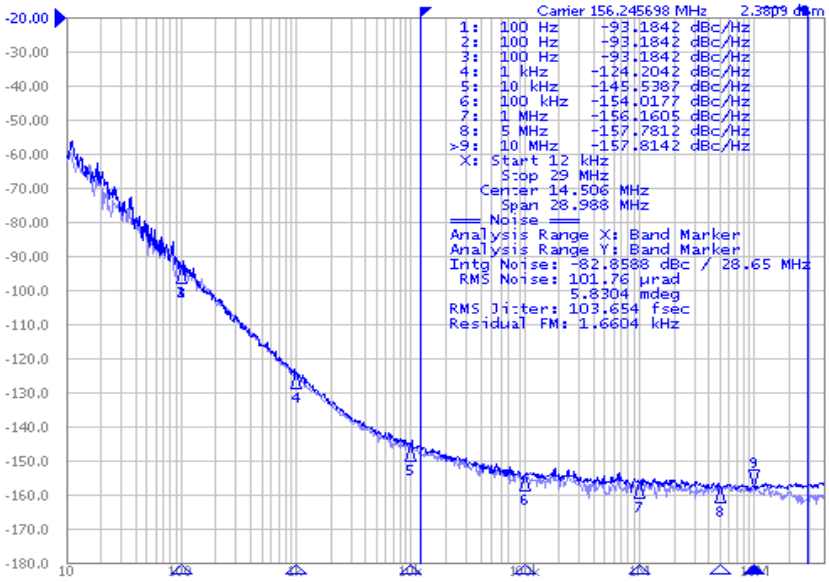

Figure. 4. PI6C5913004 output 0.103ps jitter

Low Jitter XO PCB

Selecting a XO PCB is as important as selecting a low jitter XO to guarantee the best jitter performance. Figure 5 shows the Pericom's 156.25MHz LVPECL XO driven clock buffer PCB diagram, which uses DC coupling directly driven to the buffer IC input with 150ohm pull-down and 100ohm cross termination. This design does not require any DC bias from power supply, and prevents any power supply noise injection to the clock trace. The PCB routing keep-out is necessary to prevent any board noise cross talk.

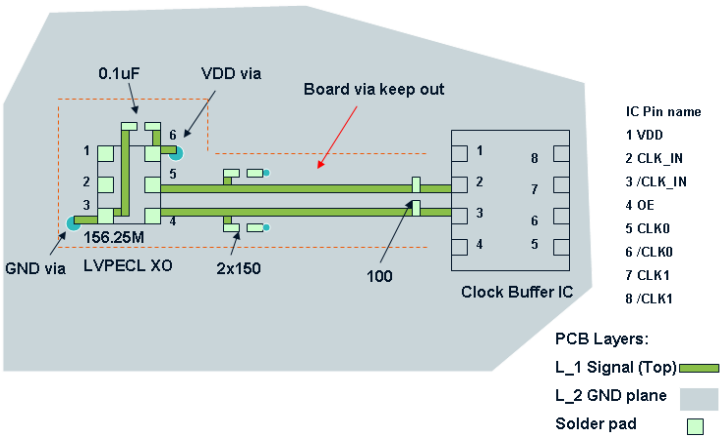

Fig. 5. 156.25MHz XO PCB diagram

More Products:

PI6C5913004 (2:4 LVPECL), PI6C5946002/4(1:2/4 CML), PI6C5922504(1:4 LVDS), PI6C5916004(1:4 LVPECL), PI6C59S6005(2:5 LVPECL/CML/LVDS), For more clock solution, please visit company web site:

Crystal Oscillator: http://www.pericom.com/products/crystals-and-crystal-oscillators/
Clock Buffer IC: http://www.pericom.com/products/clock-and-timing-ics/clock-buffers/