



PI3PCIE3413 PI3PCIE3413 DM DP Source Application with PI3HDMI511A

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Application_Note

1 Introduction

Pericom offers a wide variety of high-speed switches. For dual-mode DisplayPort 1:3 source application, PI3PCIE3413 passive switch for transmitting main link signals and PI3USB14-A for sideband signals are recommended. As the highest HDMI transmission per HDMI Specification Version 1.4 is 3Gbps, signal integrity is critical. Thus, a re-driver, PI3HDMI511A, with source termination is highly recommended on HDMI path to support such data rate. PI3PCIE3413 de-mux application circuits with DP, HDMI and DVI outputs are described in this document.

2 External Component Requirements

PI3PCIE3413 is designed to transmit high-speed PCIe signals. It can accept main link signals from a DP or dualmode DP source with up to 2.0V Vbias_TX per DP Standard Version 1.2. Two PI3USB14-A, which have low RON, are used in source application circuit below for AUX/DDC, CEC and HPD side-band signals. PI3HDMI511A is added in the HDMI path in figure 2 for supporting 3Gbps transmission.

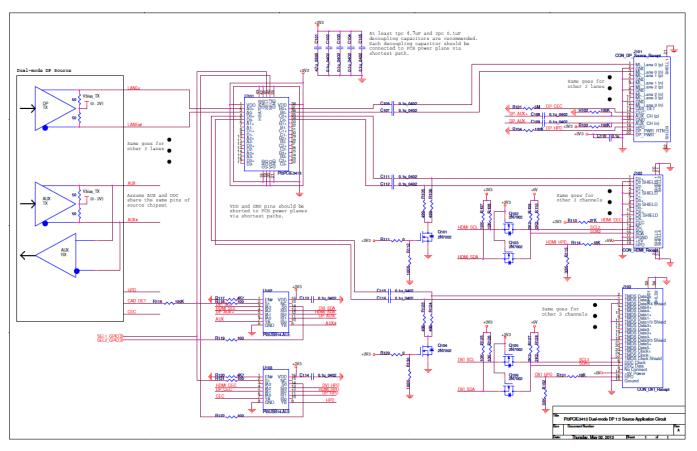


Figure 1: PI3PCIE3413 1:3 dual-mode DP Source Application Diagram



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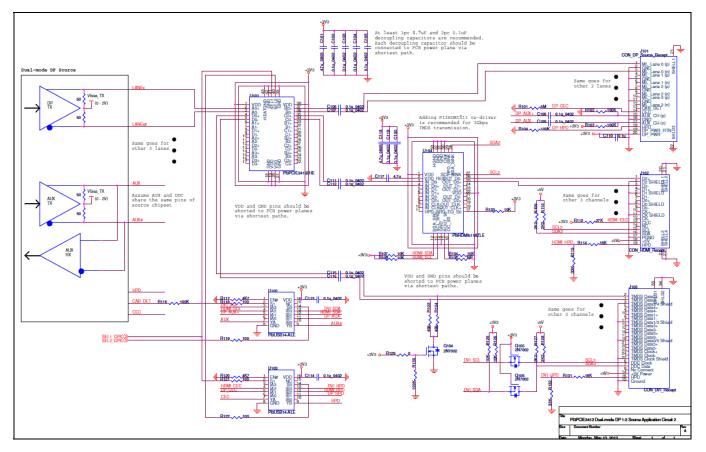


Figure 2: PI3PCIE3413 1:3 dual-mode DP Source Application Diagram with 3Gbps HDMI Transmission

2.1 Main Link Channels

In source application, AC coupling capacitors at all main link signals are inserted per DP Standard Version 1.2. AC coupling capacitor value in the range of 75 – 200nF is required. Per TMDS architecture, 499 Ω pull-down resistor should be implemented at each TMDS trace so as to create a proper DC offset for a dual-mode DP source. A FET can be used to enable all 499 Ω pull-down resistors. For supporting 3Gbps transmission, 499 Ω pull-down resistors at TMDS paths of HDMI port are replaced by PI3HDMI511A re-driver.

2.2 AUX Channels

Per DP Standard Version 1.2, AC coupling capacitor value in the range of 75 – 200nF is also required for each AUX signal. After the AC coupling capacitor, source is required to pull AUX+ to GND and AUX- to DP_PWR via resistors in the range of $10k\Omega$ to $105k\Omega$. $100k\Omega$ resistor value is recommended per DP Standard Version 1.2. When a DP sink device determines AUX+ and AUX- are being pulled to low and high, respectively, a DP source device is connected.



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2.3 DDC Channels

Per HDMI Specification Version 1.4, each of SCL and SDA is pulled up to 5V via a resistor in the range of $1.5k\Omega$ to $2k\Omega$ in HDMI source application. As DDC signals pass through PI3USB14-A which is designed for 3.3V transmission, FET is implemented to isolate 3.3V at PI3USB14-A device side from 5V at HDMI/DVI connector side. As 5V to 3.3V level shifter is implemented in PI3HDMI511A design, FET and its pull-up resistors are not required when using PI3HDMI511A in 3Gbps HDMI application.

2.4 HPD Signal

100k Ω pull-down resistor is normally implemented at HPD in order to have a known state for dual-mode DP source device when no sink device is attached to it. HPD signal from HDMI sink is 5V. A resistor ladder using 18k Ω and 33k Ω resistors is to level shift 5V HPD to 3.3V before entering PI3USB14-A.

2.5 Control Pins

SEL1 and SEL2 of PI3PCIE3413 are used for port selection. They can be connected to GPIOs to do the selections. These two pins can be used to control the S1 and S0 selection pins of the two PI3USB14-A devices in parallel.

Per DisplayPort Dual-Mode Standard Version 1, Cable Detect pin should be pulled to 3.3V via a $100k\Omega$ pull-up resistor if an HDMI device or a DVI sink device is attached to the dual-mode DP source chipset. If a DP sink device is attached, Cable Detect pin should be pulled down to ground.

Per DP Standard Version 1.2, pulling CEC pin of a DP source to ground via a $5M\Omega$ resistor is recommended. Per HDMI Specification Version 1.4, CEC pin for an HDMI source should be pulled to 3.3V via a $27k\Omega$ resistor.

3 Layout Design Guideline

Layout guideline especially for high-speed transmission is critical. Please refer to Plxxxx High Speed Layout Guideline, AN345, for detailed recommendations.

4 References

- (1) VESA DisplayPort Standard Version 1 Revision 2, Video Electronics Standards Association, January 5, 2010
- (2) VESA DisplayPort Dual-Mode Standard Version 1, Video Electronics Standards Association, February 10, 2012
- (3) VESA DisplayPort Interoperability Guideline Version 1.1a, Video Electronics Standards Association, February 5, 2009
- (4) High-Definition Multimedia Interface Specification Version 1.4, HDMI Licensing, LLC, June 5, 2009
- (5) PCI Express Board Design Guidelines Draft, Intel Corporation, June 2003