

Interface LVDS Signals Using Pericom Switches PI3V512 / PI3HDMI412FT-B

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1. Introduction

- PI3V512 and PI3HDMI412FT-B are high performance products currently used in many LVDS-LCD applications in production.
- In the LVDS-LCD application using PI3V512 and PI3HDMI412FT-B, the Vdd should be set to 1.5V to 2.0V, the ground should be set to 0V and the “SEL” signal should be set to 0V for low and Vdd +/- 10% for high.
- The charge pump in PI3V512 and PI3HDMI412FT-B increases the switch Vgs (voltage of gate) for passing the 1.0V to 1.5V LVDS signals with good performance and without clamping.
- PI3V512 and PI3HDMI412FT-B perform well in insertion loss. Figure 5 shows the insertion loss of PI3HDMI412FT-B, and PI3V512 has similar performance.
- Figure 7 compares the Rx eyes, measured at the end of a 2-meter cable at 1.6gbs speed, with and without PI3V512/PI3HDMI412FT-B (hardwired to bypass the pads).

2. Applications

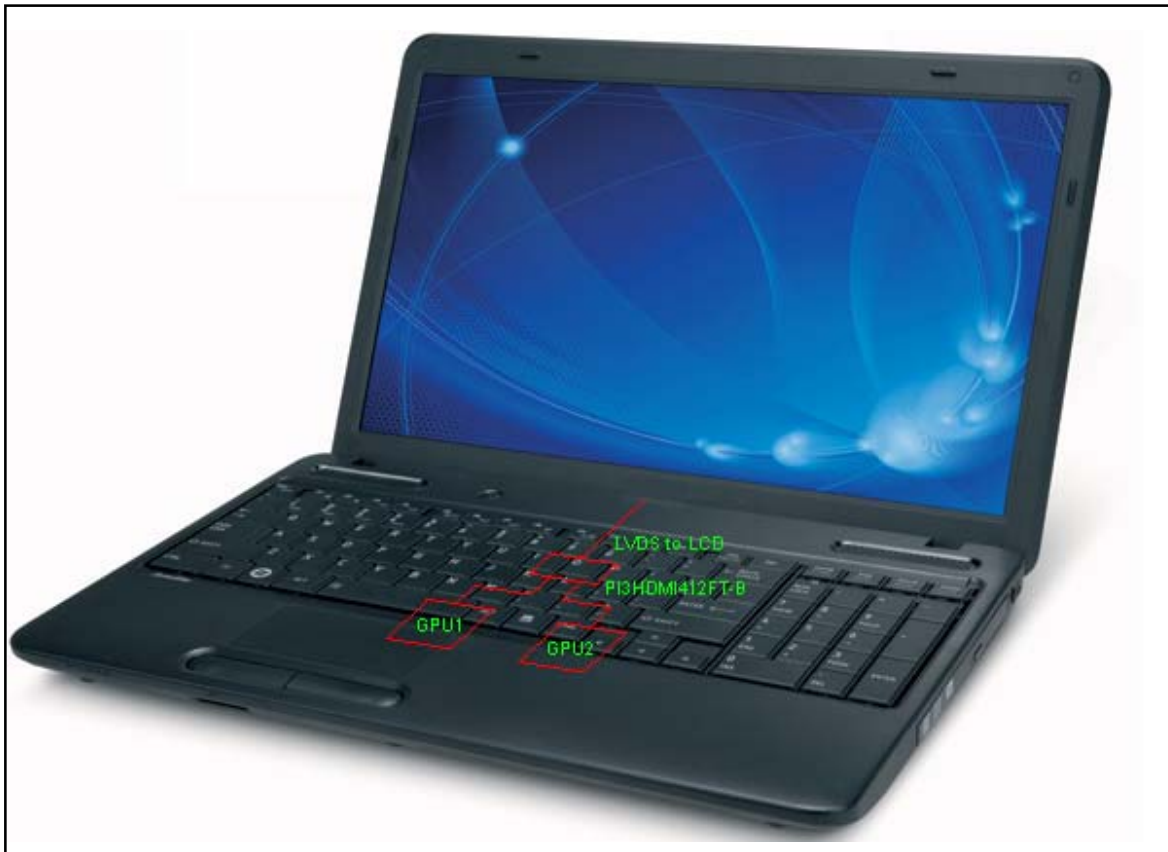


Figure 1: Typical LVDS-LCD Application in Notebook Using PI3V512 and PI3HDMI412FT-B

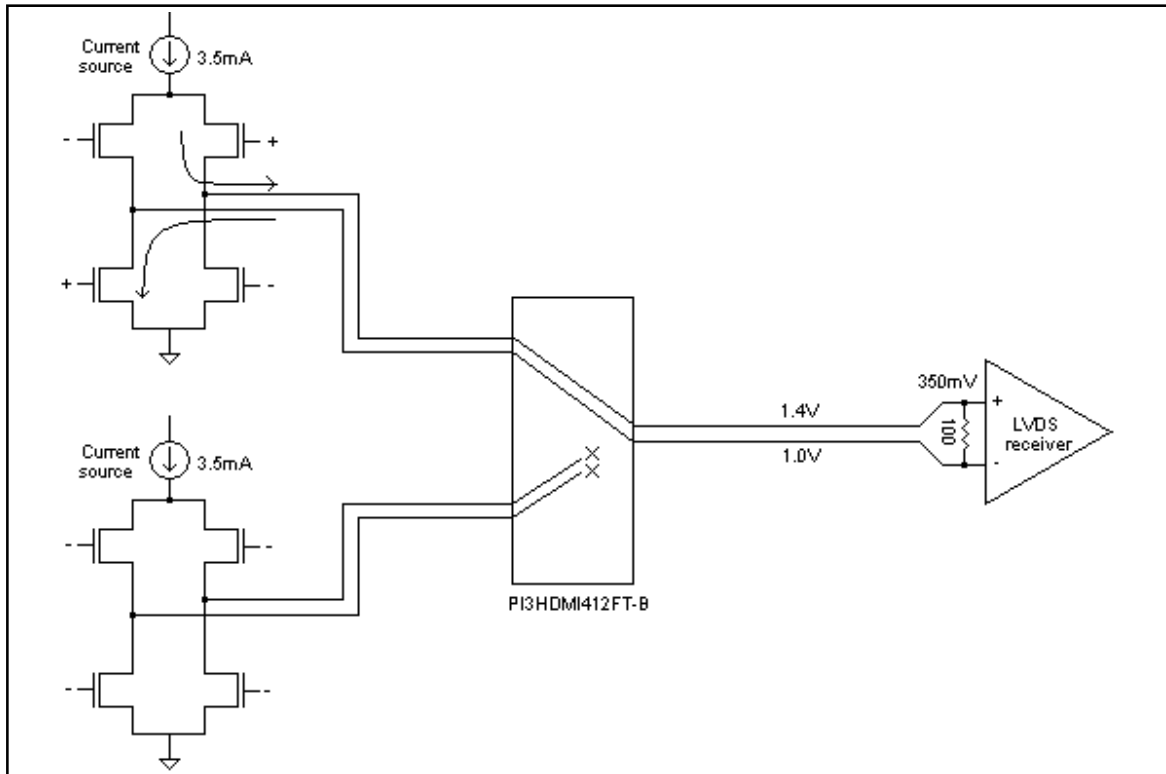


Figure 2: LVDS Signals Application Diagram

The LVDS output consists of a current source (nominal 3.5 mA) that drives the differential pair lines. The basic receiver has high DC input impedance. Therefore, the majority of driver current flows across the 100Ω termination resistor and generates about 350 mV across the receiver inputs. When the driver switches, it changes the direction of current flow across the resistor, and creates a valid “one” or “zero” logic state.

3. PI3V512 and PI3HDMI412FT-B in LVDS Applications

- PI3V512 and PI3HDMI412FT-B have an internal charge pump that charges up the V_{gs} (gate voltage of the switch channels) above V_{dd} level (1.5V-2.0V).
- Without the charge pump, the LVDS signal (1.0V-1.5V) of PI3V512 and PI3HDMI412FT-B, at 1.5V to 2.0V V_{dd}, would be clamped at output of PI3HDMI412FT-B.
- With the charge pump in PI3V512 and PI3HDMI412FT-B, the LVDS signals (1.0V-1.5V) from PI3V512 and PI3HDMI412FT-B are able to have good signal integrity and not be clamped when the V_{dd} is 1.5V to 2.0V.

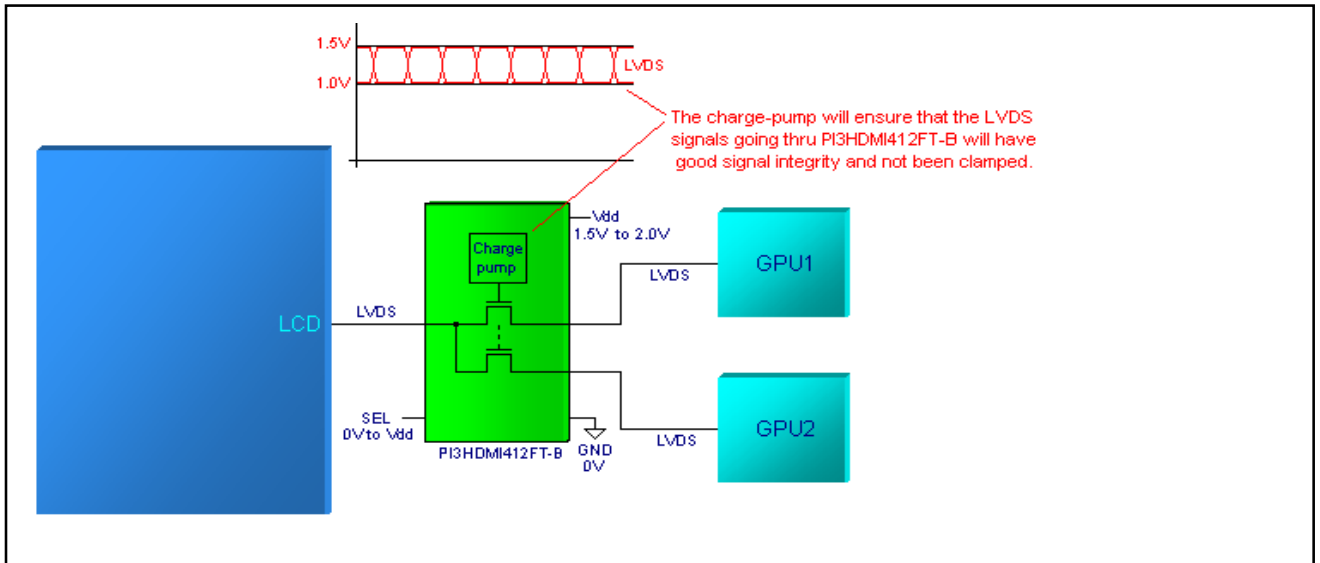


Figure 3: Charge Pump (Vdd: 1.5V to 2.0V, ground: 0V, "SEL": 0V to Vdd)

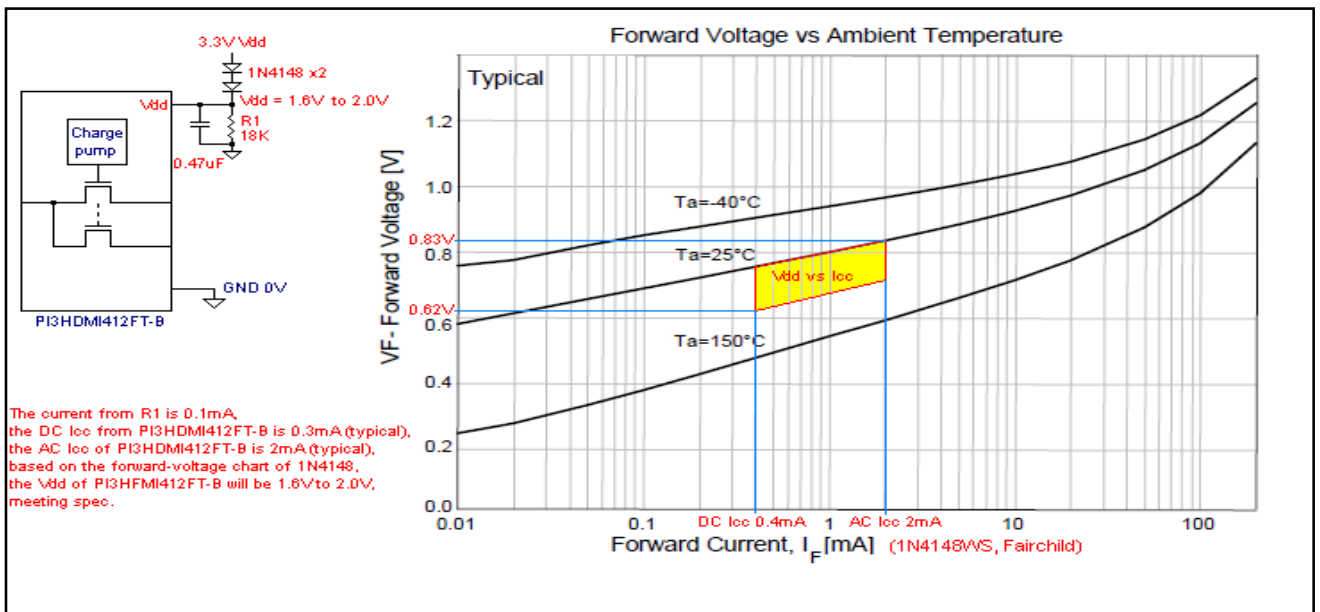


Figure 4: Two 1N4148 diodes are used for 1.6V-2.0V Vdd when using 3.3V power

- The DC Icc is the quiescent Icc of PI3V512 and PI3HDMI412FT-B when there are no input LVDS signals.
- The AC Icc is the operation Icc mainly from the parasitic capacitance between the switch channels and the Vdd rail when working with LVDS signals.

4. The bandwidth/insertion loss of PI3HDMI412FT-B

The excellent bandwidth/insertion loss (see Figure 5) of PI3HDMI412FT-B ensures the performance of the LVDS application using PI3HDMI412FT-B. The bandwidth/insertion loss in figure 5 was measured using 0V ground and 1.8V Vdd.

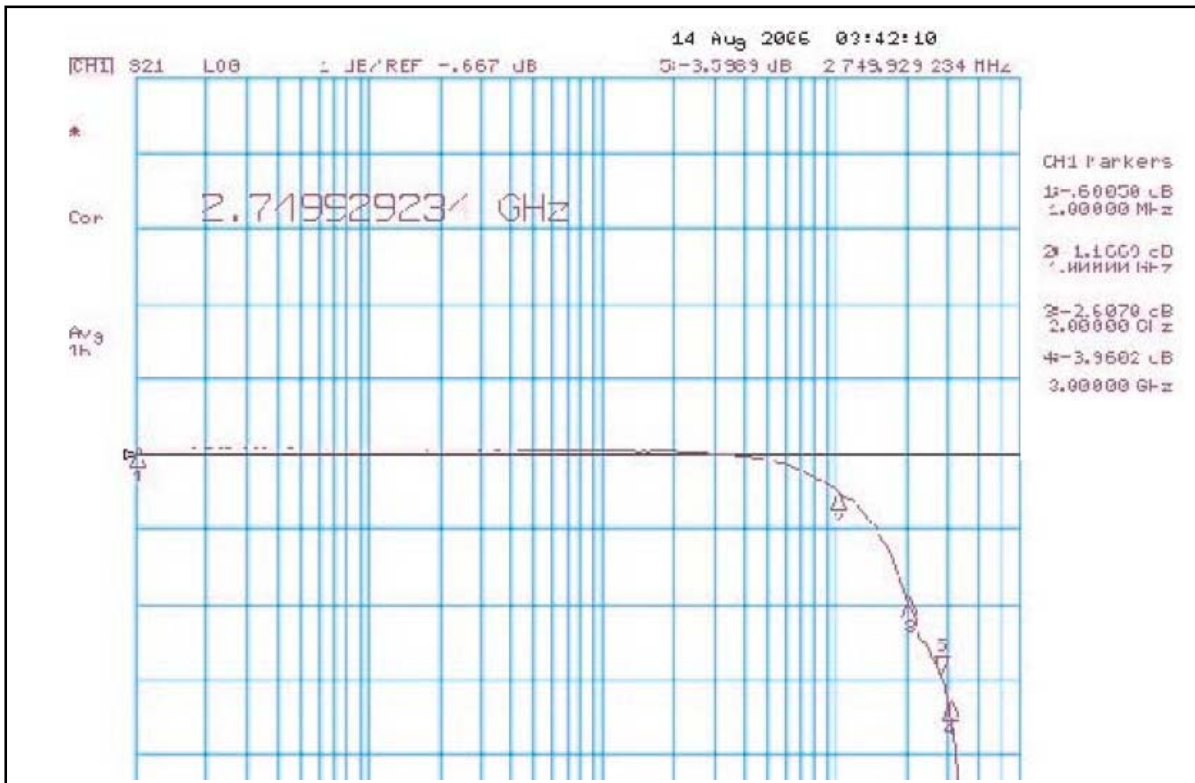


Figure 5: Bandwidth/Insertion Loss of PI3HDMI412FT-B

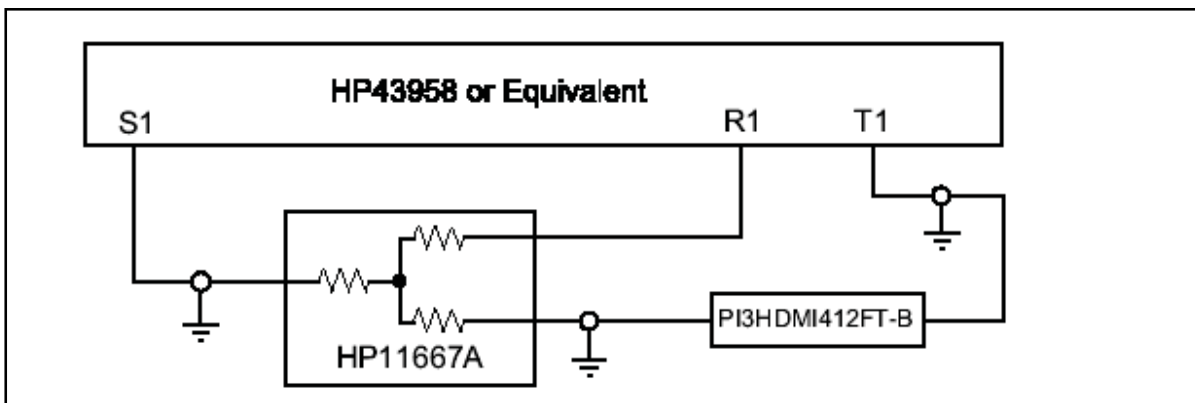


Figure 6: Test Circuit for Bandwidth/Insertion Loss of PI3HDMI412FT-B

5. Rx Eye Comparison

The Rx eye comparison with and without PI3HDMI412FT-B (see left and right side respectively in Figure 7) demonstrates that the insertion loss caused by PI3HDMI412FT-B is minimal.

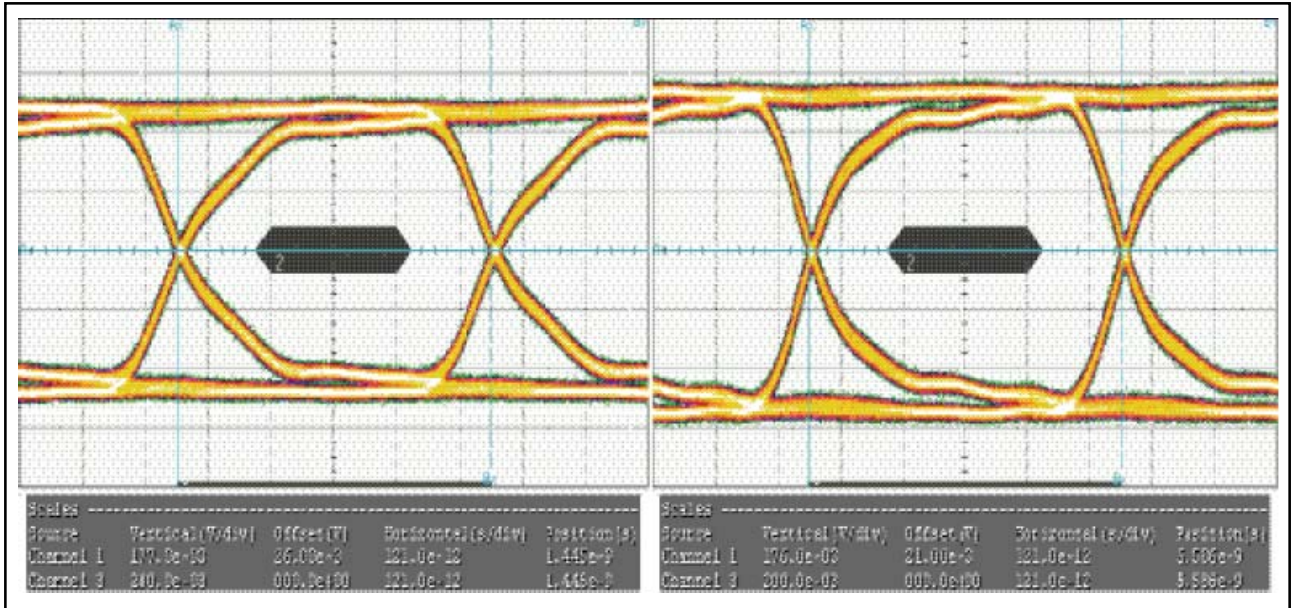


Figure 7: the Rx Eyes with PI3HDMI412FT-B (left) and Without PI3HDMI412FT-B (right – Hardwired to Bypass). Measured at the End of a 2-Meter Cable, at 1.6gbs

6. Recommended Layout for LVDS 100ohm Differential Impedance

Plane	Material	Thickness (mil)
Solder mask	Mask paint	1.2
Signal	Copper	1.9
Prepreg	2116	4.4
Vcc	Copper	1.4
Core		47
Vss	Copper	1.4
Prepreg	2116	4.4
Signal	Copper	1.9
Solder mask	Mask paint	1.2
Total		62.4

Table 1: Stack-up

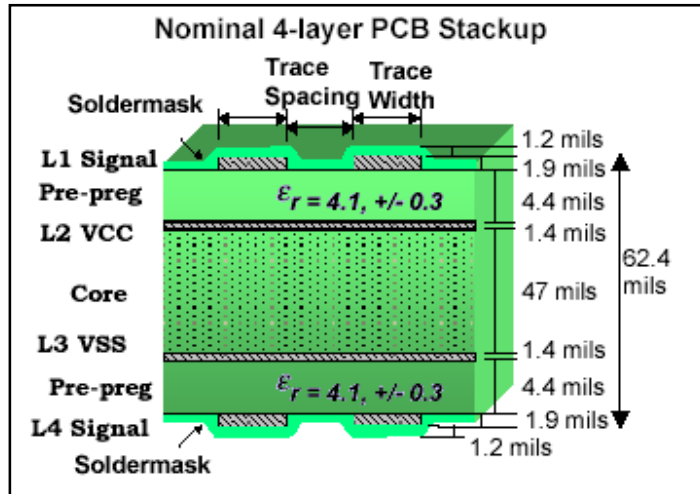


Figure 8: Stack-up

- Use 5-7-5 mils for trace-space-trace for the micro-strip lines (the traces on top and bottom layers) for 100ohm differential impedance.
- Use 5-5-5 mils for trace-space-trace for the strip-lines (the traces inside layers) for 100ohm differential impedance.
- Use standard 4 to 8 layers stack-up with 0.062 inch thick PCB.
- For micro-strip lines, using ½ OZ Cu plated is ok.
- For strip-lines in 6 plus layers, using 1 OZ Cu is recommended.
- The trace length miss-matching shall be less than 5 mils for the “+” and “-“ traces in the same pair
- More pair-to-pair spacing reduces crosstalk
- Target differential Zo of 100ohm ±15%

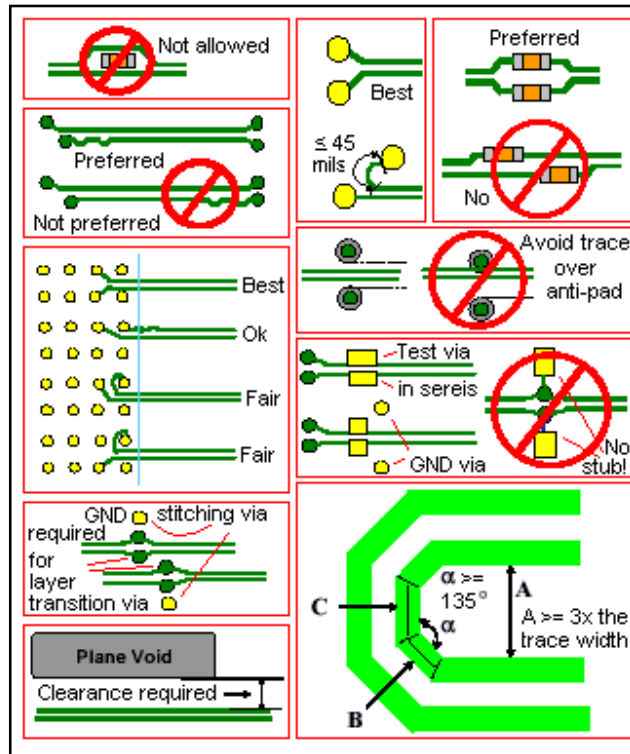


Figure 9: Layout Guidance for the Trace Routings

Recommended PCB Layout:

Use 0.1uf in size of 0402 for all the Vdd (any power pins) pins of the IC device, as close to the Vdd pins as possible, within 2-3mm if feasible.

Use dedicated Vdd and GND planes for to minimize the jitters coupled between channel trough power sources.