

Pericom PCI Express® 1.0 & PCI Express® 2.0 Advanced Clock Solutions

PCI Express Bus In Today's Market

PCI Express, or PCIe®, is a relatively new serial point-to-point bus in PCs. It was introduced as an AGP replacement for graphics and has quickly transitioned to mainstream use as an I/O interconnection. While it was built to initially target desktop and mobile personal computers, servers, and other communication network equipment, PCIe has now been adopted into the embedded ASIC market with the higher speed 5 Gbps of PCIe 2.0.

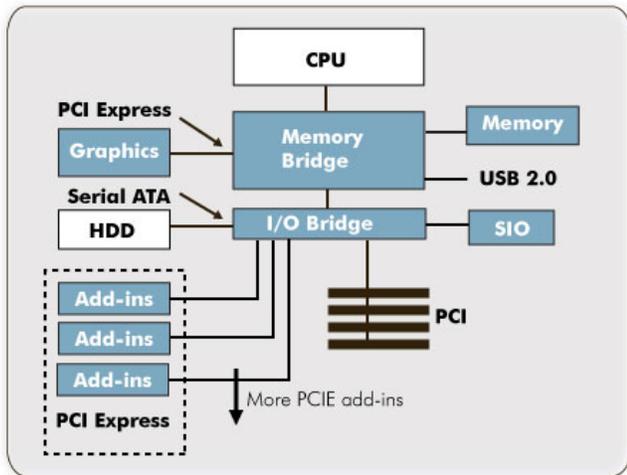


Fig. 1 PCIe® add-ins in today's computer system design

In fact, when PCIe bus meets serial bus market trends, the flexibility will provide a scalable architecture where bandwidths will increase based on the link widths. PCIe supports x1, x2, x4, x8, x16, and x32 link widths as the following table shows.

Table 1. PCIe® link scale and bandwidth

Raw Bit Rate (Gbps) by Lane Width					
Signaling Rate	X1	X4	X8	X16	X32
PCIe1.0 - 2.5 Gbps per lane	2.5	10	20	40	80
PCIe2.0 - 5 Gbps per lane	5	20	40	80	160

PCI-SIG® (Peripheral Component Interconnect Special Interest Group) is responsible for the PCIe specification (www.pcisig.com).

The main changes from PCIe 1.0 to PCIe 2.0 are:

- Speed increase from 2.5 Gbps to 5.0 Gbps
- Speed negotiation from 2.5 Gbps to 5.0 Gbps and 5.0 Gbps to 2.5 Gbps
- Electrical idle entry and exit for power savings, design ease, and robustness
- Link with down-configure for power savings and up-configure when additional bandwidth is required

PCIe 2.0 must be 1.0 compatible and have a higher jitter requirement on its reference clock 100 MHz due to its higher speed with smaller UI margin.

The Importance of a PCIe Reference Clock

To accommodate interoperation, PCIe, like any other serial bus protocol product, must pass the compliance test as final products according to the PCI-SIG specification. The following two diagrams show how the physical link compliance test setup looks like.

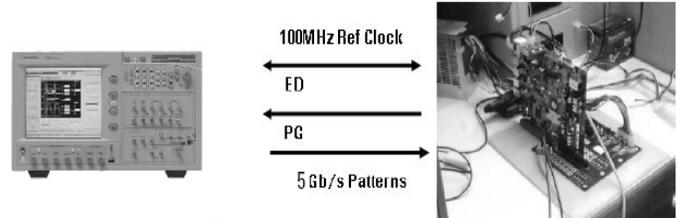


Fig. 2 PCIe® physical link compliance test board setup

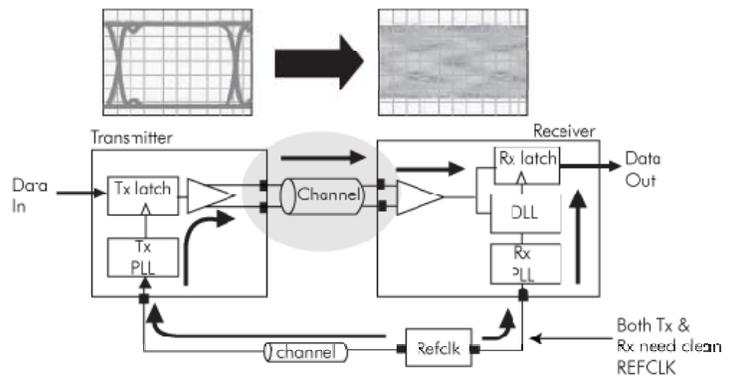


Fig. 3 PCIe® physical link compliance test diagram

PCIe buses need to maintain a BER performance similar to the other network serial I/O links. For a given BER level, the eye-closure and total jitter for CDRC (clock data recovery circuit) is related by:

$$Eye-closure(BER) = UI - TJ(BER)$$

$$TJ = RJ + DJ (=DCD + ISI + PJ)$$

The total system RJ (random jitter) is critical since it will not be equalized in general pre-emphasis circuits. The total RJ is combined with TX and RX PLL RJ, and their reference clock random jitter directly contributes to them. CPI-SIG specified PCIe RX eye jitter budget is 0.4UI min. for both 1.0 and 2.0 as shown in the following diagram and table. How much Refclk jitter is allowed in the PCIe eye closure brings us to the next question.

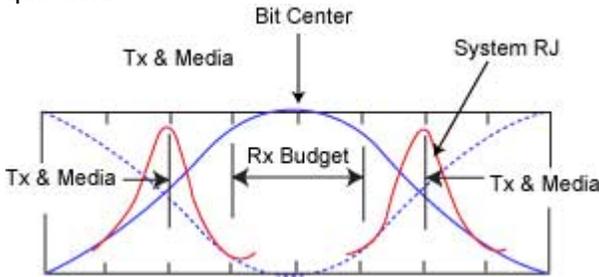


Fig. 4 PCIe[®] RX eye budget diagram

Table 2 PCIe[®] TX/RX PLL BW and RX eye budget:

PCIe	Data rate (Gb/s)	Common Clk divide ratios	System LBW (MHz)	RX Eye Budget
1.0	2.5	25	1.5	0.4UI
2.0	5.0	50	5 to 16 8 to 16	0.4UI

What is the budget jitter of reference clock for PCIe serial link?

PCI-SIG and Intel referenced clock jitter to PCIe link jitter transfer function model in both theory and bench verification. They stated that this Refclk jitter transfer function is a reverse U shape BPF with peaking around 1.5MHz as the following red line curve in Fig. 5 which is mostly related to the system eye closure.

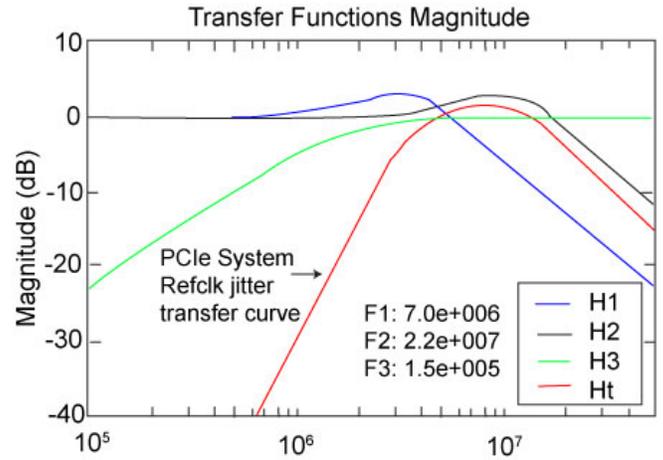


Fig. 5 PCIe[®] system Refclk jitter transfer curve

Fig. 6 shows how a normal clock jitter spectrum changes after the PCIe reference clock jitter band passes the system transfer function.

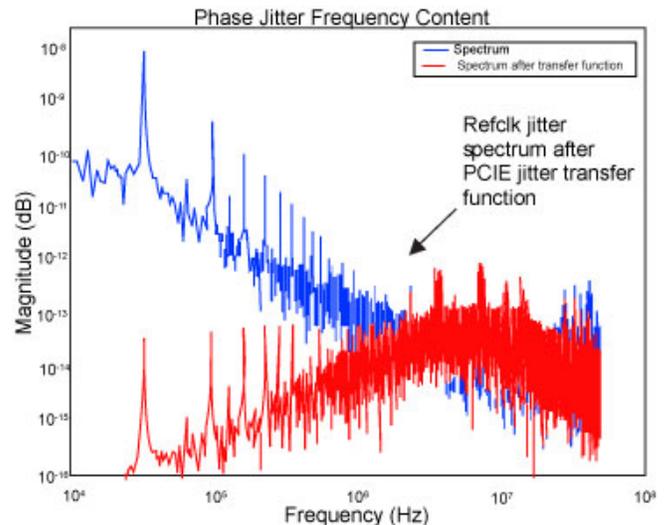


Fig. 6 Refclk jitter spectrum after through PCIe jitter transfer curve

Here the PCIe reference clock jitter spectrum in the range of 400 kHz to 10MHz is mostly amplified and contributes directly to PCIe link eye-closure.

PCI-SIG has a PCIe 1.0 and 2.0 reference clock jitter budget for the PCIe common clock system architecture. See Table 3.

Table 3 Reference Clock Jitter Budget:

PCIe	Refclk Freq.	Refclk Drive signal	Refclk Budget (RJ)	PCIe jitter test template
1.0	100MHz	HCSL	86 ps	PCIe_1_1
2.0	100Mhz	HCSL	27.9 ps 3.1 RMS	PCIe_2_0's

Table 3 shows how PCIe 2.0 has dramatically raised the jitter requirement budget from 1.0.

Qualifying PCIe Reference Clock Jitter

The 2.0 reference clock measurement test setup is the same as 1.0 according to PCI-SIG specification, shown in the following diagram:

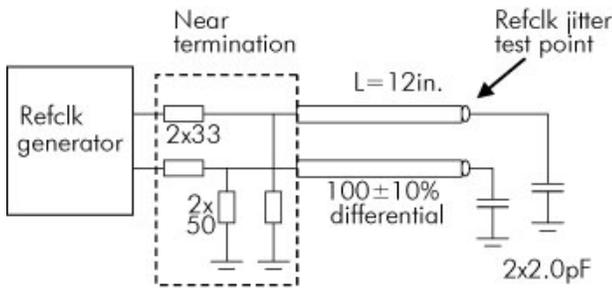


Fig. 7 PCIe Refclk PCI-SIG[®] recommended test setup.

PCIe reference clock jitter test must cooperate with Intel's clock jitter tool software with the procedure:

In Fig. 7 test setup, use approved Tek scope (for example Tek. DTS7404) to take 1 million clock cycles and record the cycle trend data as it shows here:

```
9.9888888888885945E-9
9.975000000040507E-9
9.986111111095174E-9
9.98055555551363E-9
1.0008333333421347E-8
9.981250000015533E-9
```

Load the above scope cycle trend data to Intel PCIe jitter compliance jitter tool software and run Refclk jitter test in the selected jitter template profile.

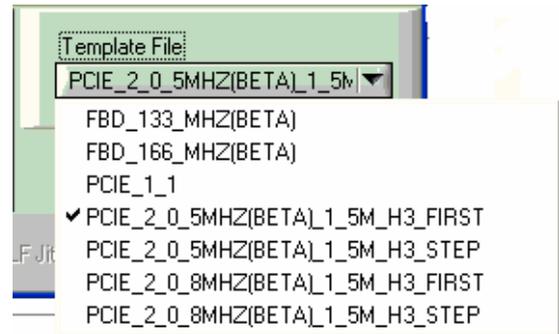


Fig. 8 Intel jitter tool test template selection

Here is the Refclk jitter template example of PCIe[®] 2.0 8MHz, 1.5MHz and 1st order:

PCIe_2_0_8MHZ_1_5M_H3_FIRST:

- Clock Interval: 10 Nanoseconds
- Jitter Budget: 27.9 Picoseconds
- Expected Sample Size: 1 Million unit intervals
- Expected Measurement Point: System Board PCIe Connector
- Worst Case System PLL 1 (H1)
 - 16 Mhz Low Pass.
 - 40 DB/dec Rolloff
 - Damp = .54.
 - Delay = 0.
- Worst Case System PLL 2 (H2)
 - 8 Mhz Low Pass.
 - 40 DB/dec Rolloff
 - Damp = .54.
 - Delay = 12 Nanoseconds
- Minimum CDR (H3)
 - 1.5 Mhz High Pass.
 - 20 DB/dec rolloff.
- SSC Separation YES
- **Peak to Peak Jitter (ps):** The difference in the maximum and minimum values in the accumulated phase jitter array.
- **RMS Jitter (ps):** The root mean square value of all the values in the accumulated phase jitter array.
- **Maximum Allowed Jitter (ps):** The maximum allowed jitter (per spec) for the specified template.

Note, the PCIe_2_0_8MHZ(BETA)_1_5M_H3_STEP template has the widest jitter pass band, which generates the largest PCIe_II jitter value for the same clock cycle trend data.

Fig. 9 shows a test example of Pericom's high-end PCIe 2.0 6-pin 100MHz XO, Part#: SHA000001. Other product details can be found at the company web: www.pericom.com/pdf/datasheets/se/290.pdf

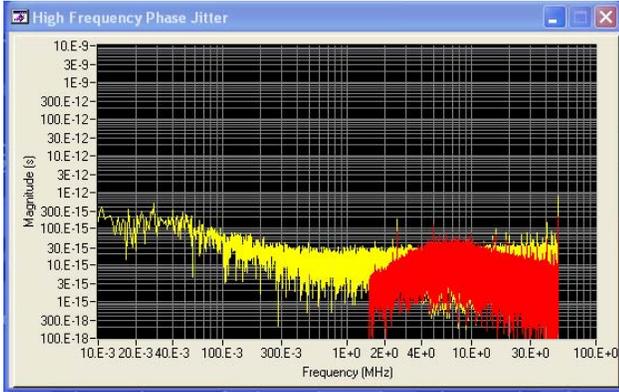


Fig. 9 Pericom SHA000001 PCIe_2_0_8MHZ_1_5M_H3_STEP high frequency jitter test plot window

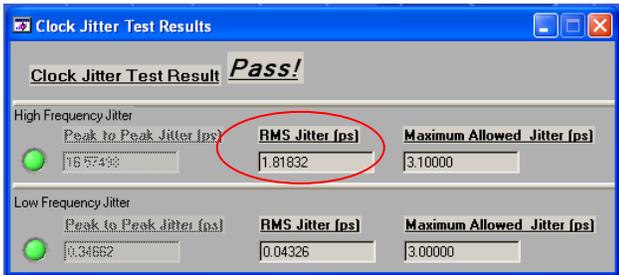


Fig. 10 Pericom SHA000001 PCIe_2_0_8MHZ_1_5M_H3_STEP high frequency jitter test result summary window.

Fig. 10 window shows this product has industrial leading PCIe 2.0 Refclk tested jitter performance with RMS jitter 1.82ps, which largely over pass the max. RMS 3.1ps specification.

Pericom PCIe® Clock Tree Solutions

Pericom has long history in high speed switch and clock IC business. It has most Intel specified PCIe® clock products to meet the market PCIe clock tree design requests:

PI6C410BS 1.0, 2.0 applications

This is an Intel sever PC clock generator with a SRC clock supporting PCIe 1.0, PCIe 2.0 internal and peripheral I/O designs.

PI6C557-03 1.0 application

This is a 25 MHz crystal generating two PCIe clocks with SSC feature.

PI6C20400 & PI6C20800 PCIe 1.0/2.0

These two products are Intel specified 4 and 8 pairs PCIe HCSL differential clock buffers

PI6C21900 PCIe 1.0/2.0

This is PCIe clock buffer providing up to 19 pairs of HCSL clocks.

To meet the particular PCIe® application of Refclk design, customers may contact Pericom's technical, sales or application support for assistance with selecting the correct solutions for your needs.

Design in High Performance PCIe® Clocks

To meet the particular PCIe application of clock tree design, there are 2 steps to consider:

Step 1, Clock Tree Planning:

To consider PCIe architecture and count how many independent internal and external PCIe I/Os, including later rev. expansion. Then decide the PCIe clock source to choose the clock buffer tree, in price and performance trade-offs.

Step 2, PCB layout:

Since RJ is the most critical random noise jitter for PCIe system, so PCB layout is extremely important to immunize the noise going into the Refclk chips through Vdd or GND bounce. Here are two basic chip power decoupling rules:

Rule 1: Each Vdd pin must have 0.1uF decoupling capacitor close to the pin;

Rule 2: For analog Vdd_A and Vss_A pins, put 0.1uF (and 1uF) decoupling capacitors on the component side between those two pins in addition Vdd_A serial with FB or 2~4 ohm resistor. Normally, it is not recommended to put over than 10uF decoupling capacitor directly on the Vdd_A pin to prevent GND bounce noise directly coupling to Vdd_A.

A PCIe Clock Tree Design Example

Fig. 11 is a 12-slot PCIe motherboard clock tree design example showing Pericom's 100MHz high-performance PCIe XO (SHA000001) as a high-quality clock source. PI6C20400 is in non-PLL mode to directly buffer and drive two PI6C20800 clocks, and the PI6C1900 clock is used to make the system clock distribution. This clock tree keeps all system PCIe clocks in synchronization. For other applications, it may use this set up in part, but generally the clock tree concept remains the same.

For PCIe Reclk SSC applications, the PCIe standard states that the link data can be modulated from +0% to -0.5% of the nominal data rate frequency. The modulation rate shall not exceed the range in 30 kHz to 33 kHz in a triangle-type shape. From a system standpoint, the +/-300ppm frequency requirement has to be maintained, so that the two communicating SSC ports do not exceed a total 600ppm difference.

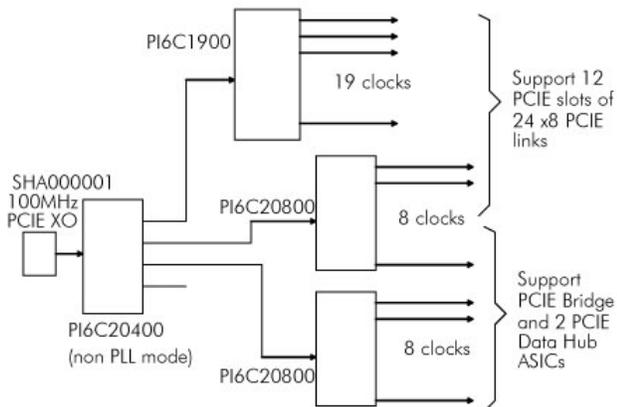


Fig. 11 12 PCIe® slot mother board Refclk tree design example

In PCIe® SSC clock design realization, there are three notes need to be addressed:

1. If the PCIe system has SSC feature, the same SSC clock source must be used in the system
2. Control the SSC spread % as needed in order to pass EMIC compliance test, never exceed the data link ppm allowance (+/-300ppm).
3. SSC-on may influence the PCIe TX eye compliance test so do the SSC-off test first. Optionally, do a SSC-on system performance verification test as some PCIe clock products have RJ increase when in SS-on mode.

Pericom Contact Information

Please contact Pericom regional sales representative or distributor at www.pericom.com

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Related Reference Papers

- 1) "PCIe Base Specification 1.1" PCI-SIG, 2005
- 2) PCI Express 2.0 Base Specification Rev. 0.7, 2007
- 3) "PCI Express Jitter Modeling", PCI-SIG, 2004
- 4) Intel Clock Jitter Tool 1.3 Release Notes, 2006
- 5) PCI Express Testing with J_Bert N4903A, Agilent, 2006