

PI3HDMI231-A/B
PI3HDMI231-A/B Demo Board Rev.B User Manual
by Ada Yip

Introduction

Pericom's PI3HDMI231-A and B are 3:1 active HDMI switches with electrical idle detect. Other than offering different DDC performances when all three input ports are de-selected, PI3HDMI231-A and B have the same functions. This user manual describes the components and the usage of PI3HDMI231-A/B Demo Board Rev.B.

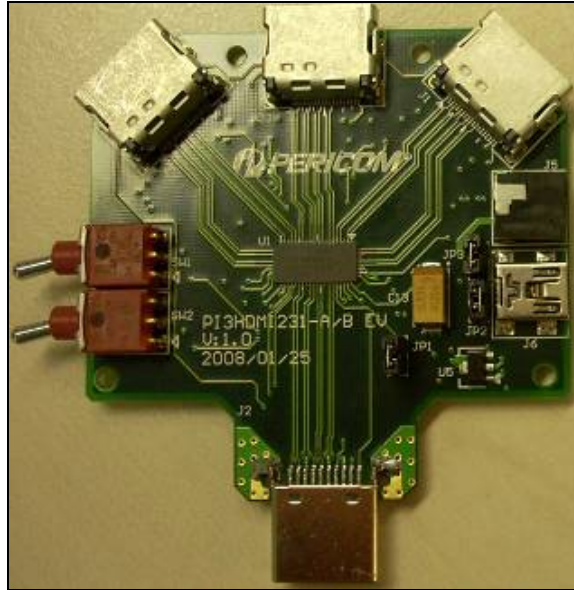


Figure 1a: Top View of PI3HDMI231-A Demo Board

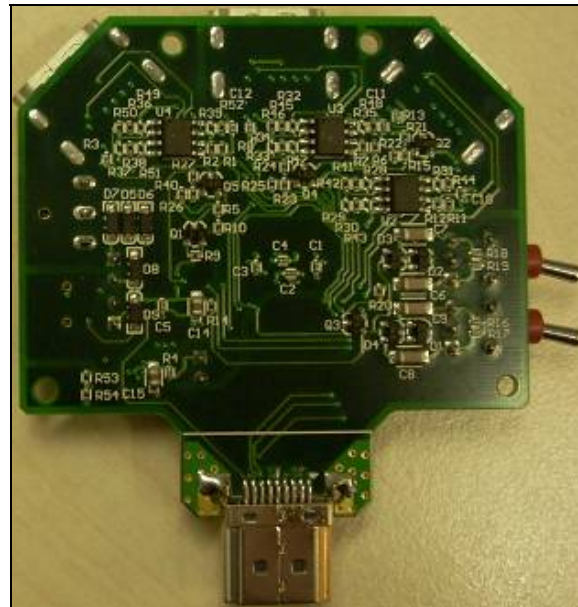


Figure 1b: Bottom View of PI3HDMI231-A Demo Board

Key Components / Circuits

- a. 3.3V for PI3HDMI231-A/B and 5V for passive components on demo board can be supplied via three ways, i.e., using 5V supplied from Input Port, Power Jack, or from USB Type B Connector.

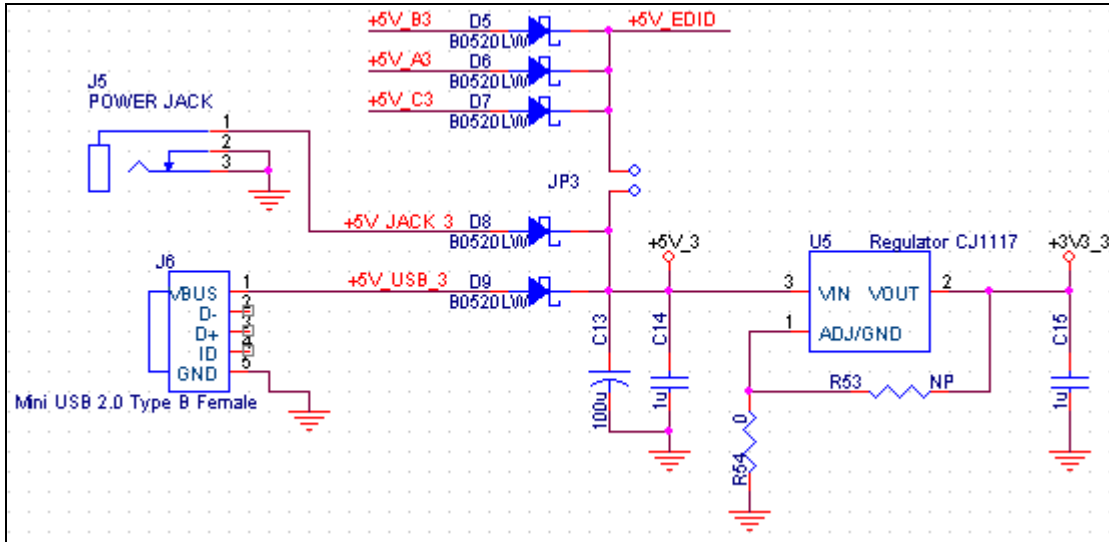


Figure 2: Schematic of 5V Power Supply of PI3HDMI231-A Demo Board Rev.B

Header JP3 on demo board is not connected at default. If using voltage of input port to power up the entire board, jumper must be added.



Figure 3: JP3 shown on PCB

5V supplying to VDD5 pin (pin 51) of PI3HDMI231-A/B, namely +5V_EDID, comes from any source connecting to input connector J1, J3 or J4 if header JP3 is not connected.

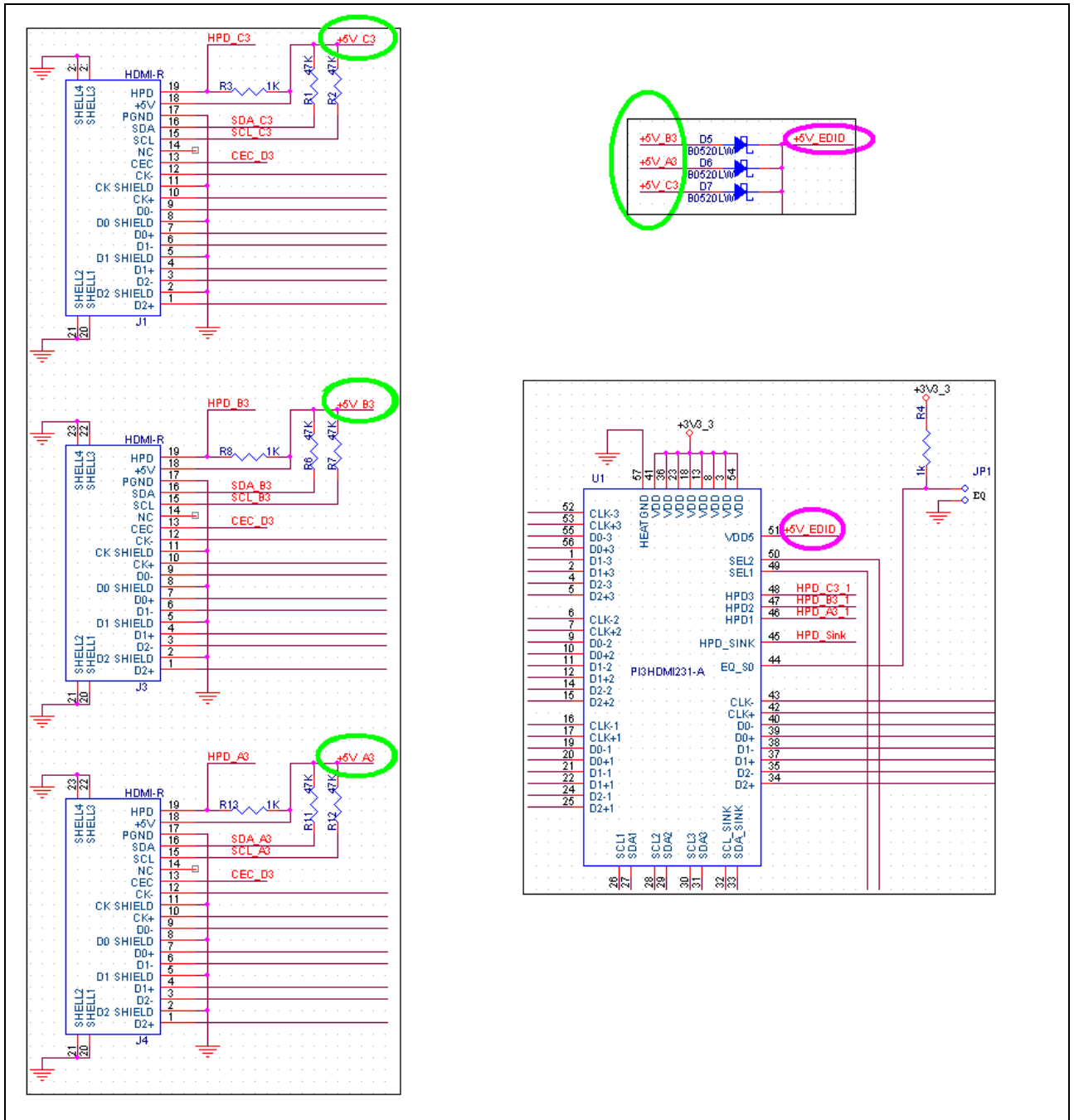


Figure 4: Schematic of 5V Power Supply to Sideband Signals of PI3HDMI231-A/B

If JP3 is shorted, voltage applied on Power Jack J5 or Mini USB connector J6 can be used to provide voltage to VDD5 pin of PI3HDMI231-A/B.

5V supplying to output HDMI connector, namely +5V_D3, is provided by +5V_3 power via shorting header JP2 as shown below.

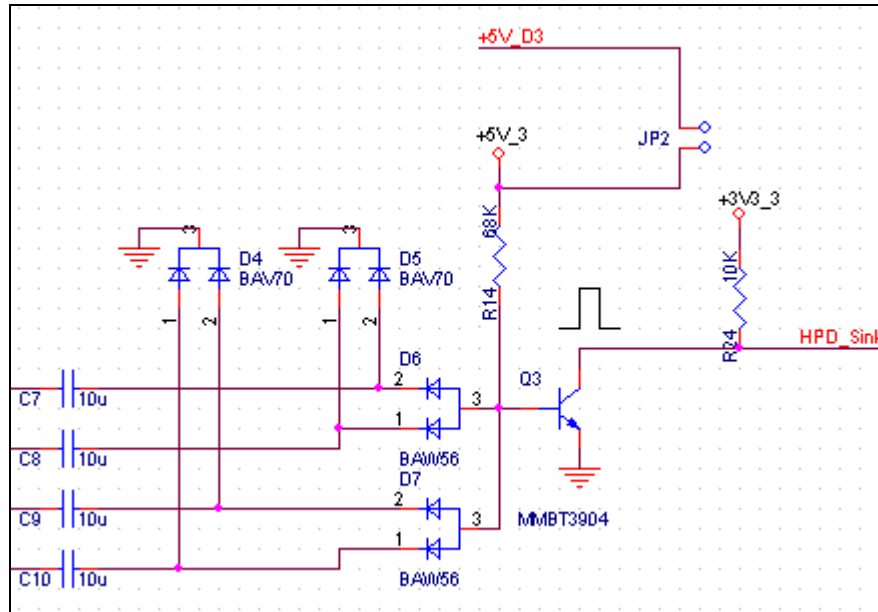


Figure 5: Schematic of 5V Power Supply to Output HDMI Connector



Figure 6: JP2 shown on PCB

- b. An HPD pulse of 350ms is generated at output of an NPN transistor Q3, called HPD_Sink, when switching port via switch SW1 or SW2 in the following circuit.

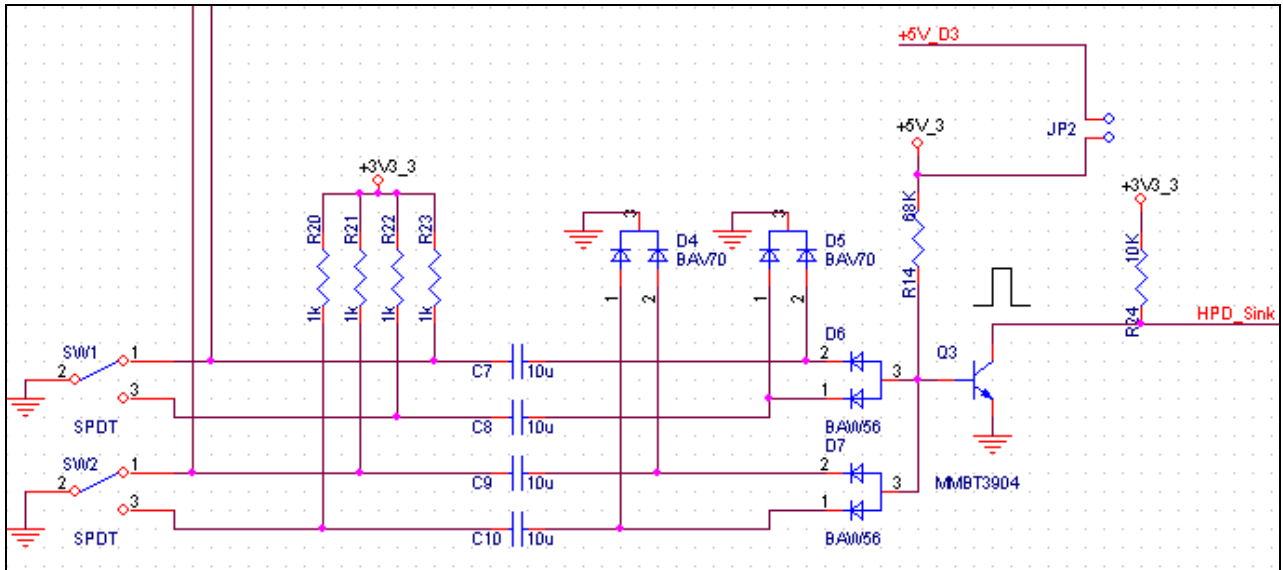


Figure 7: HPD Reset Pulse Circuit

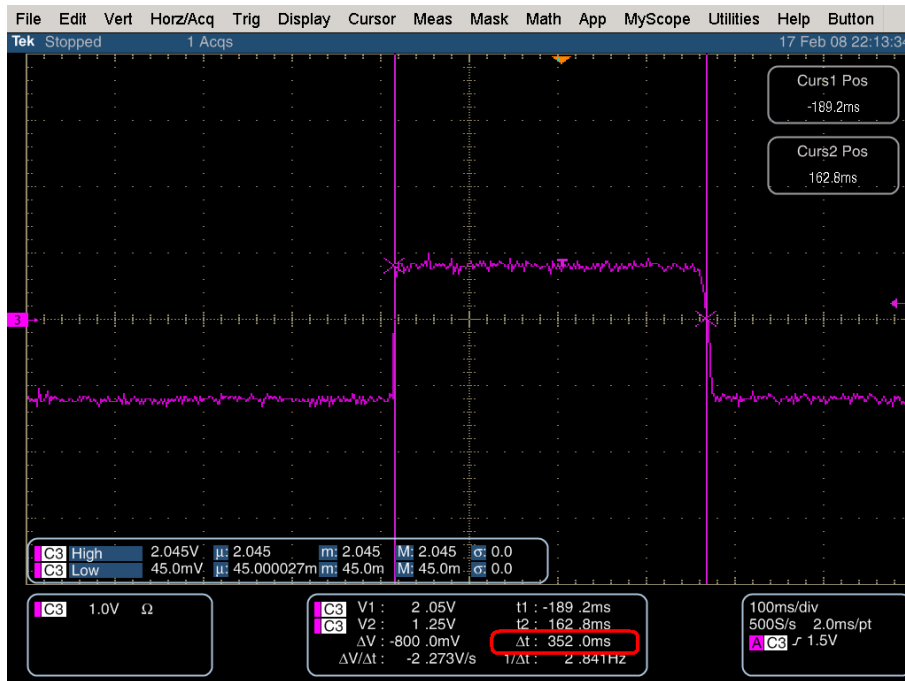


Figure 8: 350ms HPD Pulse

This pulse will be transferred from HPD_SINK pin of PI3HDMI231-A/B to one of its HPD pins, i.e., HPD1, 2 or 3, according to the port selection. It will then initiate a reset of HPD at the corresponding input connector, HPD_A3, HPD_B3 or HPD_C3, through NPN transistors, Q2, Q4 or Q5, respectively. Please refer to Figure 9. Resetting HPD is to ensure that HDCP Transmitter Link State is reset back to reset state H0. For details, please refer to Application Note AN202.

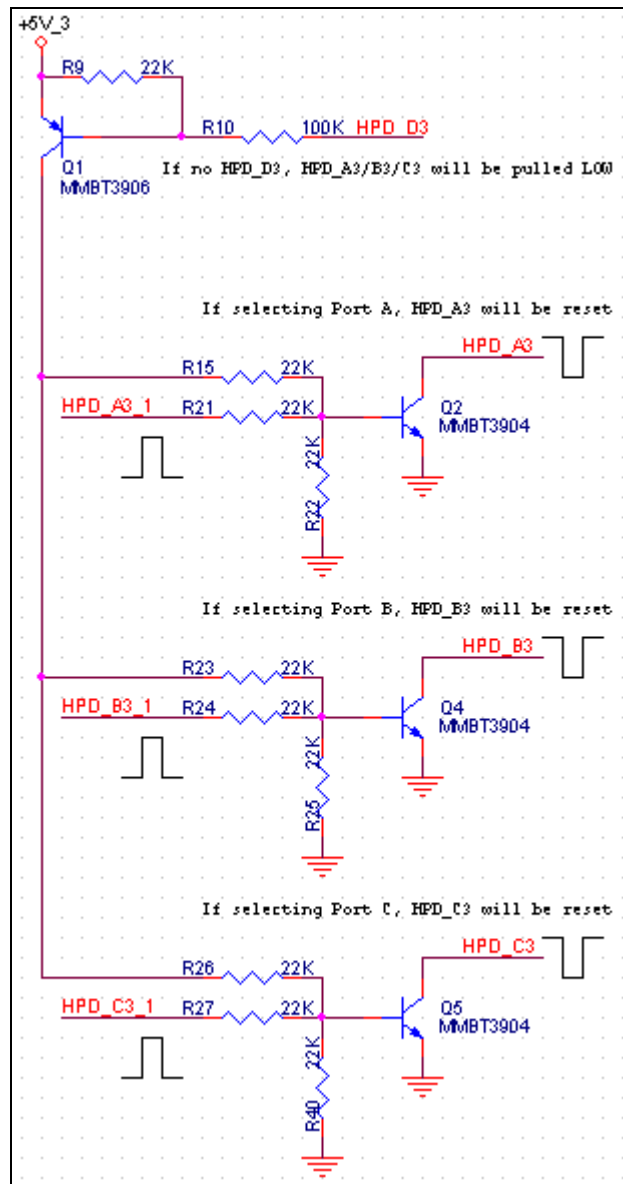


Figure 9: Source HPD Reset of PI3HDMI231-A Demo Board Rev.B

- c. If Sink receiver is not connected to HDMI connector J2, HPD_D3 pin will become low. This will turn on PNP transistor Q1 and then three NPN transistors Q2, Q4 and Q5 in Figure 9. As a result, all the HPD signals at source side are pulled low and reset to state H0.

- d. Since PI3HDMI231-A/B is a 3:1 ActiveEye™ HDMI switch, two SPDT switches at references SW1 and SW2 are used to select the connections of SCL_SINK and SDA_SINK among four conditions manually.

PI3HDMI231-A

SEL2	SEL1	SCL_SINK / SDA_SINK
H	H	SCL1 / SDA1
H	L	SCL2 / SDA2
L	L	SCL3 / SDA3
L	H	Are pulled HIGH by external pull-up terminations

Table 1a: Source Selection Look-up Table of PI3HDMI231-A

PI3HDMI231-B

SEL2	SEL1	SCL_SINK / SDA_SINK
H	H	SCL1 / SDA1
H	L	SCL2 / SDA2
L	L	SCL3 / SDA3
L	H	All SCLx & SDAx are shorted to SCL_sink & SDA_sink

Table 1b: Source Selection Look-up Table of PI3HDMI231-B

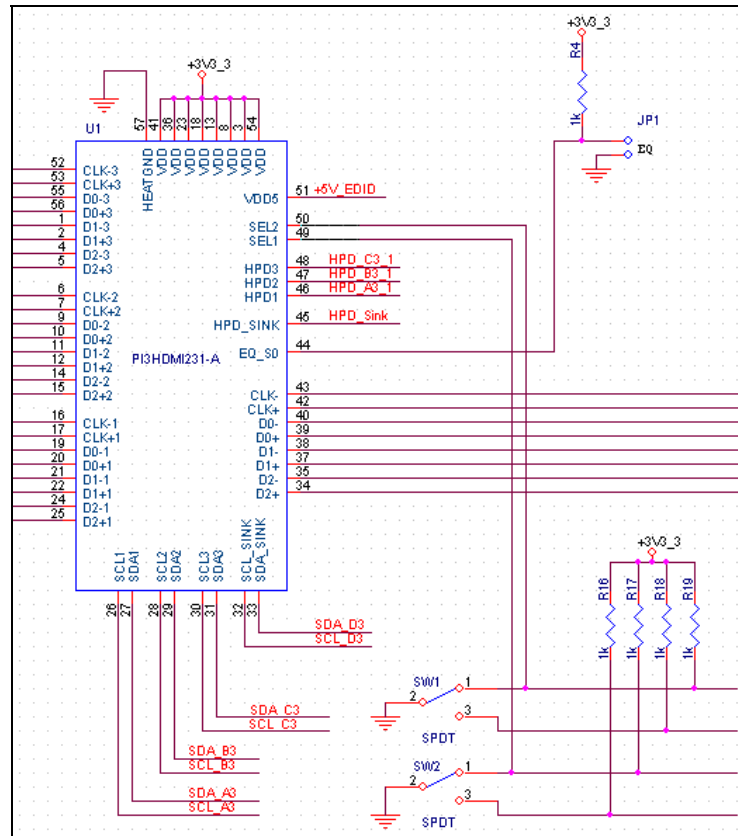


Figure 10: Schematic of Port Selection

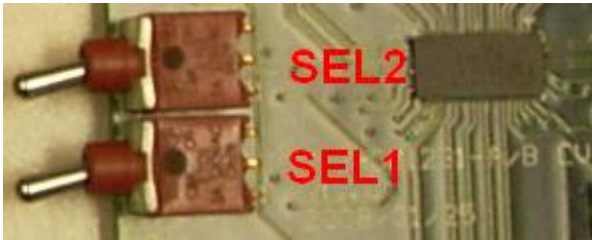


Figure 11a: Choosing Port 1



Figure 11b: Choosing Port 2



Figure 11c: Choosing Port 3



Figure 11d: Disconnecting All Terminations

- e. PI3HDMI231-A/B gives the opportunity to set equalization value of TMDs data via EQ_S0 pin. For short input cable application, EQ value is recommended to set as 6dB by leaving EQ_S0 pin float since it is internally 100kΩ pulled down or by shorting this pin to ground externally. For long input cable application, on the other hand, it is recommended to pull EQ_S0 pin to high by external resistor so as to set EQ value to 12dB. On PI3HDMI231-A/B demo board, EQ_S0 pin is initially pulled up by external resistor R4. In order to set this pin to low, a jumper has to be added to the header at reference JP1.

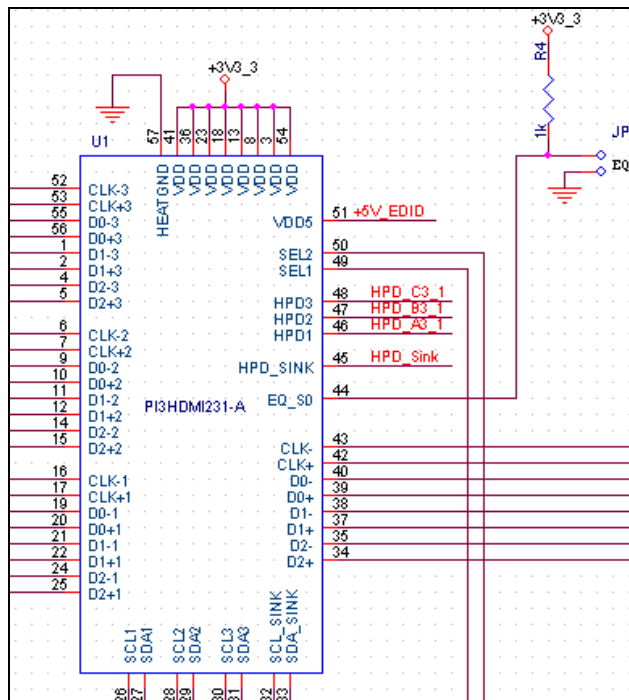


Figure 12: EQ Pin of PI3HDMI231-A Demo Board Rev.B

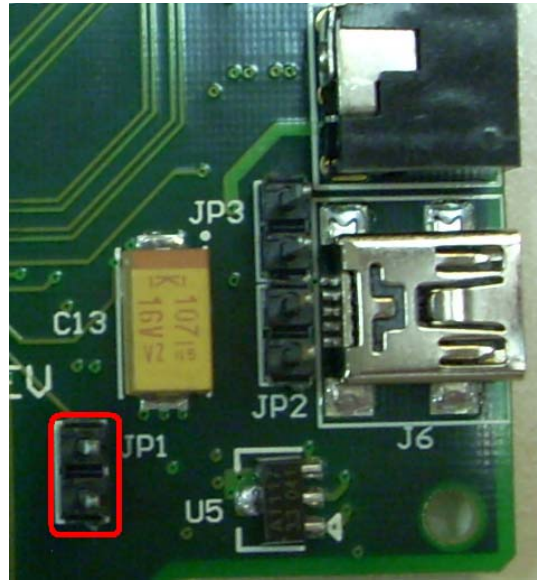


Figure 13: JP1 shown on PCB

- f. Three AT24C02B EEPROMs are implemented in PI3HDMI231-A/B demo board to model I2C application. The EEPROM is for DDC line capacitance measurement purpose. A0 and A1 address inputs of each AT24C02B are pulled to low by external pull-down resistors while address A2 is pulled high. Write protection of each EEPROM is disabled.

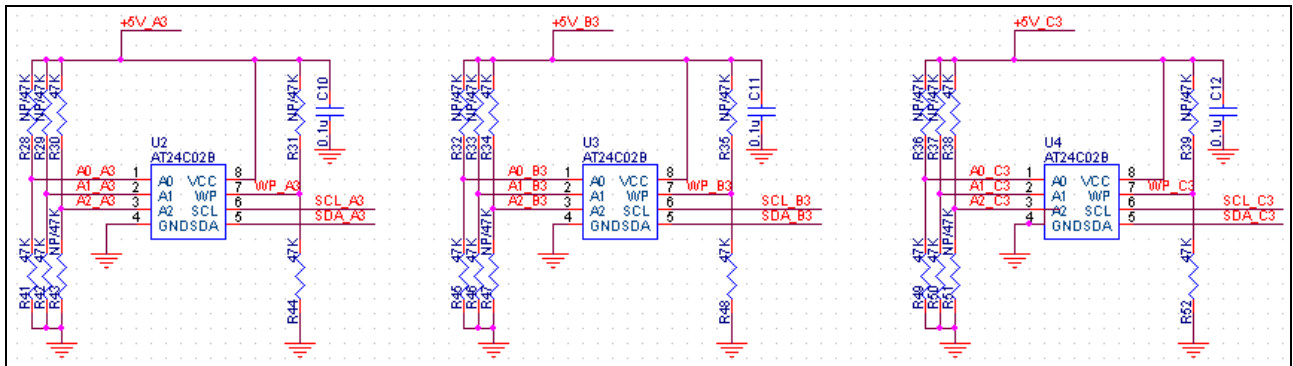


Figure 14: Schematic of EEPROM of PI3HDMI231-A Demo Board Rev.B

- g. In some DVD players, no sink current circuitry is implemented in TMDS. When these DVD players are de-selected, CLK signals stay at high level. To ensure the DVD players can enter idle mode when being de-selected, input CLK+/- pins are pulled down externally. 22kΩ pull-down resistors are added to CLK+ and - to pull CLK to low level when there is no 50Ω termination. HDCP can then be reset by RxSense when the port is being selected back. To maintain trace impedance consistency, it is recommended to avoid stub between pull-down resistor pad and CLK signal trace on PCB layout.

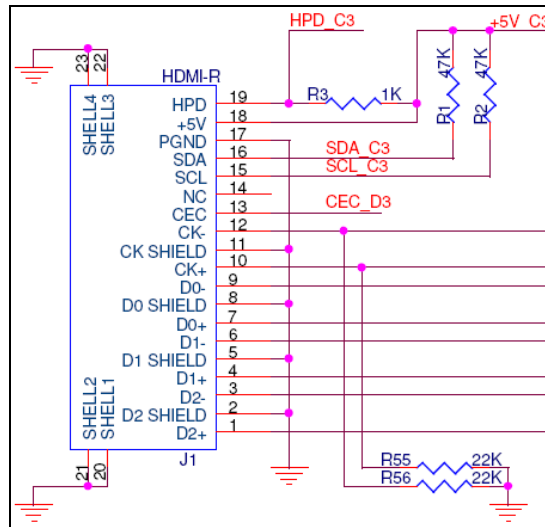


Figure 15: Input CLK External Pull-down of PI3HDMI231-A Demo Board Rev.B

Test Results

On PI3HDMI231-A demo board, few Source pre-test items are performed from (a) to (d) when 1920x1080p@60Hz input source of 8-bit RGB, 148.5MHz pixel rate and 673ps Tbit is used. An HDMI-R to SMA test fixture, 30cm SMA cables and P7350SMA differential probes are connected to D2 and CLK outputs. 2-meter 28-AWG and 10-meter 28-AWG cables are connected to input connector, one at a time, for 6dB and 12dB equalization evaluations.

Eye diagrams when a deep color (1920x1080p@60Hz of 12-bit RGB) input source is applied to the demo board are also captured in (d) when equalization is set to 12dB for 2-meter 28-AWG and 10-meter 28-AWG cable applications.

- a. Source Test ID 7-4: TMDS – Rise Time or Fall Time at 1920x1080p@60Hz Resolution & 8-bit RGB

EQ_S0	Cable Length	Output	T _{RISE}	T _{FALL}	Min Spec	Units
6 dB	2 meters	CLK+/-	157.43	158.47	75	ps
		D2+/-	142.81	137.44	75	ps
12 dB	10 meters	CLK+/-	155.41	152.94	75	ps
		D2+/-	133.35	124.56	75	ps

Table 2: Rise/Fall Times of TMDS at J2 when Resolution=1920x1080p@60Hz & RGB=8bit

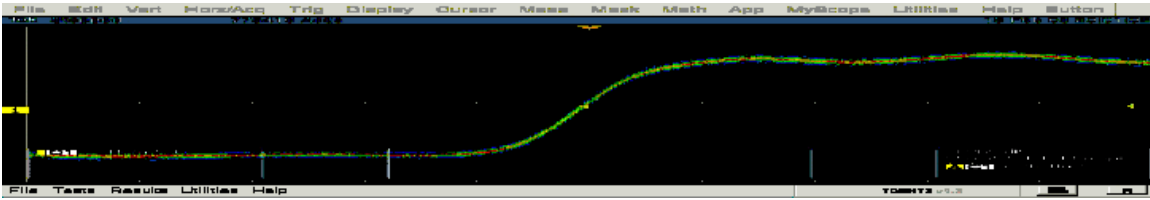


Figure 16a: T_{RISE} of CLK when EQ=6dB and Resolution=1920x1080p@60Hz & RGB=8bit

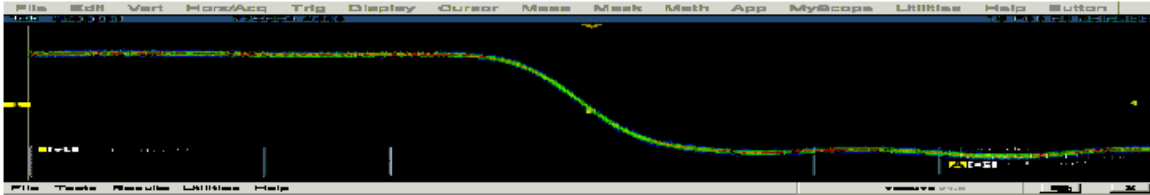


Figure 16b: T_{FALL} of CLK when EQ=6dB and Resolution=1920x1080p & RGB=8bit

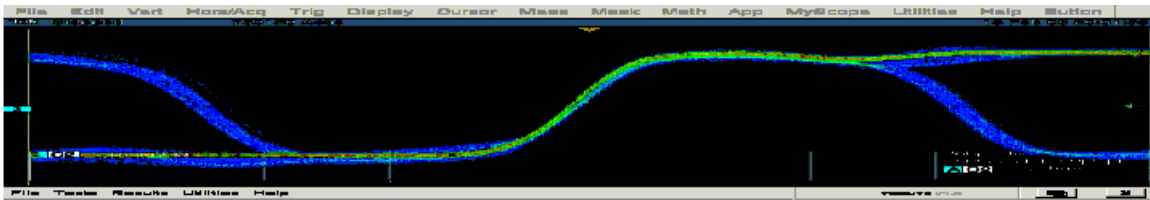


Figure 16c: T_{RISE} of D2 when EQ=6dB and Resolution=1920x1080p & RGB=8bit

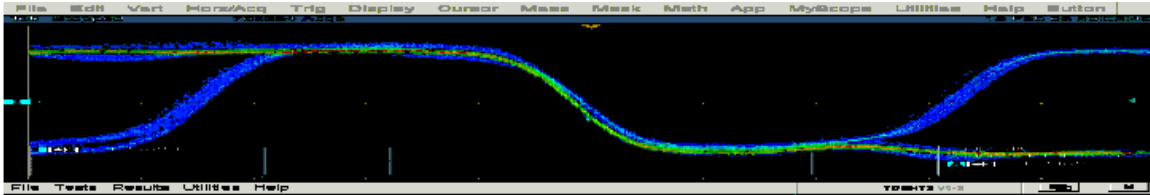


Figure 16d: T_{FALL} of D2 when EQ=6dB and Resolution=1920x1080p & RGB=8bit

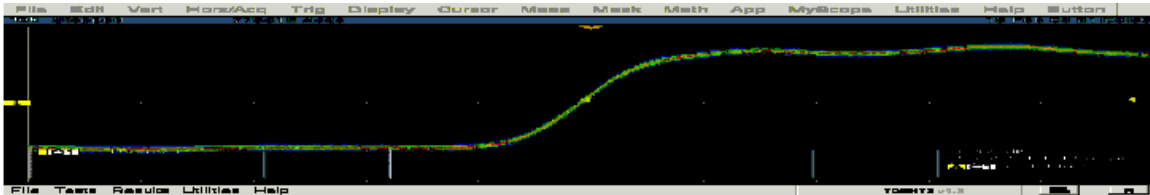


Figure 17a: T_{RISE} of CLK when EQ=12dB and Resolution=1920x1080p & RGB=8bit

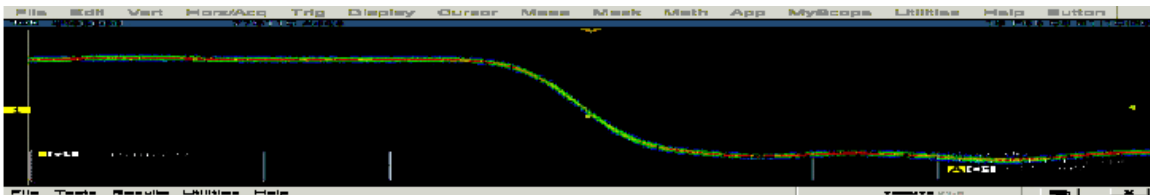


Figure 17b: T_{FALL} of CLK when EQ=12dB and Resolution=1920x1080p & RGB=8bit

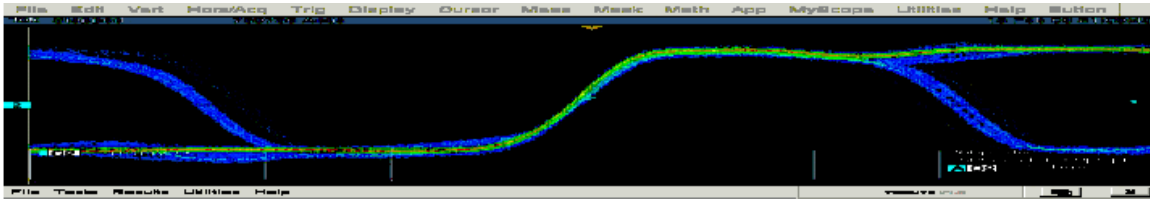


Figure 17c: T_{RISE} of D2 when EQ=12dB and Resolution=1920x1080p & RGB=8bit

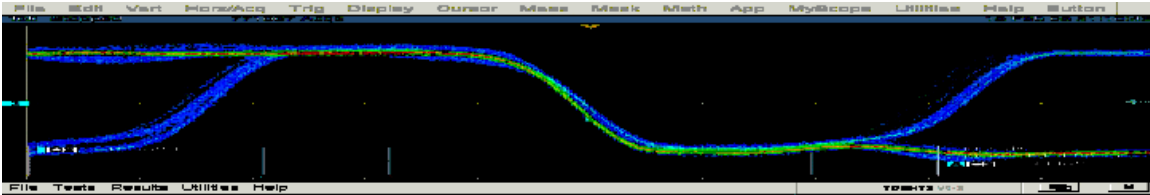


Figure 17d: T_{FALL} of D2 when EQ=12dB and Resolution=1920x1080p & RGB=8bit

b. Source Test ID 7-8: TMD5 – Clock Duty Cycle at 1920x1080p@60Hz Resolution & 8-bit RGB

EQ_S0	Cable Length	Output	Min Duty Cycle	Max Duty Cycle	Min Spec	Max Spec	Units
6 dB	2 meters	CLK+/-	49.90	50.49	40	60	%
12 dB	10 meters	CLK+/-	49.60	50.49	40	60	%

Table 3: Clock Duty Cycle at J2 when Resolution=1920x1080p@60Hz & RGB=8bit

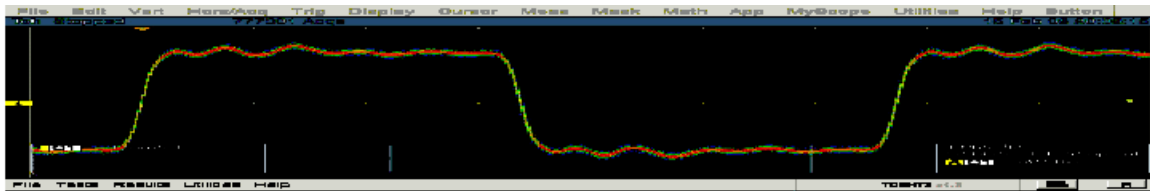


Figure 18a: Max Duty Cycle of CLK when EQ=6dB and Resolution=1920x1080p@60Hz & RGB=8bit

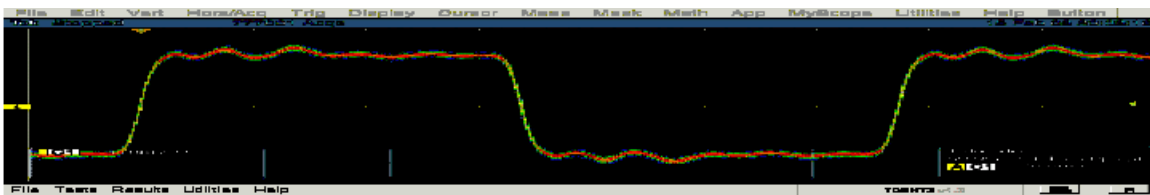


Figure 18b: Min Duty Cycle of CLK when EQ=6dB and Resolution=1920x1080p@60Hz & RGB=8bit

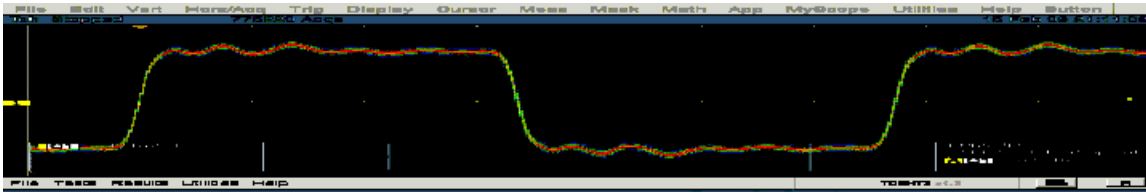


Figure 19a: Max Duty Cycle of CLK when EQ=12dB and Resolution=1920x1080p@60Hz & RGB=8bit

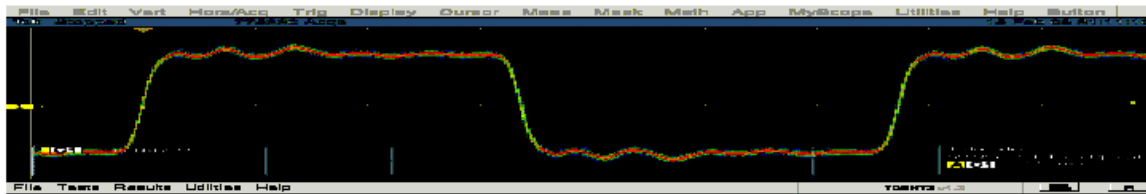


Figure 19b: Min Duty Cycle of CLK when EQ=12dB and Resolution=1920x1080p@60Hz & RGB=8bit

c. Source Test ID 7-9: TMDS – Clock Jitter at 1920x1080p@60Hz Resolution & 8-bit RGB

EQ_S0	Cable Length	Output	Clock Jitter	Max Spec	Units
6 dB	2 meters	CLK+/-	0.071	0.25	T _{BIT}
12 dB	10 meters	CLK+/-	0.076	0.25	T _{BIT}

Table 4: Clock Jitter at J2 when Resolution=1920x1080p@60Hz & RGB=8bit

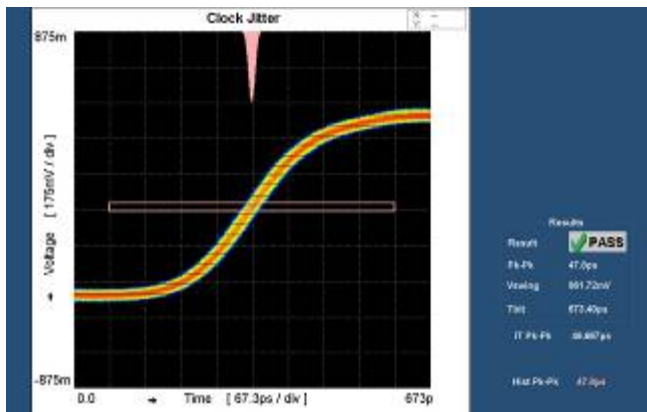


Figure 20: Clock Jitter of CLK when EQ=6dB, Resolution=1920x1080p@60Hz & RGB=8bit

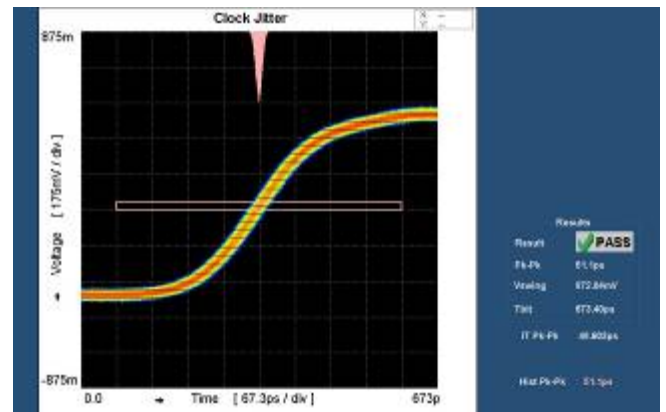


Figure 21: Clock Jitter of CLK when EQ=12dB, Resolution=1920x1080p@60Hz & RGB=8bit

d. Source Test ID 7-10: TMDS – Data Jitter & Eye Diagrams at 1920x1080p@60Hz Resolution & 8-bit RGB

EQ_S0	Cable Length	Output	Data Jitter	Max Spec	Units
6 dB	2 meters	CLK+/-	0.17	0.3	T _{BIT}
12 dB	10 meters	CLK+/-	0.20	0.3	T _{BIT}

Table 5a: Data Jitter at J2 when Resolution=1920x1080p@60Hz & RGB=8bit

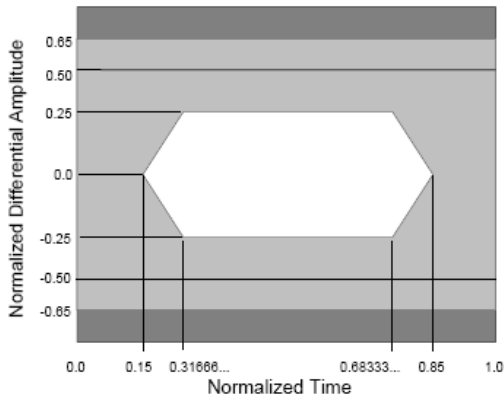


Figure 22: Source Eye Diagram

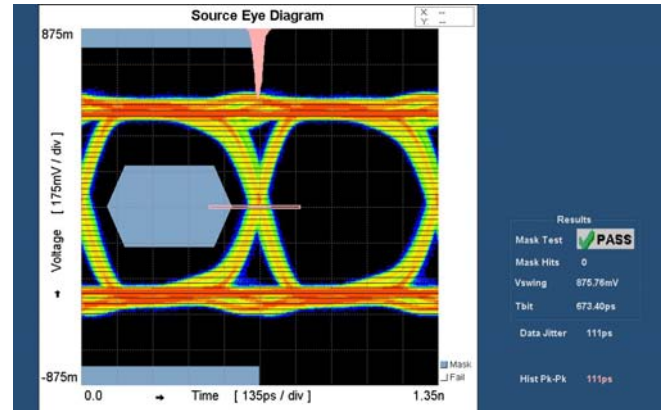


Figure 23: Eye Diagram of D2 when EQ=6dB, Resolution=1920x1080p@60Hz & RGB=8bit

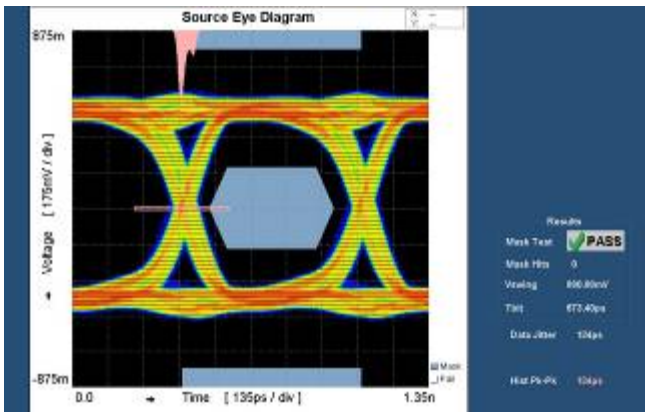


Figure 24: Eye Diagram of D2 when EQ=12dB, Resolution=1920x1080p@60Hz & RGB=8bit

Source Test ID 7-10: TMDS – Data Jitter & Eye Diagrams at 1920x1080p@60Hz & 12-bit RGB

EQ_S0	Cable Length	Output	Data Jitter	Max Spec	Units
12 dB	2 meters	CLK+/-	0.18	0.3	T _{BIT}
12 dB	10 meters	CLK+/-	0.27	0.3	T _{BIT}

Table 5b: Data Jitter at J2 when Resolution=1920x1080p@60Hz & RGB=12bit

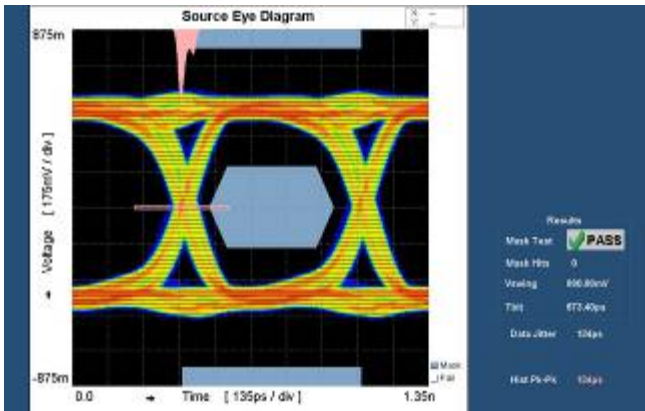


Figure 25: Eye Diagram of D2 when Cable Length=2m, Resolution=1920x1080p@60Hz & RGB=12bit

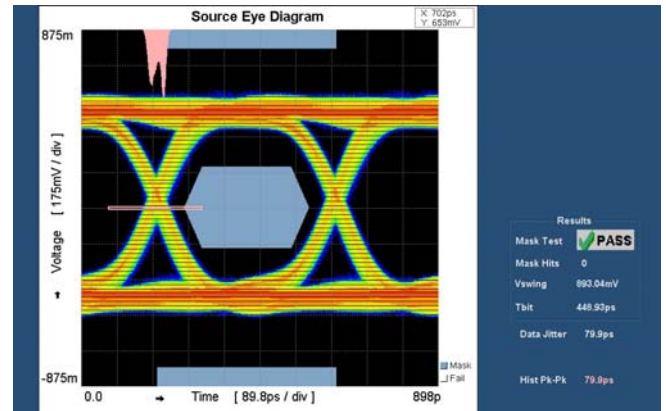


Figure 26: Eye Diagram of D2 when Cable Length=10m, Resolution=1920x1080p@60Hz & RGB=12bit

e. Sink Test ID 8-8: TDR Measurement

Differential impedance of PI3HDMI231-A on an HDMI-HDMI demo board is measured to confirm the trace impedance is within the requirement described in Test ID 8-8 in HDMI Compliance Test Specification Version 1.3a.

Test ID 8-8: TMDS – Differential Impedance

Reference	Requirement
[HDMI: Table 4-20] HDMI Sink Impedance at TP2	Through-connection impedance : $100\Omega \pm 15\%^*$ * A single excursion is permitted out to a max/min of 100 ohms $\pm 25\%$ and of a duration less than 250psecs. At Termination impedance (when Vicm is within Vicm1 range) $100\text{ ohms} \pm 10\%$

Table 6: HDMI Pre-test Test ID 8-8 Specification

CDF field Sink_Diff_PowerOn = N for each TMDS input. The termination is switched from 50Ω to 800kΩ pull-up when PI3HDMI231-A is not powered up. Thus, at-termination impedance cannot be obtained at TMDS channel.

Through impedance is measured at input side of the demo board. Filter of 180ps is employed throughout the following measurement.

For Port 1,

- Sink_Term_Distance of D2 = 0.52ns
- Sink_Term_Distance of D1 = 0.50ns
- Sink_Term_Distance of D0 = 0.46ns
- Sink_Term_Distance of CLK = 0.46ns

For Port 2,

- Sink_Term_Distance of D2 = 0.42ns
- Sink_Term_Distance of D1 = 0.40ns
- Sink_Term_Distance of D0 = 0.40ns
- Sink_Term_Distance of CLK = 0.40ns

For Port 3,

- Sink_Term_Distance of D2 = 0.50ns
- Sink_Term_Distance of D1 = 0.48ns
- Sink_Term_Distance of D0 = 0.52ns
- Sink_Term_Distance of CLK = 0.52ns

Through Impedance		D2	D1	D0	CLK	Spec		Units
						Min	Max	
Port 1	Min	98	95	94	95	85	115	Ω
	Max	109	107	105	107	85	115	Ω
Port 2	Min	97	94	94	94	85	115	Ω
	Max	109	107	107	108	85	115	Ω
Port 3	Min	98	94	95	95	85	115	Ω
	Max	110	108	109	109	85	115	Ω

Table 7: Through Impedance Result

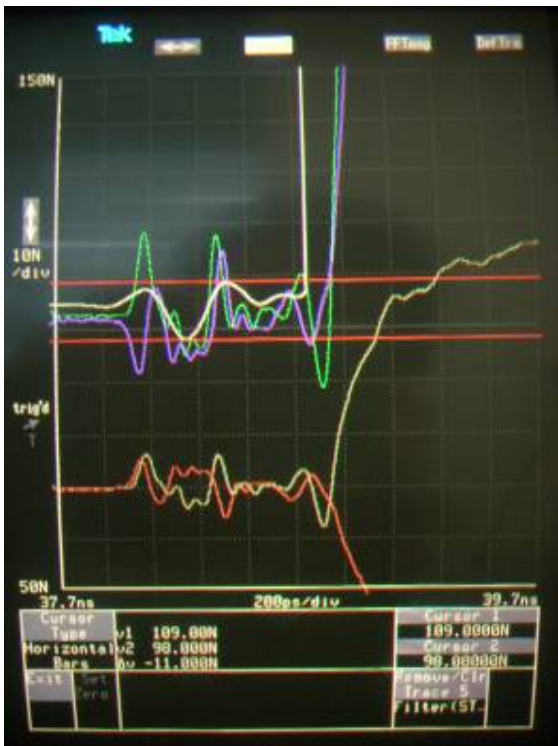


Figure 27a: Through Impedance of D2 at Port 1

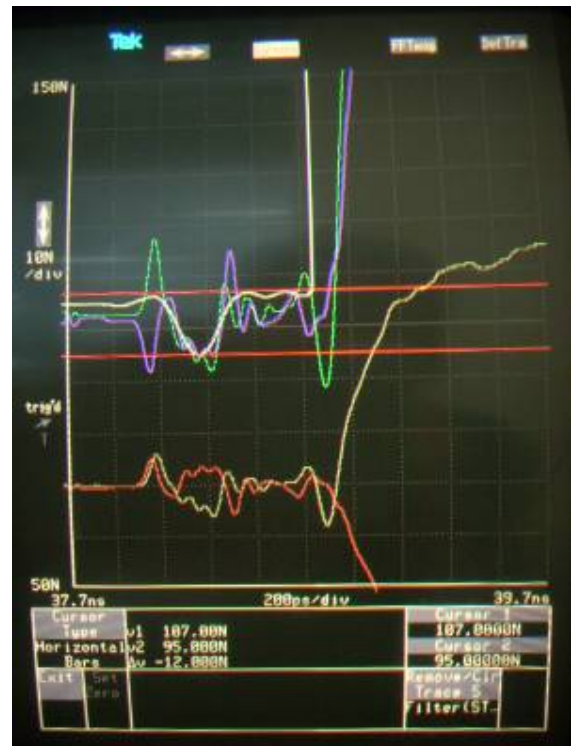


Figure 27b: Through Impedance of D1 at Port 1



Figure 27c: Through Impedance of D0 at Port 1

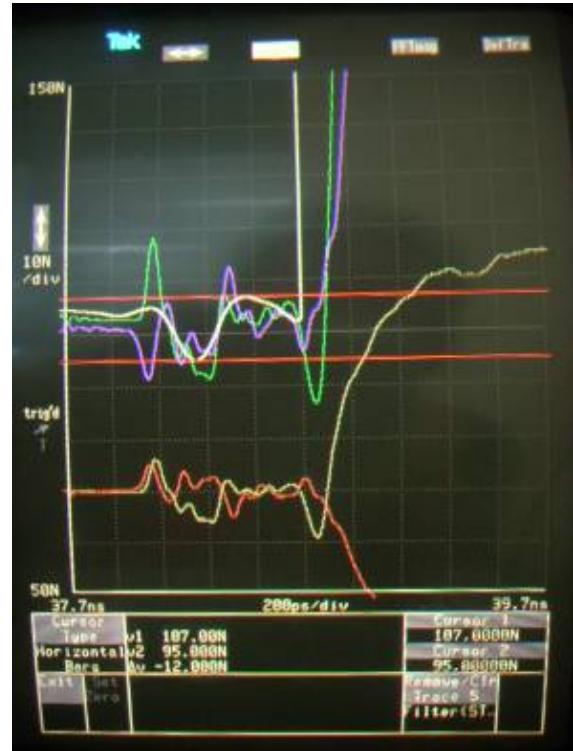


Figure 27d: Through Impedance of CLK at Port 1

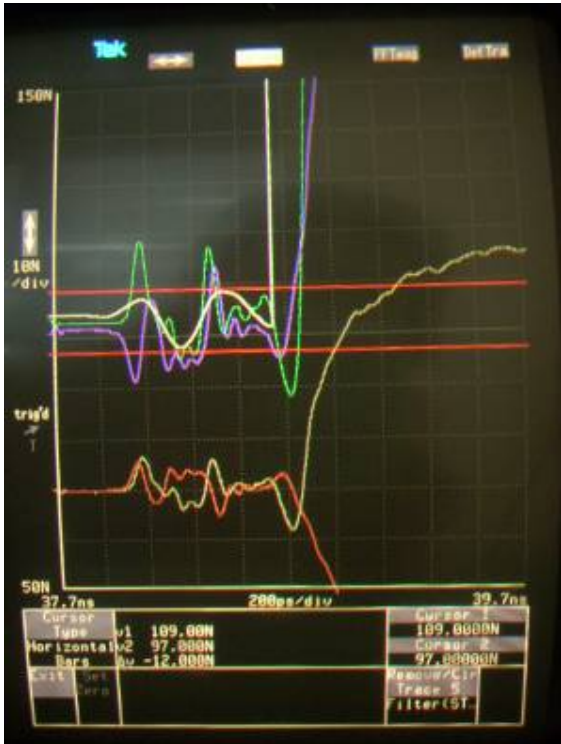


Figure 28a: Through Impedance of D2 at Port 2

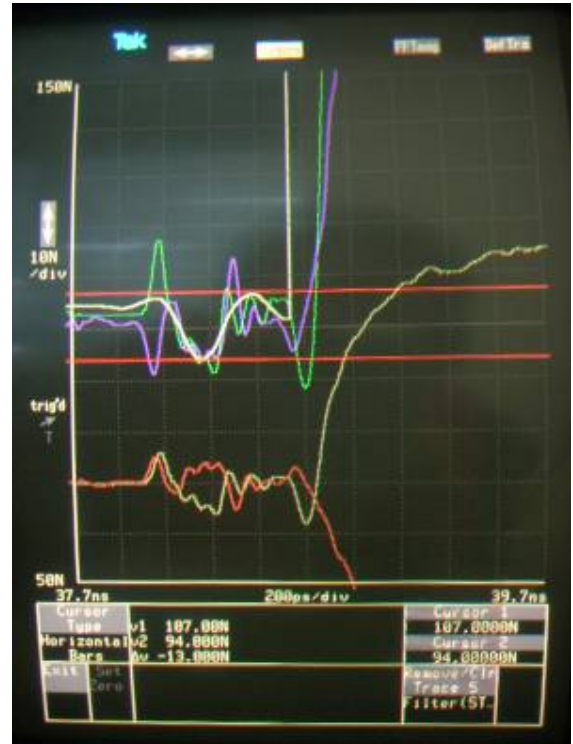


Figure 28b: Through Impedance of D1 at Port 2



Figure 28c: Through Impedance of D0 at Port 2

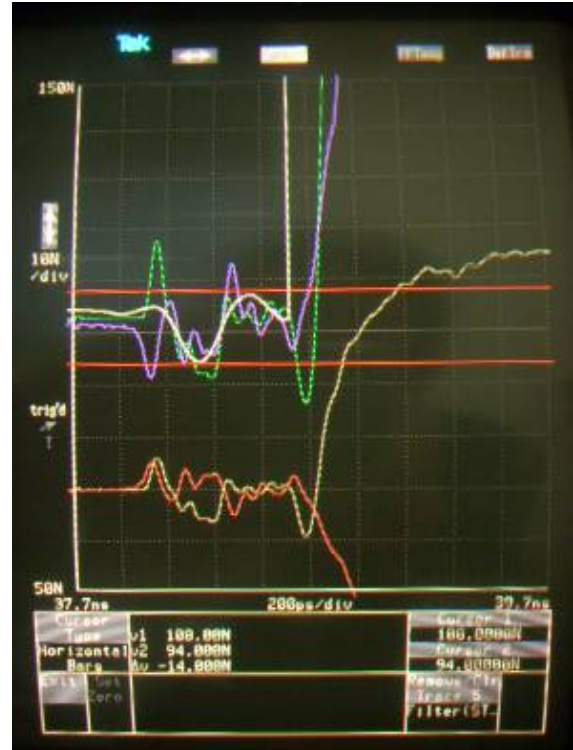


Figure 28d: Through Impedance of CLK at Port 2

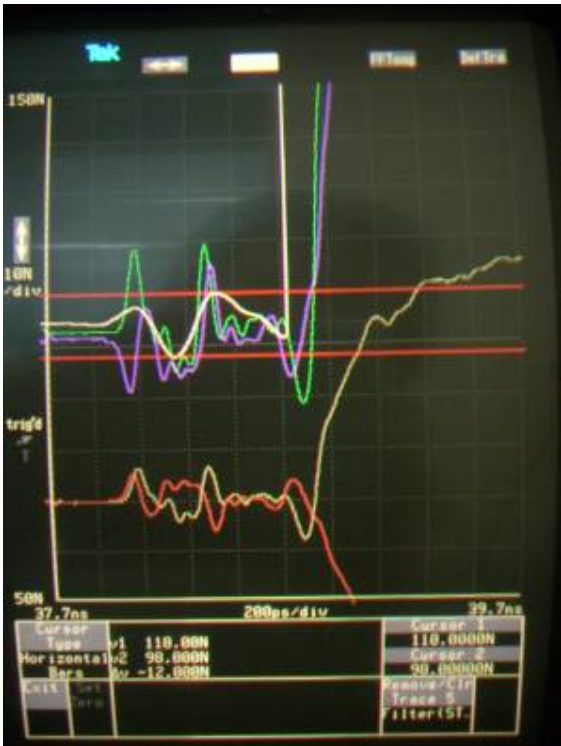


Figure 29a: Through Impedance of D2 at Port 3

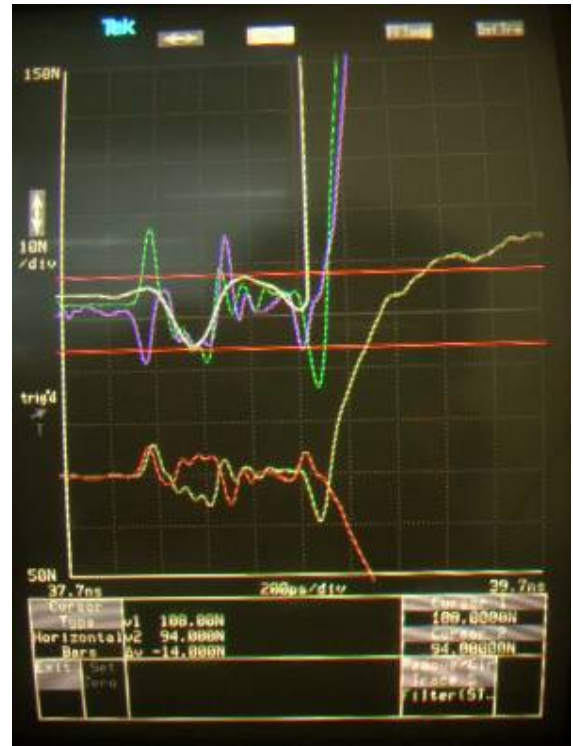


Figure 29b: Through Impedance of D1 at Port 3

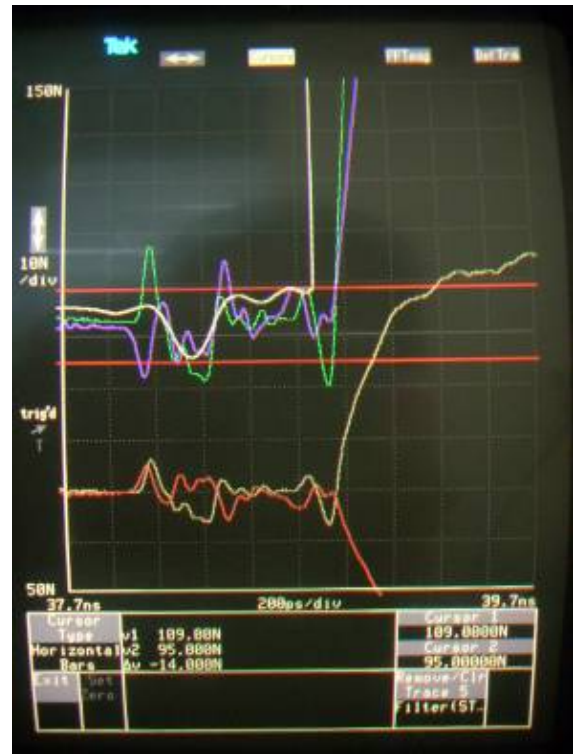


Figure 29c: Through Impedance of D0 at Port 3

Figure 29d: Through Impedance of CLK at Port 3

f. Power Consumption from Power Jack

PI3HDMI231-A/B offers power saving modes when it is not fully active. If 5V is not applied to VDD5 pin (pin 51), PI3HDMI231-A/B enters sleep mode. If TMDS signal is less than V_{th} voltage level, which is $VDD-0.6V$ or 2.7V, PI3HDMI231-A/B enters standby mode. If setting SEL2 and SEL1 to L and H, respectively, the DDC signals of PI3HDMI231-A/B enter Hi-Z state. Current consumed from the Power Jack at J5, when JP3 is not connected, is measured on demo board.

Mode	Icc	Units
Sleep	19	mA
Standby	66	mA
Hi-Z	18	mA
Full Active	119	mA

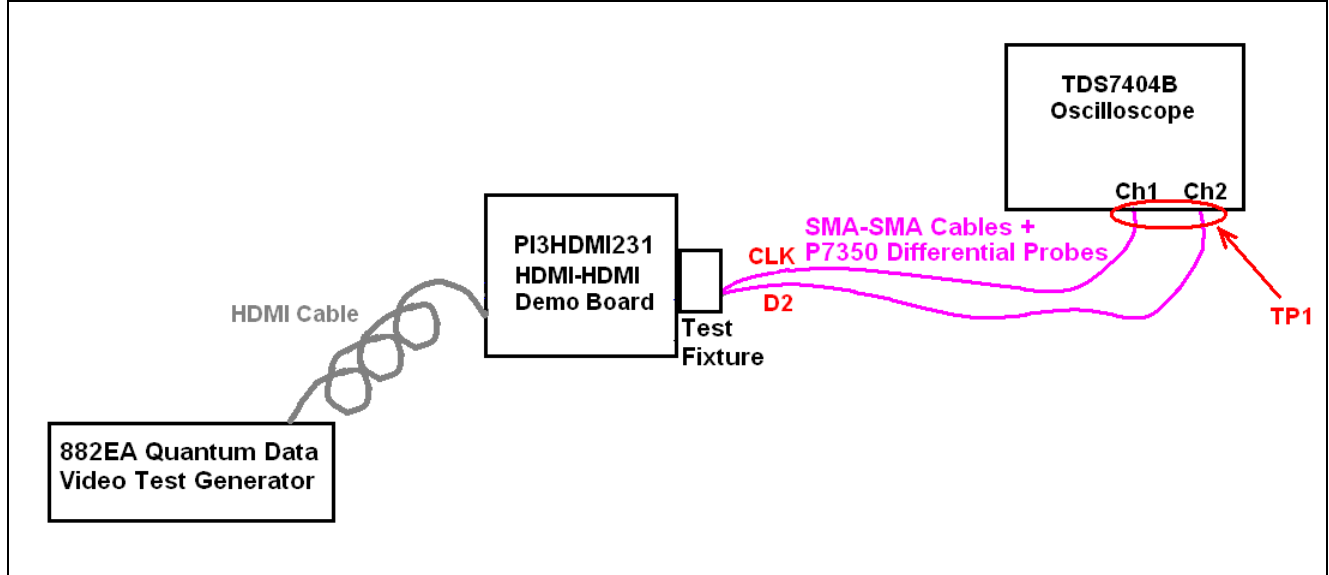
Table 8: ICC from Power Jack of PI3HDMI231-A

The current consumed by the regulator at U5 and all the passive components on demo board is about 16mA.

Appendix A: Test Setup

Test setup:

a. For Source Test



Equipment Use:

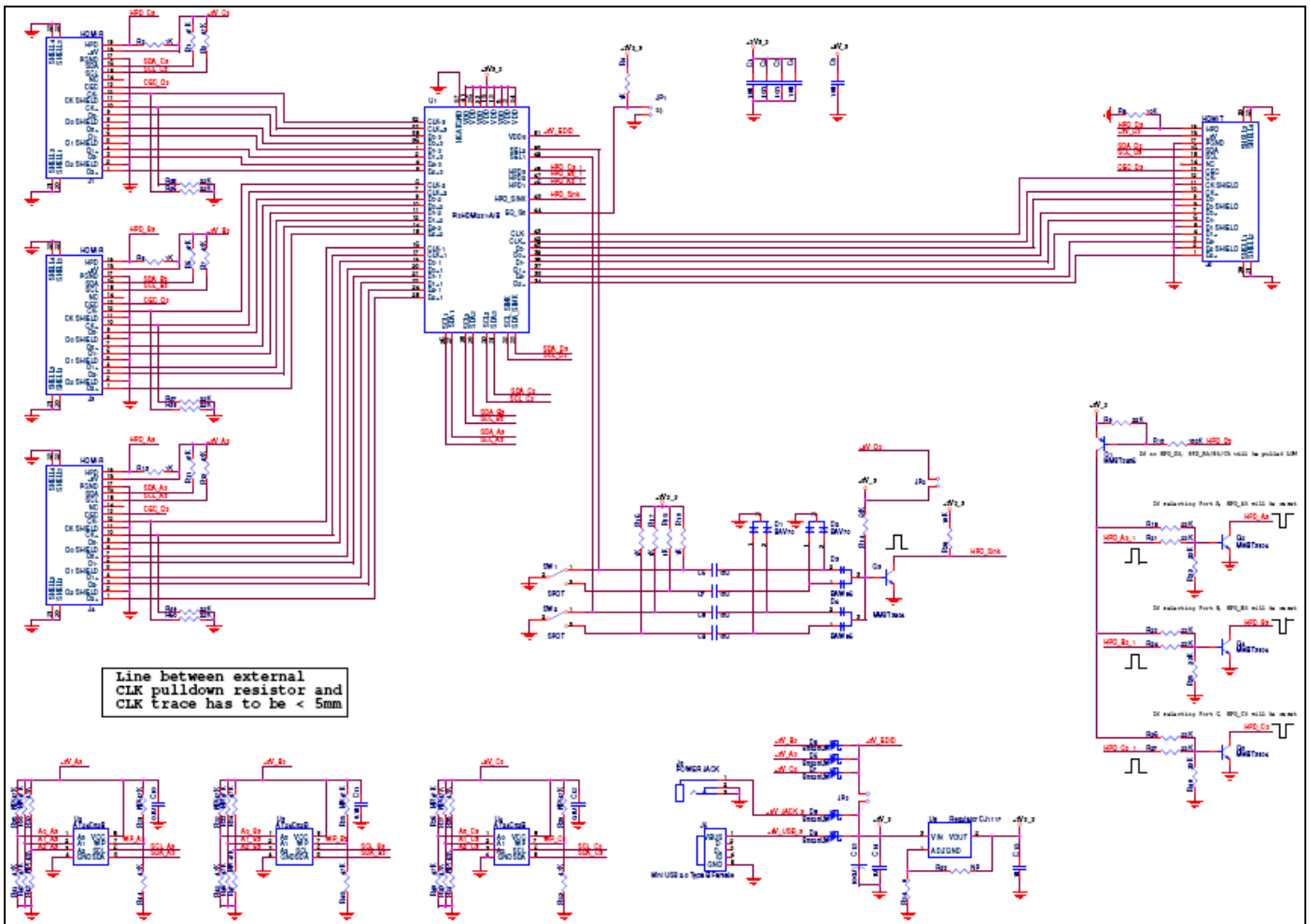
a. For Source Test

- TDS7404B Oscilloscope with P7350SMA Differential Probes
- 30cm SMA-SMA Cables
- 2-meter 28-AWG and 10-meter 28-AWG HDMI Cables
- HDMI-R to SMA Test Fixture
- 882EA Quantum Data Video Test Generator
- Agilent Power Supply
- 5V DC Adaptor

b. For Sink Test

- Tek11801C Digital Sampling Oscilloscope
- Agilent 4395A Impedance Analyzer with 43961A and 16092A
- SMA Matching Cables
- PSC High BW TDR Test Fixture
- PSC High BW Cap Test Fixture
- Agilent Power Supply
- 5V DC Adaptor

Appendix B: PCB Schematic



Appendix C: PCB Layout Requirements

a. Stack Up:

Plane	Material	Thickness (mil)
Signal		1.9
Prepreg	1080 + 2116	7.3
Ground		1.2
Core		44
Power		1.2
Prepreg	1080 + 2116	7.3
Signal		1.9

b. Isolation Spacing = 30 mil

c. Width & Spacing (W/S) of 100Ω Differential Trace = 9.0 / 10 mil

* W/S for 80 mils before and after contacting the TMDS input/output pads of PI3HDMI231 = 5.0 / 15 mil to compensate the impedance drop of PI3HDMI231 solder pads

Appendix D: BOM List

Item	Quantity	Reference	Description
1	5	C1, C2, C3, C4, C5	10nF Capacitor
2	4	C6, C7, C8, C9	10uF Capacitor
3	3	C10, C11, C12	0.1uF Capacitor
4	1	C13	100uF Capacitor
5	2	C14, C15	1uF Capacitor
6	2	D1, D2	BAV70 Common Cathode Double Diode
7	2	D3, D4	BAW56 Common Anode Double Diode
8	5	D5, D6, D7, D8, D9	B0520LW Schottky Rectifier
9	3	JP1, JP2, JP3	2-pin Header
10	3	J1, J3, J4	HDMI Receptacle Connector
11	1	J2	HDMI Plug Connector
12	1	J5	Power Jack
13	1	J6	Mini USB Female Connector
14	1	Q1	MMBT3906 PNP Transistor
15	4	Q2, Q3, Q4, Q5	MMBT3904 NPN Transistor
16	18	R1, R2, R6, R7, R11, R12, R30, R34, R38, R41, R42, R44, R45, R46, R48, R49, R50, R52	47kΩ Resistor
17	8	R3, R4, R8, R13, R16, R17, R18, R19	1kΩ Resistor
18	2	R5, R20	10kΩ Resistor
19	16	R9, R15, R21, R22, R23, R24, R25, R26, R27, R40, R55, R56, R57, R58, R59, R60	22kΩ Resistor
20	1	R10	100kΩ Resistor
21	1	R14	68kΩ Resistor
22	13	R28, R29, R31, R32, R33, R35, R36, R37, R39, R43, R47, R51, R53	NOT CONNECTED
23	1	R54	0Ω Resistor
24	2	SW1, SW2	SPDT Switch
25	1	U1	PI3HDMI231-A HDMI Switch
26	3	U2, U3, U4	AT24C02B EEPROM
27	1	U5	1117 Regulator