PI3HDMI201

PI3HDMI201 HDMI-HDMI Demo Board Rev.A User Manual

by Ada Yip

Introduction

This user manual describes the components and the usage of PI3HDMI201 Demo Board Rev.A. HDMI connectors are used as input and output connectors for the following HDMI-HDMI demo board version.

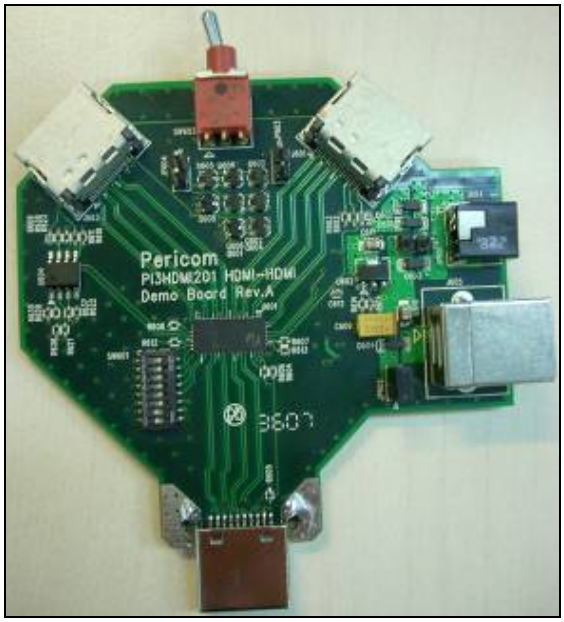


Figure 1a: Top View of PI3HDMI201 HDMI-HDMI Demo Board

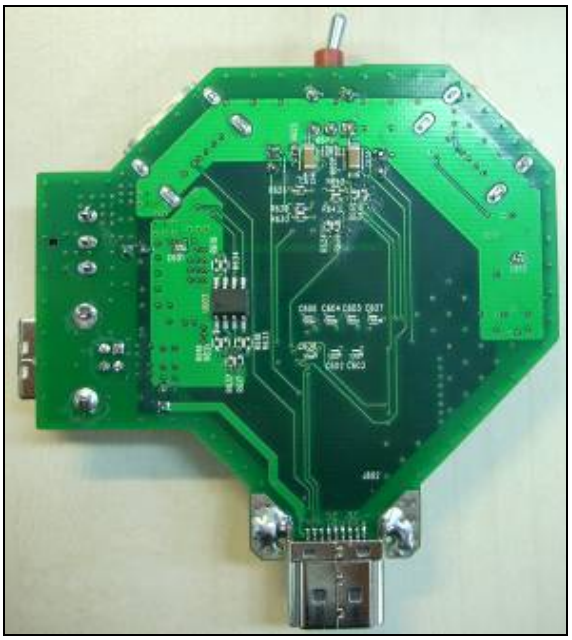


Figure 1b: Bottom View of PI3HDMI201 HDMI-HDMI Demo Board

Key Components / Circuits

a. 5V of PI3HDMI201 demo board can be supplied via three ways, i.e. using 5V supplied from Input Port, Power Jack, or from USB Type B Connector. Jumper JP601 on demo board is not connected at default. If using voltage of input port to power up the entire board, jumper must be added.

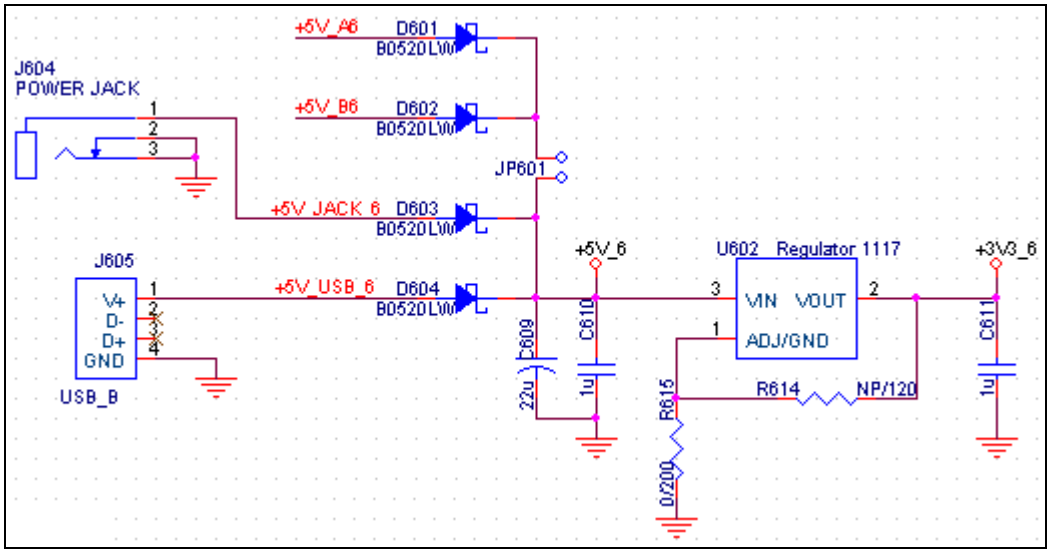


Figure 2: Schematic of 5V Power Supply of PI3HDMI201 HDMI-HDMI Demo Board

5V supplying to output HDMI connector is provided by +5V_6 power via shorting Jumper JP602.

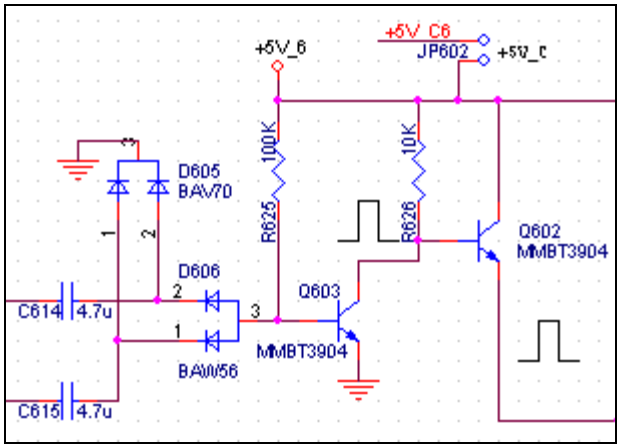


Figure 3: Schematic of 5V Power Supply to Output HDMI Connector

b. The voltage of HPD signal at output HDMI connector, HPD_C6, is sent through HPD_Sink pin to HPDA pin (so called HPD_A1_6) or HPDB pin (so called HPD_B1_6) on PI3HDMI201. The signals at these two pins are then used to control input HPD voltage level at Ports A and B through transistors Q601 and Q605 below. If Sink is not connected at output HDMI connector, HPD_C6 on PI3HDMI201 will be low and cause HPD_A1_6 and HPD_B1_6 appearing low. When HPD_A1_6 is low, Q601 will be closed, and Q604 will then be closed to pull HPD_A6 signal of HDMI input connector at Port A to ground. This is to alert Source that no Sink is connected to PI3HDMI201. HPD_B1_6 works in the same way as HPD_A1_6.

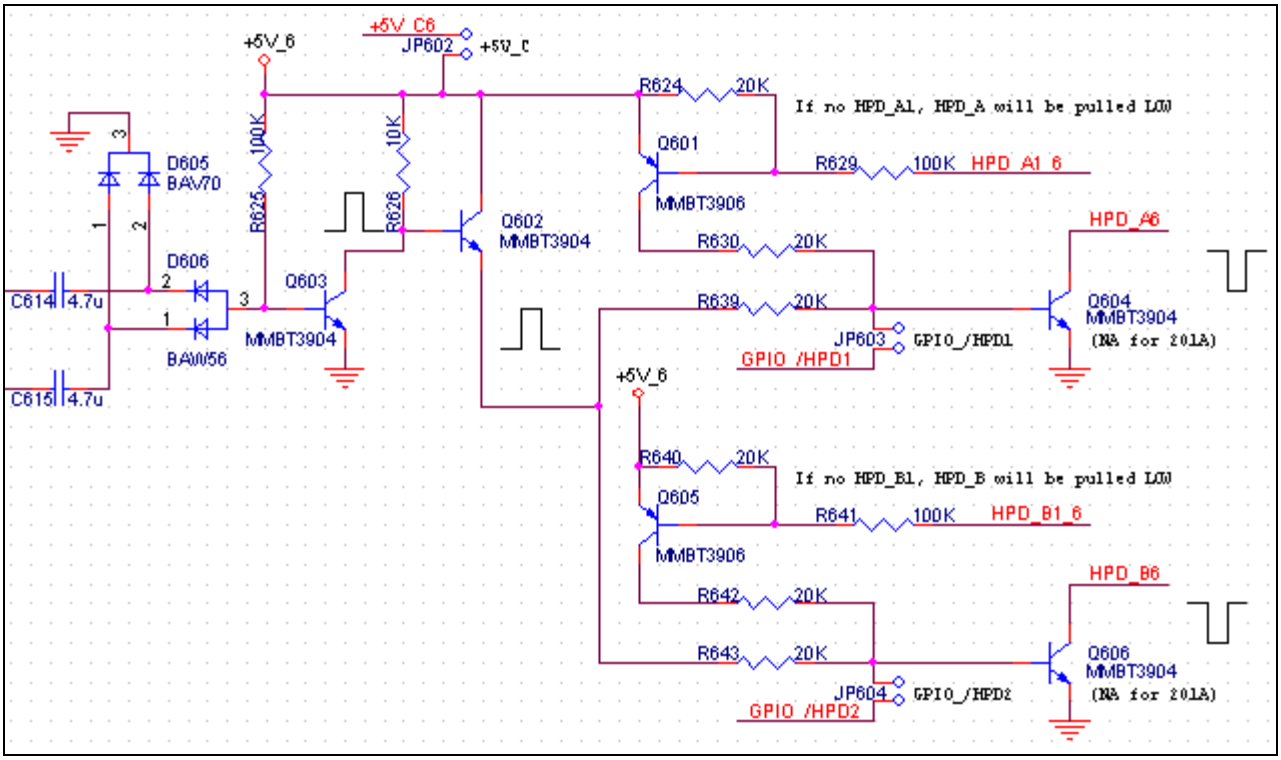


Figure 4: Control of Sink HPD of PI3HDMI201 HDMI-HDMI Demo Board

c. As PI3HDMI201 is a 2:1 MUX, a SPDT switch at reference SW602 is used to choose either Port A or B as the input port manually.

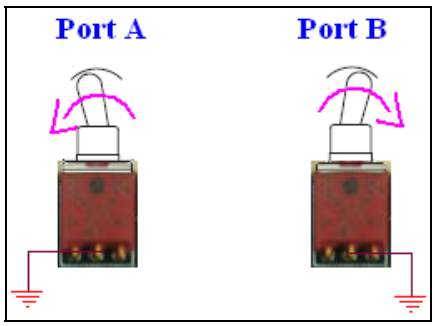


Figure 5: SPDT Switch SW602

When switch SW602 is tied to Port A, SEL1 and SEL2 pins of PI3HDMI201 are set to 3.3V and 0V, respectively. HPD_Sink pin is therefore connected to HPDA pin while HPDB becomes low. When SW602 is switched to Port B, the voltages of SEL1 and SEL2 are swapped. In this case, HPD_Sink is connected to HPDB pin. Pins 9 and 10 on switch SW601 are for evaluation use only. They should be tied to high through resistors R627 and R628 and controlled by SW602 manually.

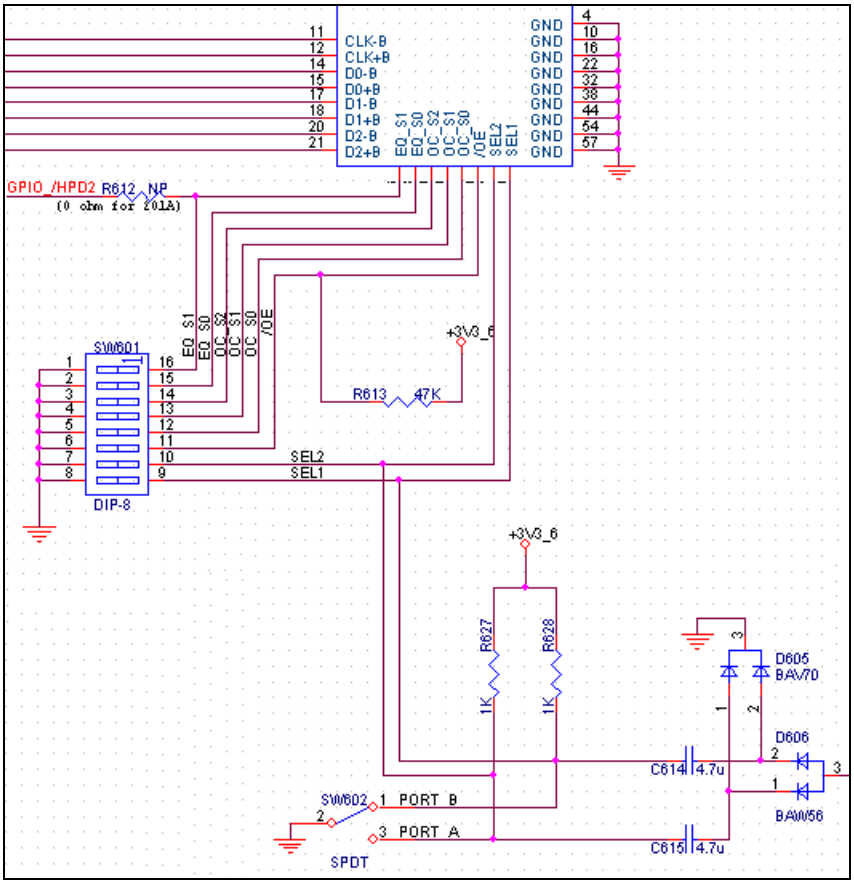


Figure 6: Schematic of Port Selection

d. A 250ms pulse is generated once switching is employed at switch SW602. The pulse is used to pull HPD_A6 and HPD_B6 signals at HDMI input ports to low for 250ms so as to reset HDCP Transmitter Link State back to reset state H0. For details, please refer to Application Note AN202.

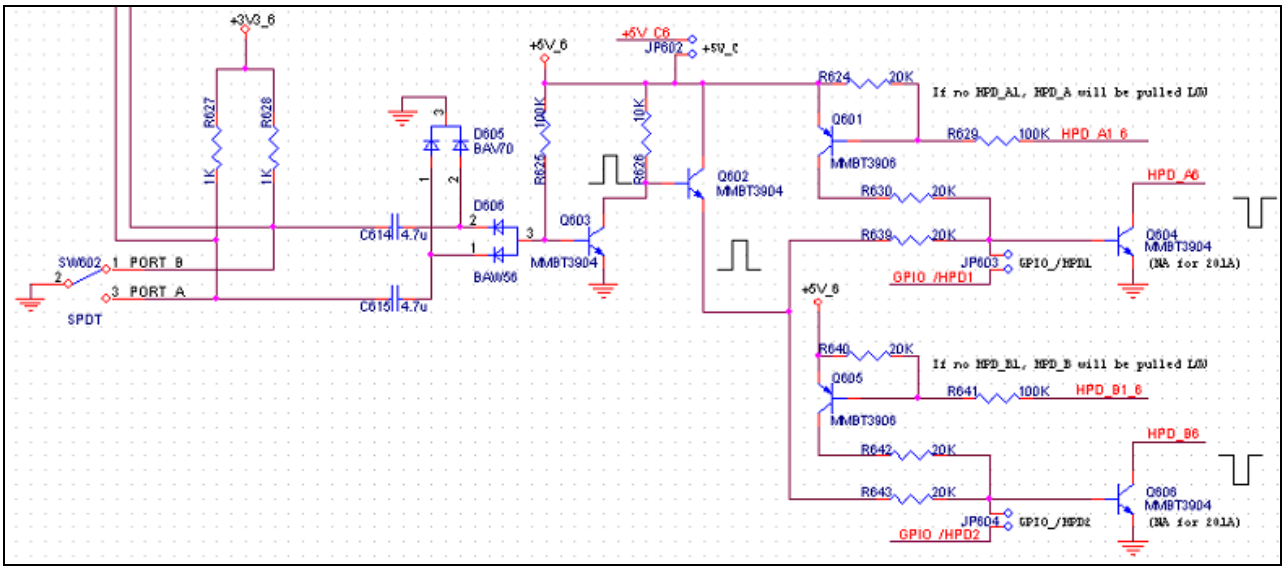


Figure 7: HPD Reset Circuit

e. Output Swing, De-emphasis and Equalization of signals can be adjusted by setting EQ_S[1:0] and OC_S[2:0] pins through switch SW601. These few control pins have internal pull-ups. Enable pin, /OE, can also be set using SW601. To enable the outputs of PI3HDMI201, /OE has to be shorted to ground.

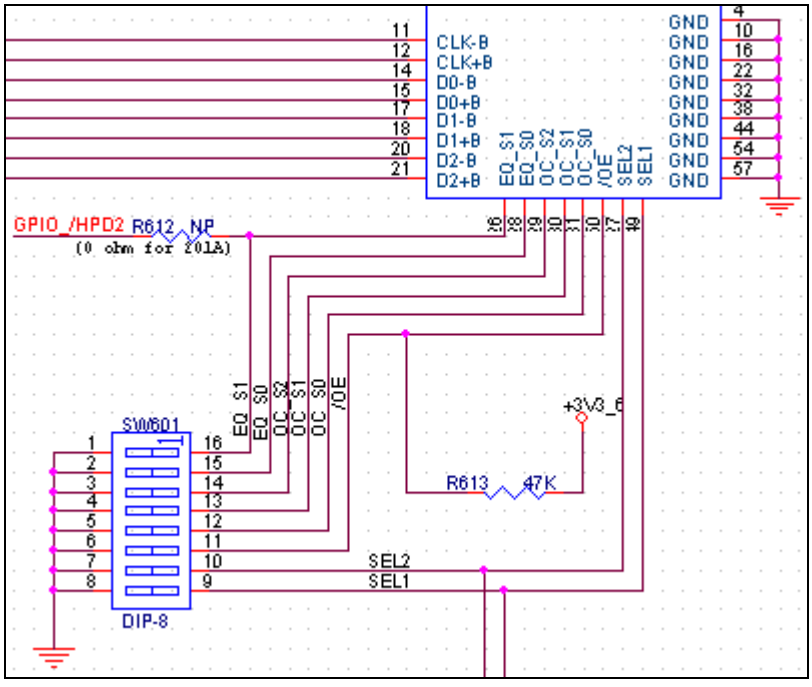


Figure 8: Control Pins of PI3HDMI201 HDMI-HDMI Demo Board

f. Two AT24C02B EEPROMs are implemented in PI3HDMI201 demo board to model I2C application. The EEPROM is for DDC line capacitance measurement purpose. Please refer to p.16 for measurement result. A0 and A1 address inputs of each AT24C02B are pulled to low by external pull-down resistors while address A2 is pulled high. Write protection of each EEPROM is disabled.

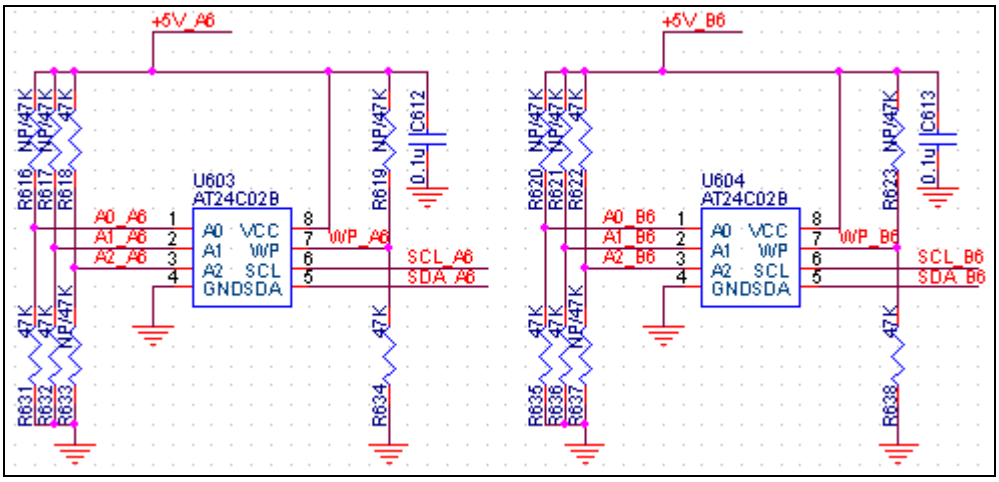


Figure 9: Schematic of EEPROM of PI3HDMI201 HDMI-HDMI Demo Board

Test Results

Few Source and Sink pre-test items are performed below. Source pre-test results with three output settings of swing and pre-/de-emphasis are tabulated. These three settings can generate passing eye diagrams with 1-meter cables connecting to both input and output connectors. All the eye diagrams of 8 different output settings are attached in section (d) below for reference.

a. Source Test ID 7-3: TMDS – V_{OFF}

TMDS single-ended standby (off) output voltage is tested when 50Ω resistor at each TMDS signal is pulled up by 3.3V AVcc.

Output	V_{OFF}	Spec		Units
		Min	Max	
D2+	0	-10	10	mV
D2-	0	-10	10	mV
D1+	0	-10	10	mV
D1-	0	-10	10	mV
D0+	0	-10	10	mV
D0-	0	-10	10	mV
CLK+	0	-10	10	mV
CLK-	0	-10	10	mV

Table 1: V_{OFF} at Connector J602

b. Source Test ID 7-4: TMDS – Rise Time or Fall Time at 3dB Equalization & 1920x1080i Resolution

OC_S[2:0]	Output	T_{RISE}	T_{FALL}	Min Spec	Units
010	CLK+/-	112.17	108.59	75	ps
	D2+/-	117.90	113.63	75	ps
011	CLK+/-	121.60	118.74	75	ps
	D2+/-	129.60	127.44	75	ps
100	CLK+/-	122.05	120.41	75	ps
	D2+/-	127.14	127.28	75	ps

Table 2: Rise/Fall Times of TMDS at J602 when EQ=3dB and Resolution=1920x1080i

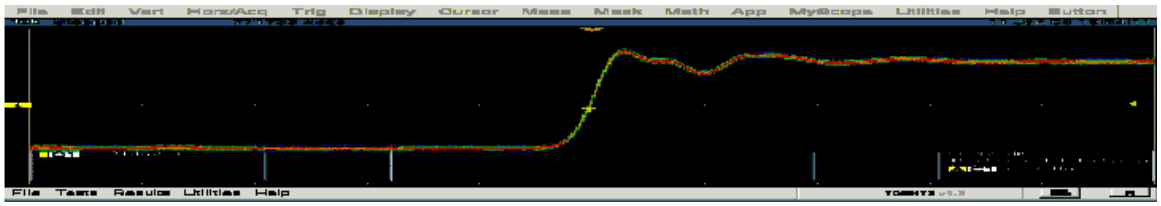


Figure 10a: T_{RISE} of CLK when OC_S[2:0]=010, EQ=3dB and Resolution=1920x1080i

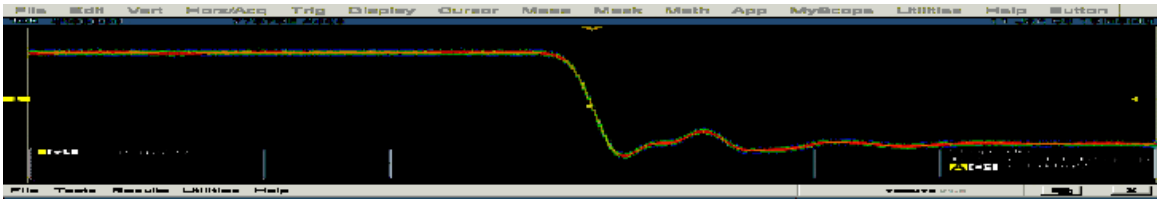


Figure 10b: T_{FALL} of CLK when OC_S[2:0]=010, EQ=3dB and Resolution=1920x1080i

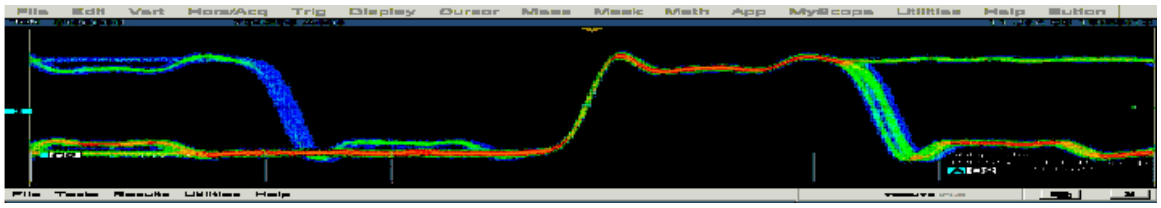


Figure 10c: T_{RISE} of D2 when OC_S[2:0]=010, EQ=3dB and Resolution=1920x1080i

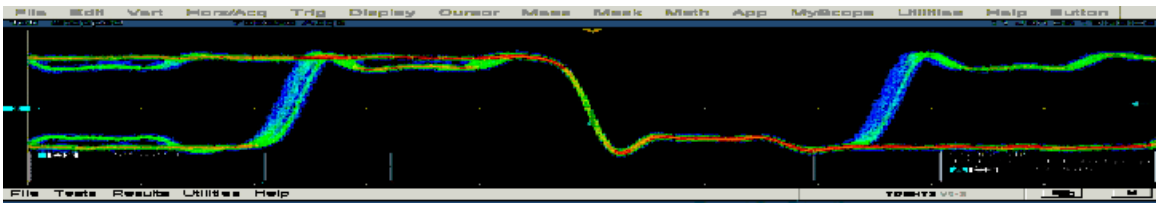


Figure 10d: T_{FALL} of D2 when OC_S[2:0]=010, EQ=3dB and Resolution=1920x1080i

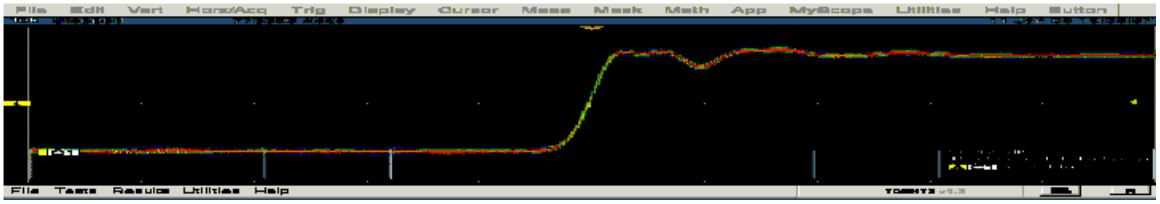


Figure 11a: T_{RISE} of CLK when OC_S[2:0]=011, EQ=3dB and Resolution=1920x1080i

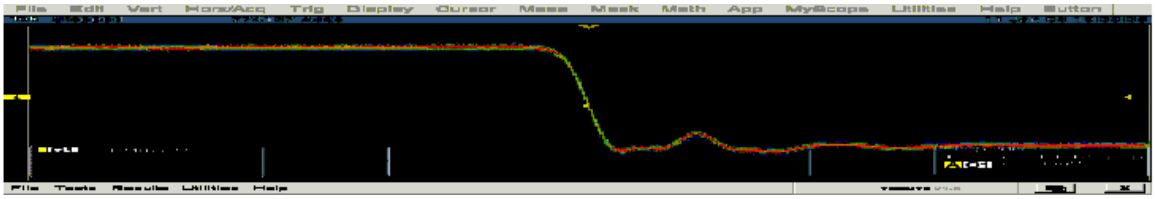


Figure 11b: T_{FALL} of CLK when OC_S[2:0]=011, EQ=3dB and Resolution=1920x1080i

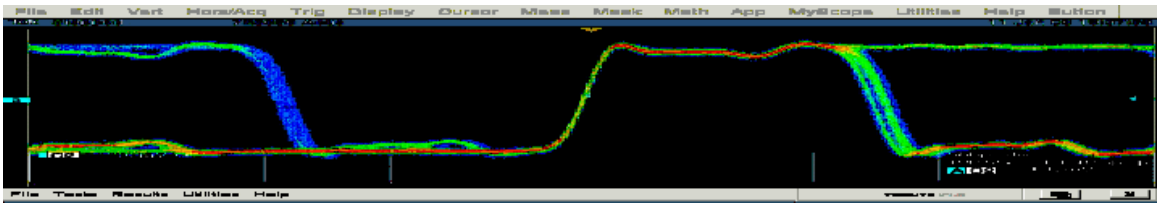


Figure 11c: T_{RISE} of D2 when OC_S[2:0]=011, EQ=3dB and Resolution=1920x1080i

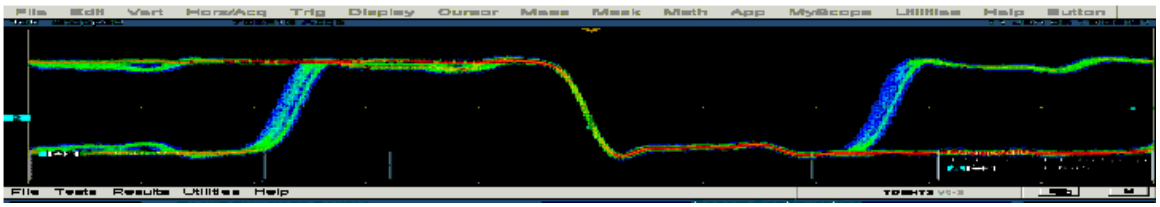


Figure 11d: T_{FALL} of D2 when OC_S[2:0]=011, EQ=3dB and Resolution=1920x1080i

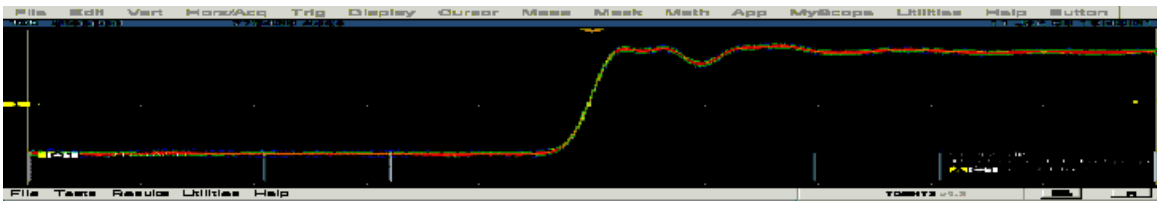


Figure 12a: T_{RISE} of CLK when OC_S[2:0]=100, EQ=3dB and Resolution=1920x1080i

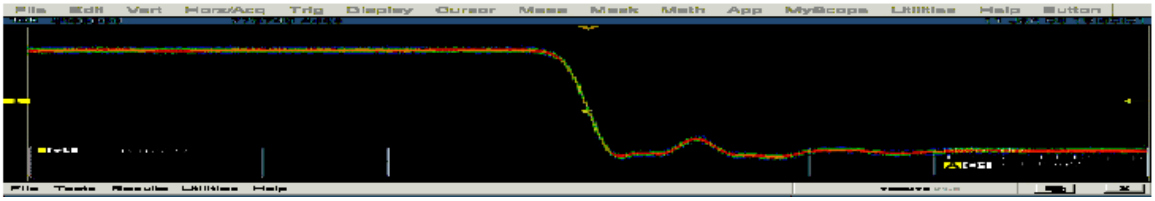


Figure 12b: T_{FALL} of CLK when OC_S[2:0]=100, EQ=3dB and Resolution=1920x1080i

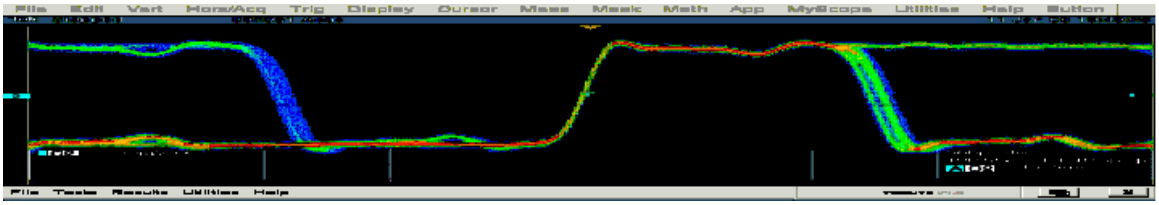


Figure 12c: T_{RISE} of D2 when OC_S[2:0]=100, EQ=3dB and Resolution=1920x1080i

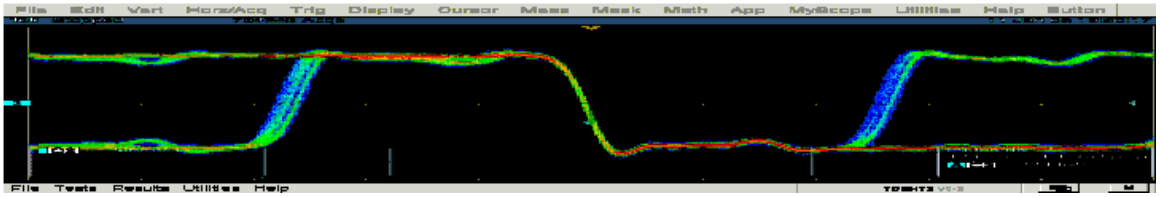


Figure 12d: T_{FALL} of D2 when OC_S[2:0]=100, EQ=3dB and Resolution=1920x1080i

c. Source Test ID 7-8: TMDS – Clock Duty Cycle at 3dB Equalization & 1920x1080i Resolution

Output	Min Duty Cycle	Max Duty Cycle	Min Spec	Max Spec	Units
CLK+/-	49.38	50.49	40	60	%

Table 3: Clock Duty Cycle at J602 when EQ=3dB and Resolution=1920x1080i

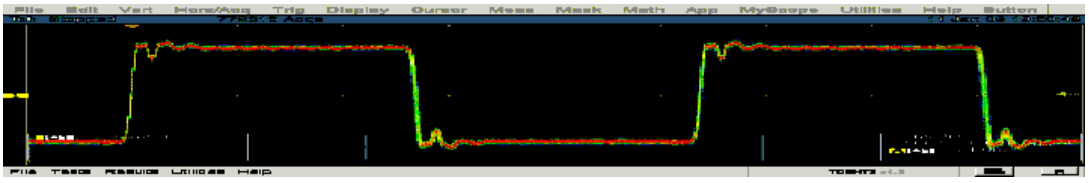


Figure 13a: Max Duty Cycle of CLK when EQ=3dB and Resolution=1920x1080i

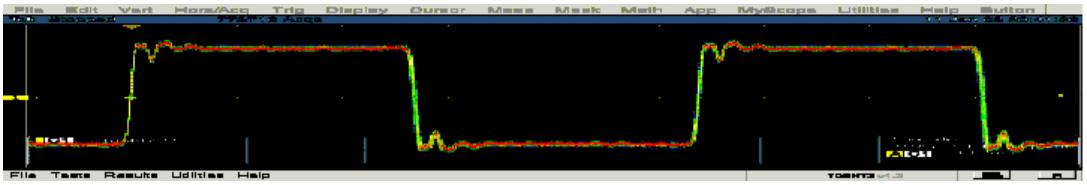


Figure 13b: Min Duty Cycle of CLK when EQ=3dB and Resolution=1920x1080i

d. Source Test ID 7-9: TMDS – Clock Jitter at 3dB Equalization & 1920x1080i Resolution

OC_S[2:0]	Output	Clock Jitter	Max Spec	Units
010	CLK+/-	0.085	0.25	T_{BIT}
011	CLK+/-	0.081	0.25	T_{BIT}
100	CLK+/-	0.081	0.25	T_{BIT}

Table 4: Clock Jitter at J602 when EQ=3dB and Resolution=1920x1080i

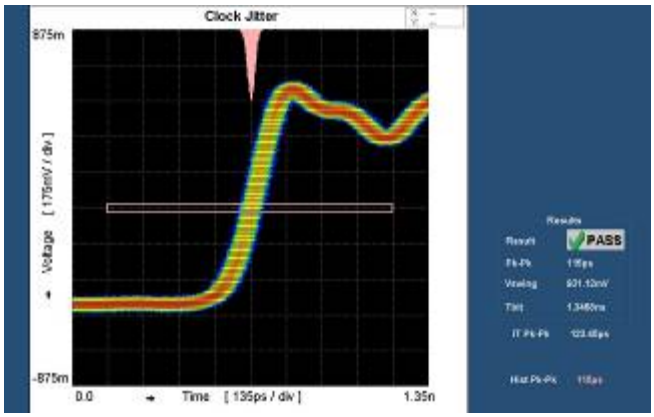


Figure 14: Clock Jitter of CLK when OC_S[2:0]=010

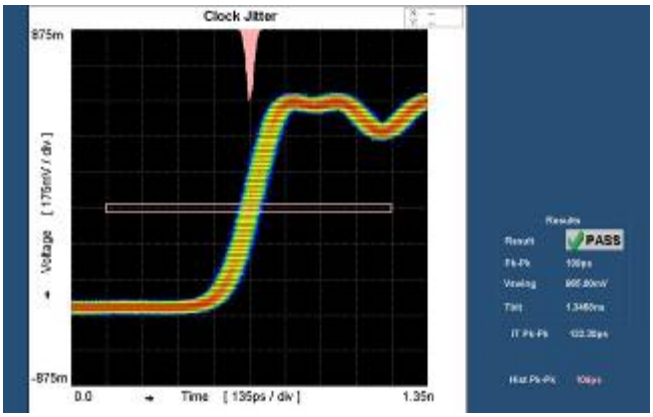


Figure 15: Clock Jitter of CLK when OC_S[2:0]=011

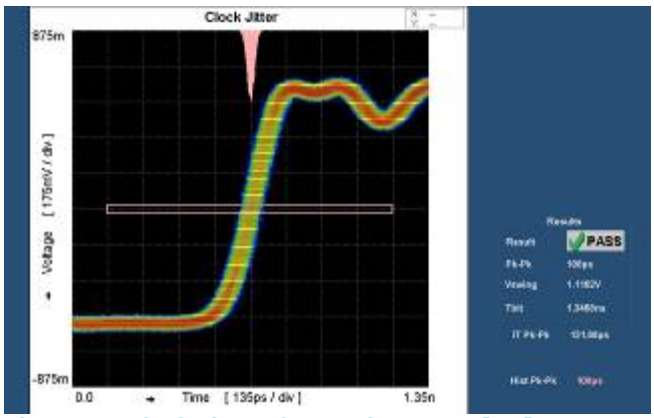


Figure 15: Clock Jitter of CLK when OC_S[2:0]=100

e. Source Test ID 7-10: TMDS – Data Jitter & Eye Diagrams at 3dB Equalization & 1920x1080i Resolution

OC_S[2:0]	Output	Data Jitter	Max Spec	Units
010	D2+/-	0.12	0.3	T_{BIT}
011	D2+/-	0.11	0.3	T_{BIT}
100	D2+/-	0.11	0.3	T_{BIT}

Table 5: Data Jitter at J602 when EQ=3dB and Resolution=1920x1080i

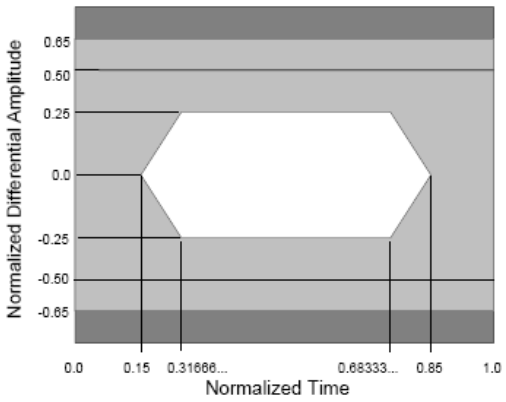


Figure 16: Source Eye Diagram

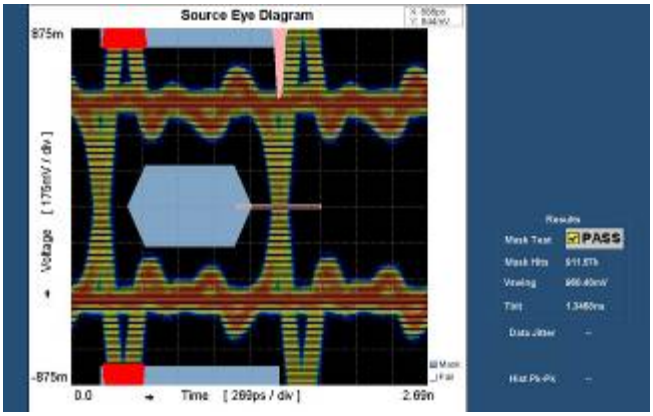


Figure 17: Eye Diagram of D2 when OC_S[2:0]=000

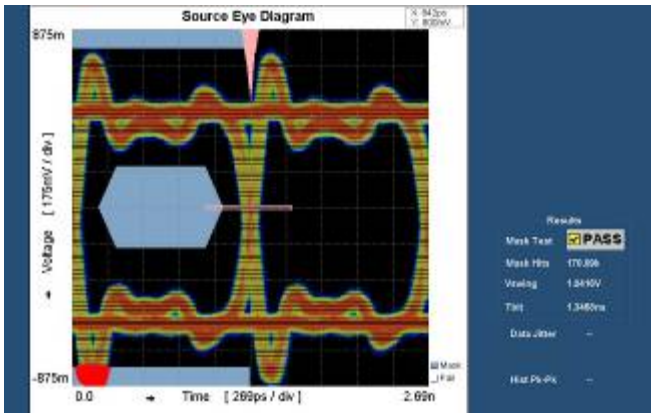


Figure 18: Eye Diagram of D2 when OC_S[2:0]=001

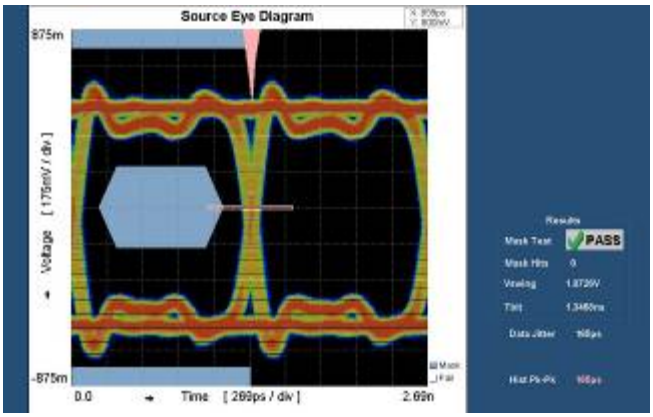


Figure 19: Eye Diagram of D2 when OC_S[2:0]=010

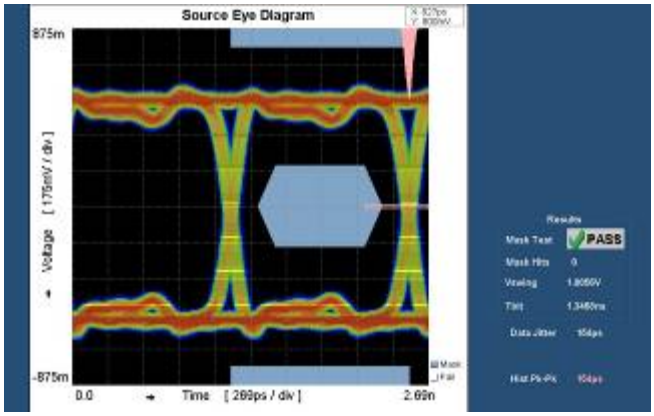


Figure 16: Eye Diagram of D2 when OC_S[2:0]=011

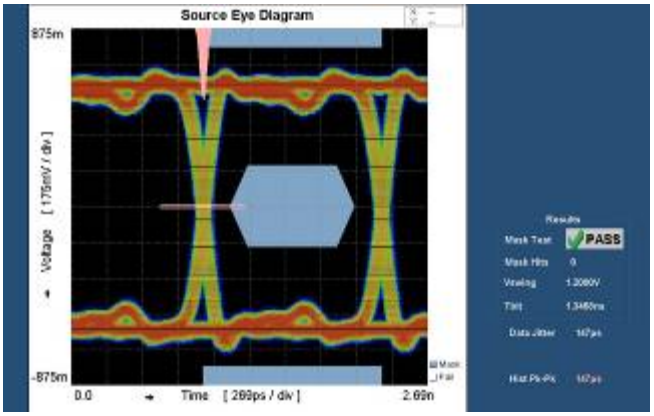


Figure 17: Eye Diagram of D2 when OC_S[2:0]=100

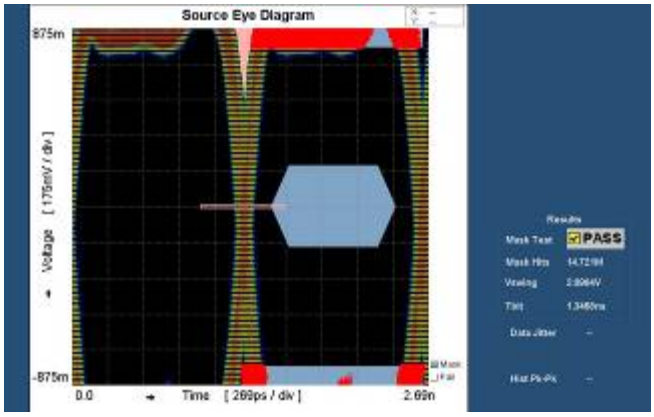


Figure 18: Eye Diagram of D2 when OC_S[2:0]=101

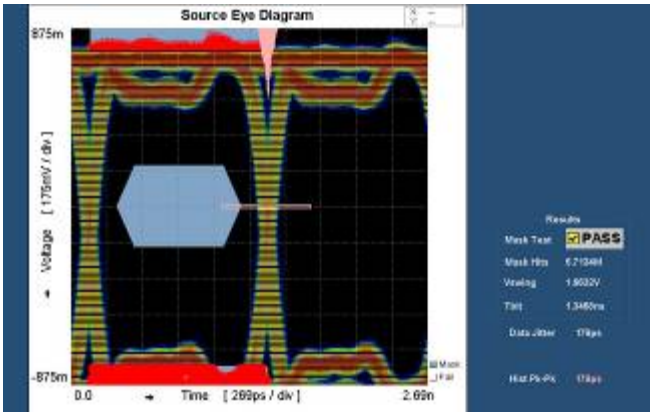


Figure 19: Eye Diagram of D2 when OC_S[2:0]=110

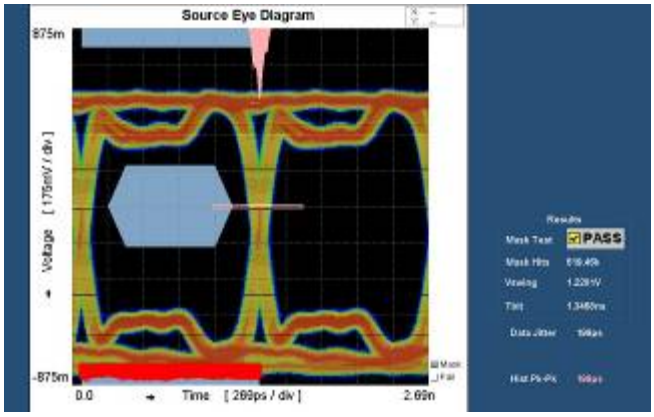


Figure 18: Eye Diagram of D2 when OC_S[2:0]=111

f. Sink Test ID 8-8: TDR Measurement

Differential impedance of PI3HDMI201 on an HDMI-HDMI demo board is measured to confirm the trace impedance is within the requirement described in Test ID 8-8 in HDMI Compliance Test Specification Version 1.3a.

Test ID 8-8: TMDS – Differential Impedance	
Reference	**Requirement**
[HDMI: Table 4-20] HDMI Sink Impedance at TP2	Through-connection impedance : 100Ω ± 15%* ** A single excursion is permitted out to a max/min of 100 ohms ±25% and of a duration less than 250psecs.* At Termination impedance (when Vicm is within Vicm1 range) 100 ohms ±10%

Table 6: HDMI Pre-test Test ID 8-8 Specification

CDF field Sink_Diff_PowerOn = Y for each signal input. The terminations of each clock and data are switched from 50Ω to 250kΩ pull-up when PI3HDMI201 is not powered up. Thus, at-termination impedance cannot be obtained without powering up PI3HDMI201.

Through impedance is measured at input side of the demo board. Filter of 180ps is employed throughout the following measurement.

For Port A,
- Sink_Term_Distance at D2 = 0.56ns
- Sink_Term_Distance at D1 = 0.54ns
- Sink_Term_Distance at D0 = 0.56ns
- Sink_Term_Distance at CLK = 0.56ns

For Port B,
- Sink_Term_Distance at D2 = 0.58ns
- Sink_Term_Distance at D1 = 0.56ns
- Sink_Term_Distance at D0 = 0.58ns
- Sink_Term_Distance at CLK = 0.58ns

Through Impedance		D2	D1	D0	CLK	Spec		Units
						Min	Max	
Port A	**Min**	97	94	94	94	85	115	Ω
	Max	107	103	103	103	85	115	Ω
Port B	**Min**	96	94	94	95	85	115	Ω
	Max	109	105	106	109	85	115	Ω

Table 7: Through Impedance Result

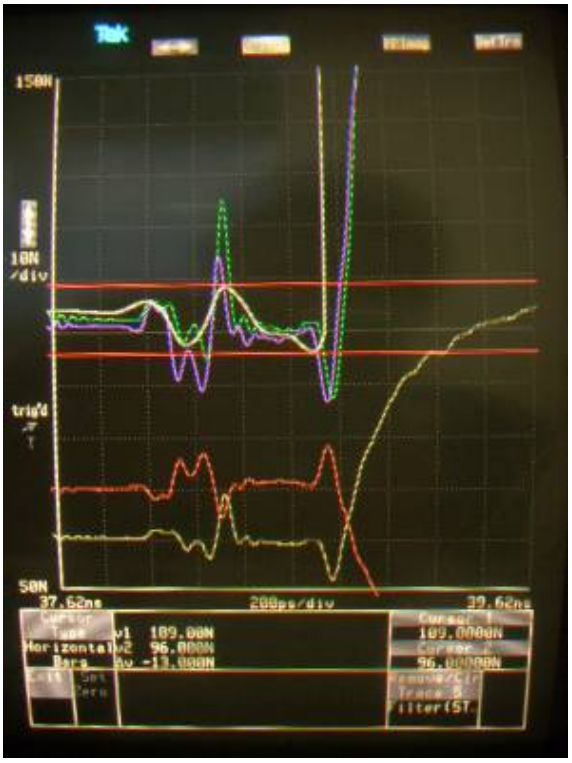


Figure 20a: TDR at D2 at Port A

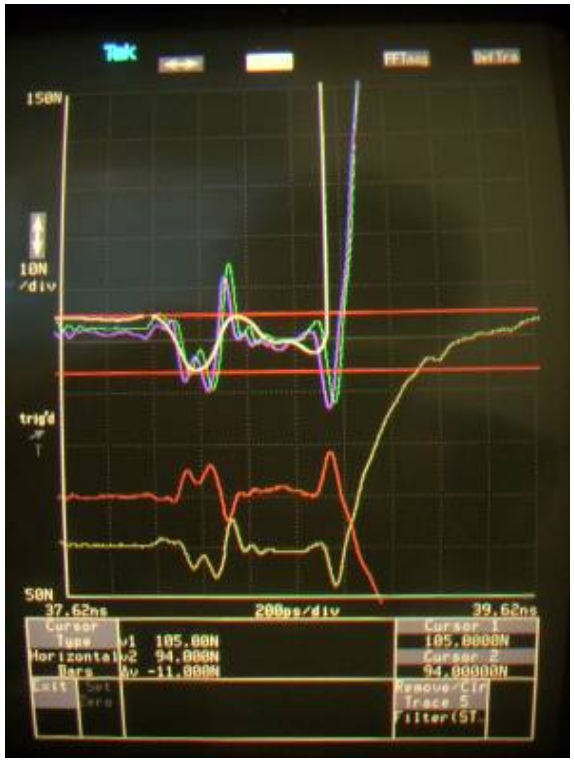


Figure 20b: TDR at D1 Port A

Figure 20c: TDR at D0 Port A

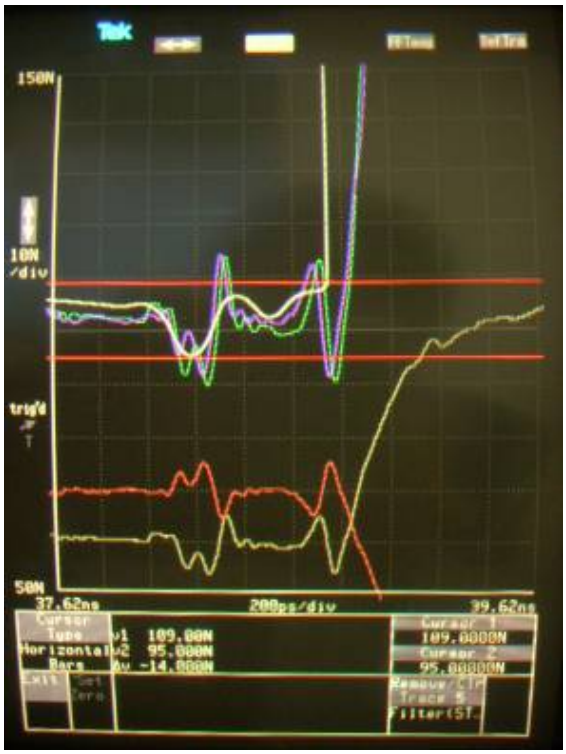


Figure 20d: TDR at CLK Port A

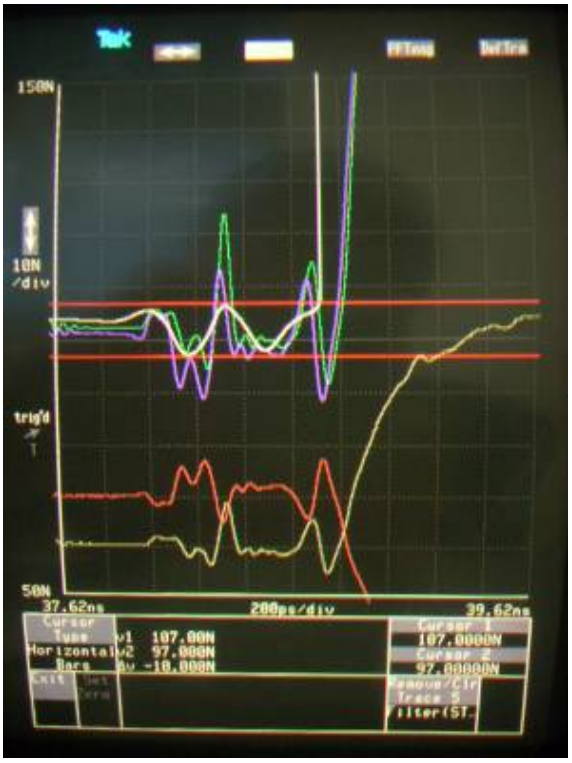


Figure 21a: TDR at D2 at Port B

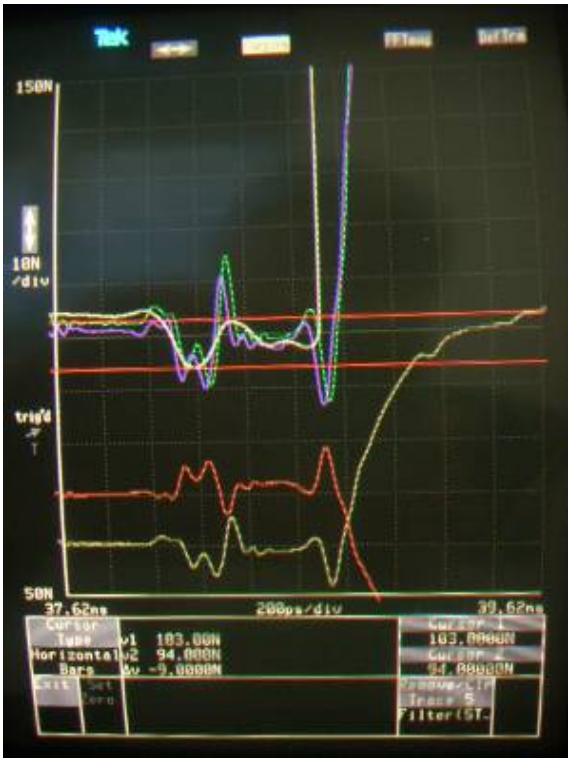


Figure 21b: TDR at D1 Port B

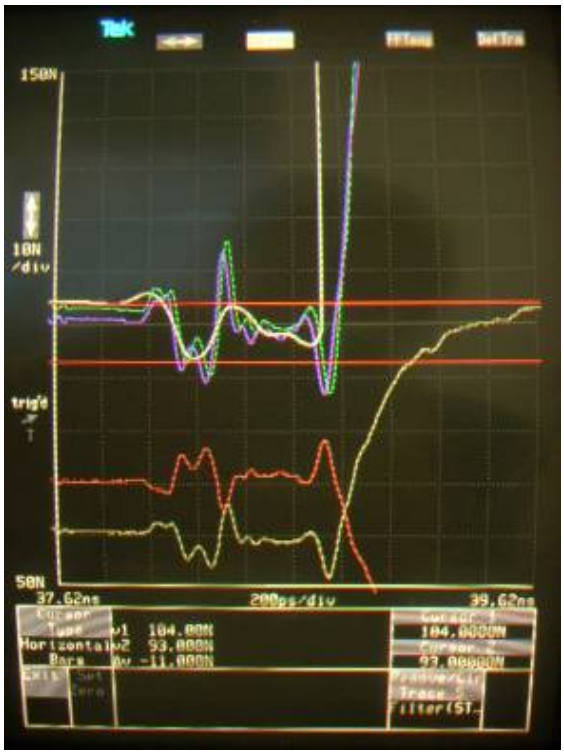


Figure 21c: TDR at D0 Port B

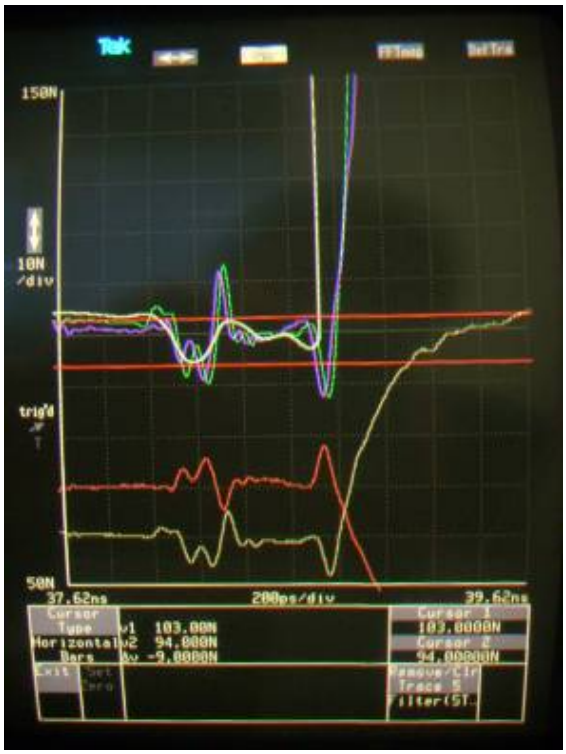


Figure 21d: TDR at CLK Port B

g. Sink Test ID 8-4: TMDS – Termination Voltage when Sink is powered up

Output	Vterm	Spec		Units
		Min	Max	
D2+	3.31	3.125	3.475	V
D2-	3.31	3.125	3.475	V
D1+	3.31	3.125	3.475	V
D1-	3.31	3.125	3.475	V
D0+	3.31	3.125	3.475	V
D0-	3.31	3.125	3.475	V
CLK+	3.31	3.125	3.475	V
CLK-	3.31	3.125	3.475	V

Table 8: Termination Voltage at Connector J603

h. Sink Test ID 8-9: DDC/CEC Line Capacitance Measurement

The capacitances of SDA and SCL signals which go through EEPROM AT24C02B are tested. The capacitance of CEC line connecting input to output HDMI is also measured. Results below show that the capacitances are within HDMI CTS V1.3a requirement.

C_{DUT} = C2 – C1

Setting of Impedance Analyzer for measuring capacitance:

For SDA/SCL, Freq=100kHz, DC Bias=2.5V, Power=15dBm (AC~1.8Vpp at DUT), IF BW=1kHz, Sweep Time=1s

For CEC, Freq=100kHz, DC Bias=1.65V, Power=15dBm (AC~1.8Vpp at DUT), IF BW=1kHz, Sweep Time=1s

Pin	Parameter	DUT Power		Spec		Units
		Off	On	Min	Max	
SDA	C1	6.9	6.9	NA	NA	pF
	C2	19.2	22.1	NA	NA	pF
	C_{DUT}	12.3	15.2		50	pF
SCL	C1	6.9	6.9	NA	NA	pF
	C2	17.9	20.9	NA	NA	pF
	C_{DUT}	11.0	14.0		50	pF
CEC	C1	7.0	7.0	NA	NA	pF
	C2	23.9	23.9	NA	NA	pF
	C_{DUT}	16.9	16.9		200	pF

Table 9: DDC/CEC Line Capacitance Result at Connector J603

i. Sink Test ID 8-12: +5V Power Max Current

Current consumption is measured when voltage is supplied to +5V pin at input HDMI connector to ensure that PI3HDMI201 does not draw more than 50mA when employing to Sink application.

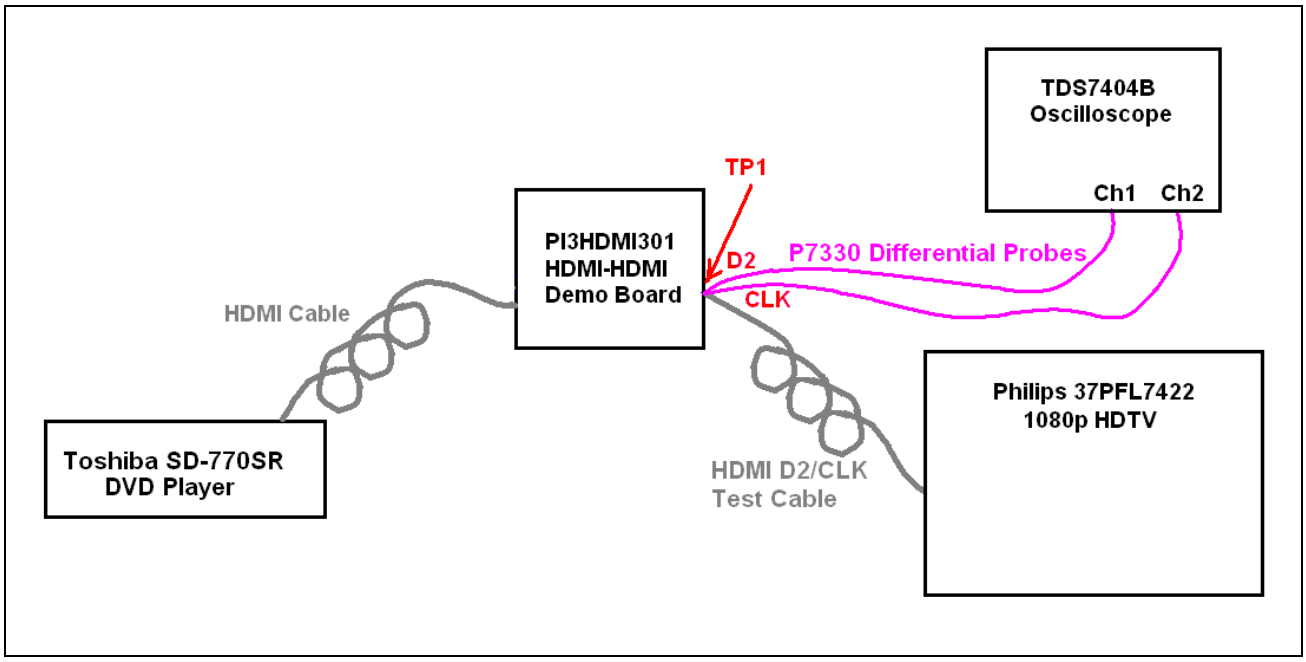
Test Condition	P_5V		Max Spec	Units
	4.9V	5.1V		
DUT Power On	4.85	5.05	10	mA
DUT Power Off / Disconnected from AC Power	0	0	50	mA

Table 10: +5V Power Max Current at Connector J603

Appendix A: Test Setup

Test setup:

a. For Source Test

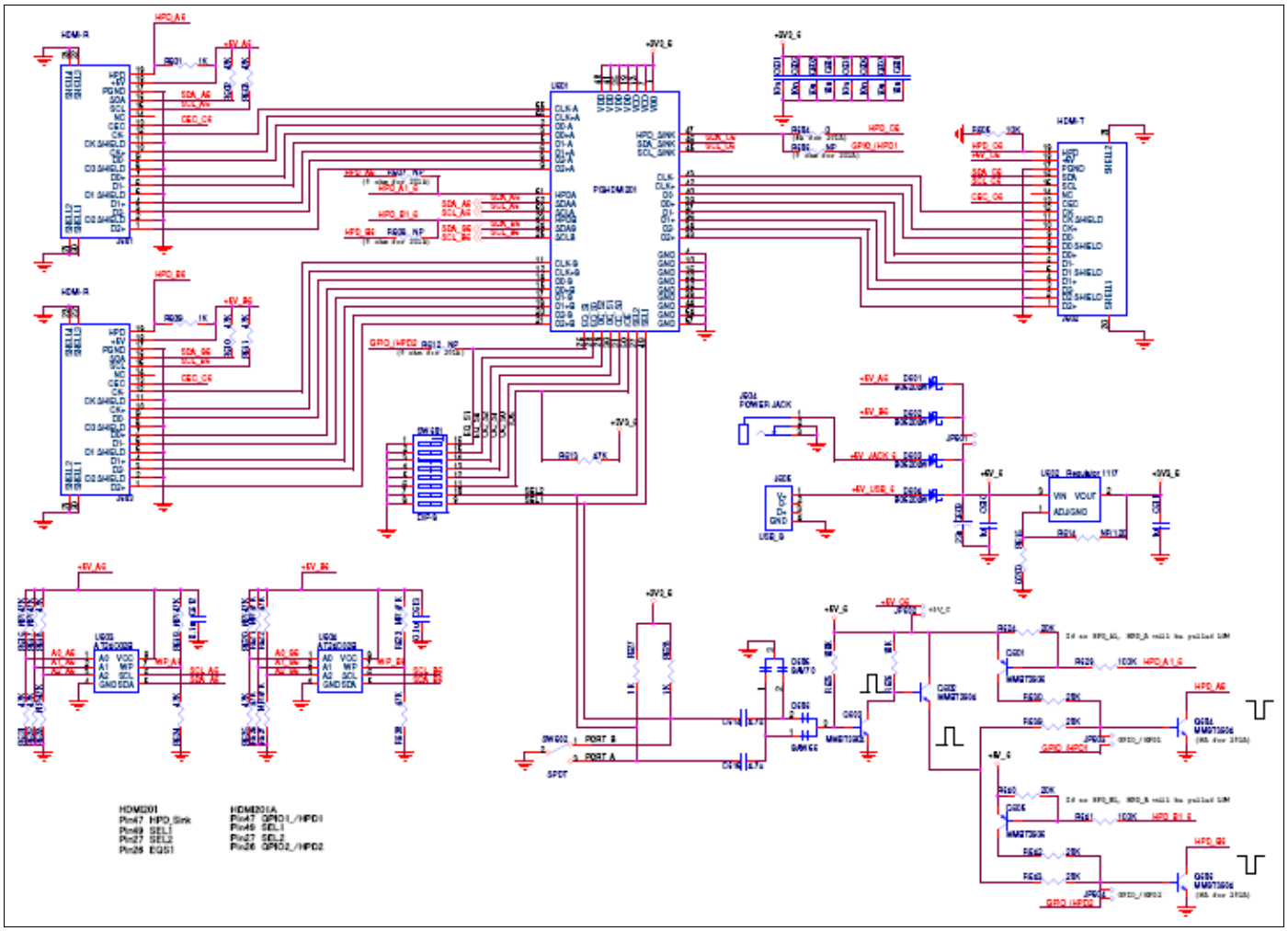


Equipment Use:

a. For Source Test
- TDS7404B Oscilloscope with P7330 Differential Probes
- 1-meter HDMI Cable
- 1-meter HDMI D2/CLK Test Cable
- Toshiba SD-770SR DVD Player
- Philips 37PFL7422 HDTV
- Agilent Power Supply

b. For Sink Test
- Tek11801C Digital Sampling Oscilloscope
- Agilent 4395A Impedance Analyzer with 43961A and 16092A
- SMA Matching Cables
- PSC High BW TDR Test Fixture
- PSC High BW Cap Test Fixture
- Agilent Power Supply

Appendix B: PCB Schematic



Appendix C: PCB Layout Requirements

a. Stack Up:

Plane	Material	Thickness (mil)
Signal		1.9
Prepreg	1080 + 2116	7.3
Ground		1.2
Core		44
Power		1.2
Prepreg	1080 + 2116	7.3
Signal		1.9

b. Isolation Spacing = 30 mil

c. Width & Spacing (W/S) of 100Ω Differential Trace = 9.0 / 10 mil
* W/S for 80 mils before and after contacting the TMDS input/output pads of PI3HDMI201 = 5.0 / 15 mil to compensate the impedance drop of PI3HDMI201 solder pads

Appendix D: BOM List

Item	Quantity	Reference	Description
1	2	C612, C613	0.1uF Capacitor
2	1	C609	22uF Capacitor
3	2	C610, C611	1uF Capacitor
4	8	C601, C602, C603, C604, C605, C606, C607, C608	10nF Capacitor
5	2	C615, C614	4.7uF Capacitor
6	4	D601, D602, D603, D604	B0520LW Schottky Rectifier
7	1	D605	BAV70 Common Cathode Double Diode
8	1	D606	BAW56 Common Anode Double Diode
9	4	JP601, JP602, JP603, JP604	2-pin Header
10	2	J601,J603	HDMI Receptacle Connector
11	1	J602	HDMI Plug Connector
12	1	J604	Power Jack
13	1	J605	USB Type B Connector
14	2	Q601, Q605	MMBT3906 PNP Transistor
15	4	Q602, Q603, Q604, Q606	MMBT3904 NPN Transistor
16	13	R602, R603, R610, R611, R613, R618, R622, R631, R632, R634, R635, R636, R638	47kΩ Resistor
17	2	R605, R626	10kΩ Resistor
18	4	R601, R609, R627, R628	1kΩ Resistor
19	2	R604, R615	0Ω Resistor
20	6	R624, R630, R639, R640, R642, R643	20kΩ Resistor
21	3	R625, R629, R641	100kΩ Resistor
22	13	R606, R607, R608, R612, R614, R616, R617, R619, R620, R621, R623, R633, R637	NOT CONNECTED
23	1	SW601	DIP-8 Switch
24	1	SW602	SPDT Switch
25	1	U601	PI3HDMI201 HDMI Switch
26	1	U602	1117 Regulator
27	2	U603, U604	AT24C02B EEPROM