PI3HDMI101
PI3HDMI101 HDMI-HDMI Demo Board Rev.B User Manual

by Ada Yip

Introduction

This user manual describes the components and the usage of PI3HDMI101 HDMI-HDMI Demo Board Rev.B. HDMI connectors are used as input and output connectors for the following HDMI-HDMI demo board version.

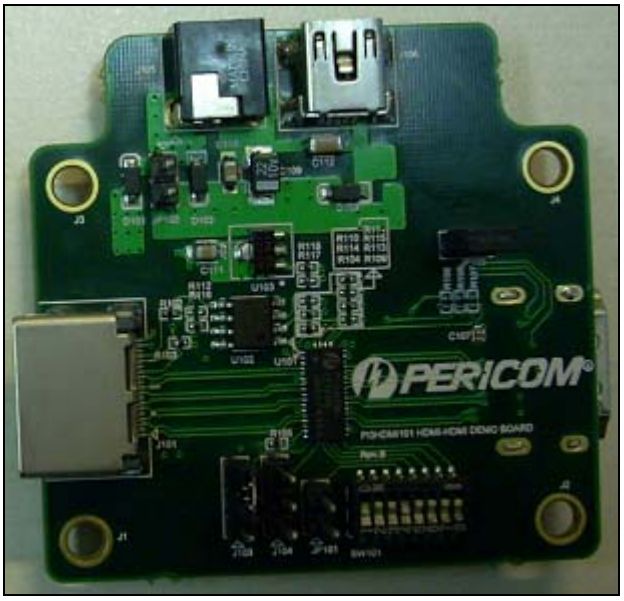


Figure 1a: Top View of PI3HDMI101 HDMI-HDMI Demo Board Rev.B

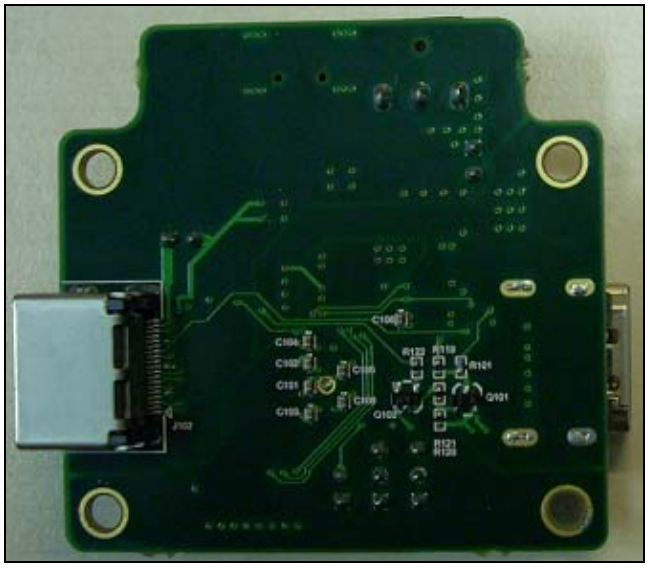


Figure 1b: Bottom View of PI3HDMI101 HDMI-HDMI Demo Board Rev.B

Key Components / Circuits

a. 5V of PI3HDMI101 demo board can be supplied via three ways, i.e. using 5V supplied from Input Port, Power Jack, or from USB Type B Connector. Jumpers on demo boards are not connected at default. If using voltage of input port to power up the entire board, jumper must be added at JP102. JP103 is shorted so as to supply 5V to +5V pin at the output HDMI connector J102.

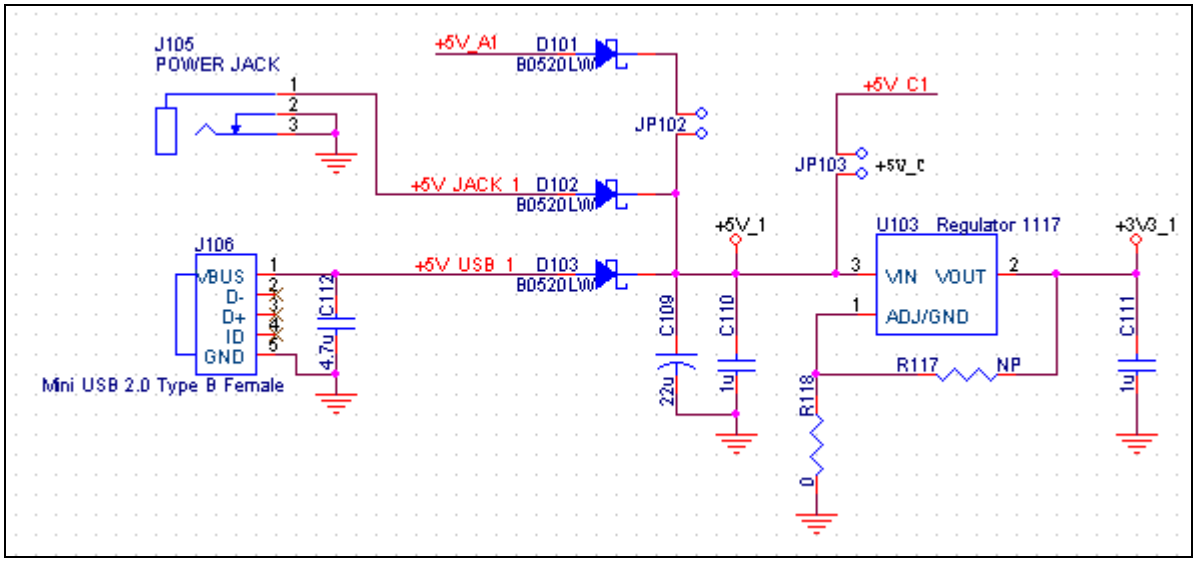


Figure 2: Schematic of 5V Power Supply of PI3HDMI101 HDMI-HDMI Demo Board Rev.B

b. Assuming that a Source is connected to HDMI connector J101, after a Sink is attached to HDMI connector J102, Sink will signal the source it is connected by pulling HPD_C1 signal (HPD pin of J102) to high level. HPD_A1 signal (HPD pin of J101) will be pulled up by +5V supplied by Source in the circuit shown below.

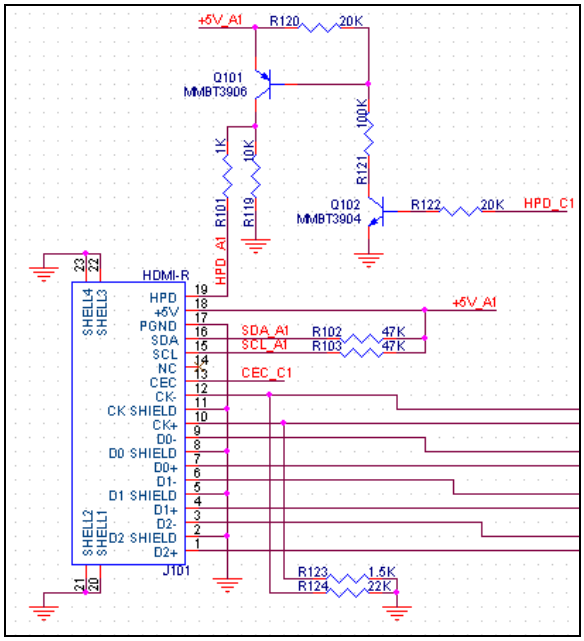


Figure 3: Schematic of Sink HPD of PI3HDMI101 HDMI-HDMI Demo Board Rev.B

c. One AT24C02B EEPROM is implemented in PI3HDMI101 demo board to model I2C application. The EEPROM is for DDC line capacitance measurement purpose. Please refer to p.16 for measurement result. A0 and A1 address inputs of AT24C02B are pulled to low by external pull-down resistors while address A2 is pulled high. Write protection of the EEPROM is disabled.

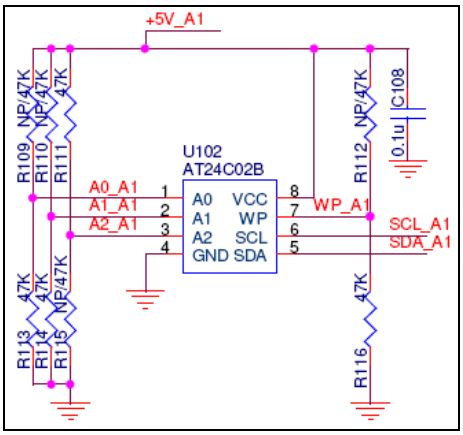


Figure 4: Schematic of EEPROM of PI3HDMI101 HDMI-HDMI Demo Board Rev.B

d. Enable, /OE, pin is used to enable TMDS outputs. As this pin is enable low, jumper J104 in the schematic below is tied to low to enable outputs.

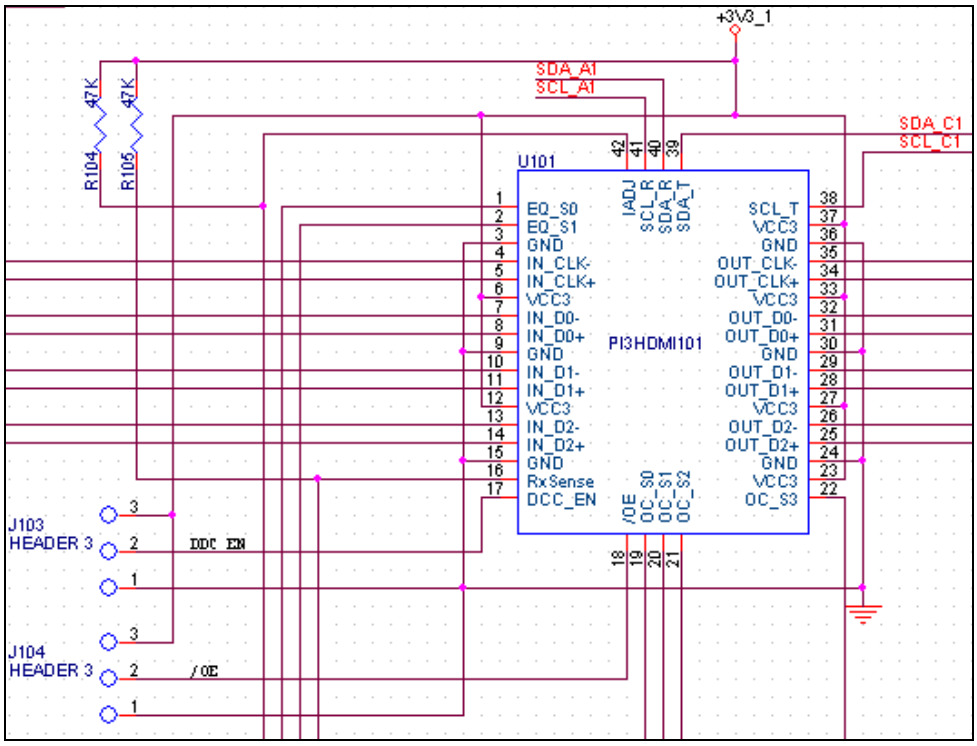


Figure 5: Enabling Circuit of PI3HDMI101 HDMI-HDMI Demo Board Rev.B

e. To enable I2C path, DDC_EN pin 17 is tied to high. As shown in the schematic above, DDC_EN can be shorted to +3V3_1 using jumper J103.

f. RxSense support is implemented in clock channels of PI3HDMI101.

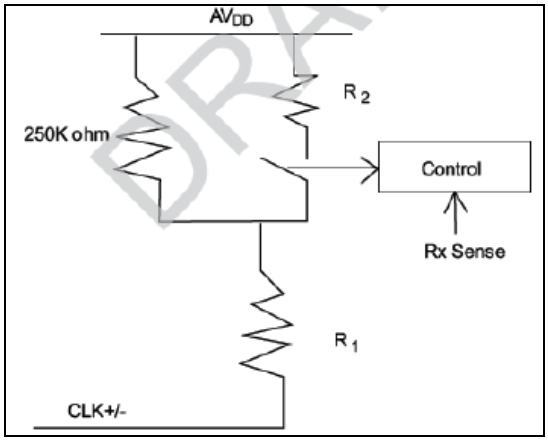


Figure 6: RxSense Scheme of PI3HDMI101

When RxSense is tied to low, the R2 switch above is open, clock channels are then terminated by 250kΩ. On the contrary, when RxSense is tied to high, R2 switch is closed to change clock termination to 50Ω. This feature can be controlled using RxSense pin 16 on PI3HDMI101. On HDMI-HDMI demo board, RxSense pin is pulled high by a resistor R105 at default. Switch SW101 can be used to pull RxSense to low.

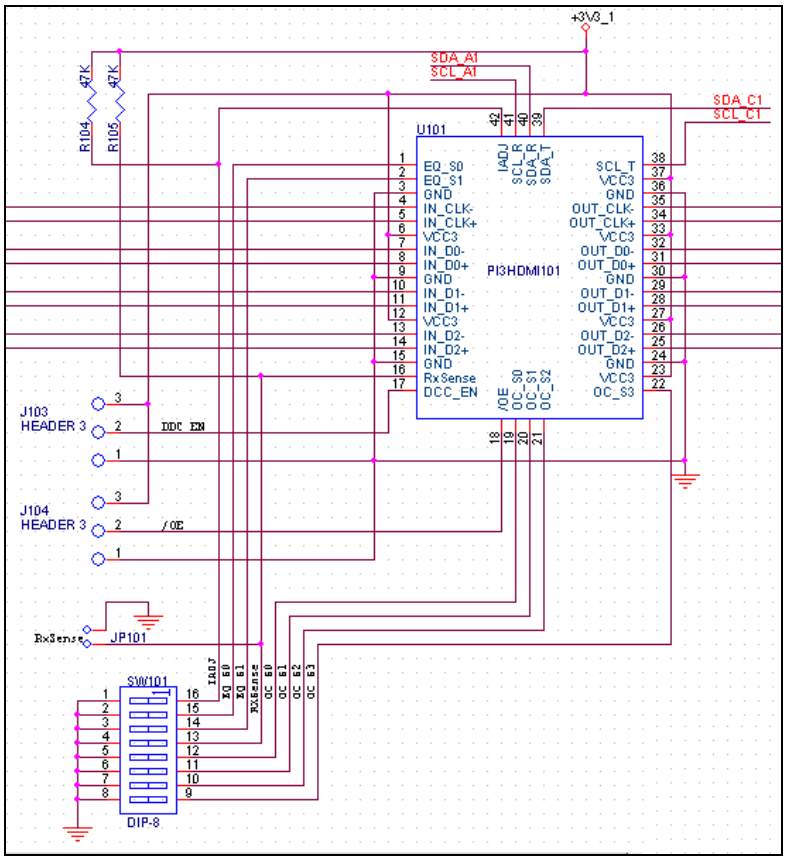


Figure 7: Schematic of RxSense/IADJ of PI3HDMI101 HDMI-HDMI Demo Board Rev.B

g. Voltage selection using IADJ pin 42 for I2C buffer of PI3HDMI101 is chosen according to I2C external pull-up range at output connector J102. IADJ is set to high via a resistor R104 at default in the schematic above. Switch SW101 is used to change IADJ to low. IADJ should be set to high if external pull-up at output connector ranges from 1kΩ to 2kΩ or low if external pull-up is larger than 3kΩ. 2kΩ pull-ups are employed at R107 and 108 on PI3HDMI101 HDMI-HDMI demo board as shown below.

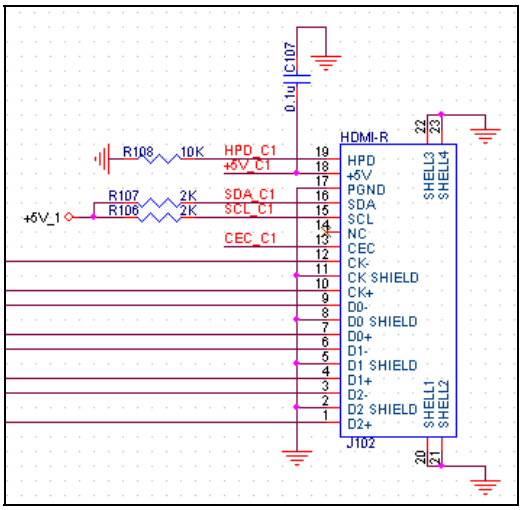


Figure 8: I2C External Pull-up of PI3HDMI101 HDMI-HDMI Demo Board Rev.B

h. When source chipset does not generate CLK signal, noise may pass through an active PI3HDMI101 to cause output oscillation. To implement fail-safe feature to prevent from output oscillation, the input CLK is recommended to be biased externally. 100mV DC bias can be added to CLK+ by adding a 1.5kΩ pull-down resistor. To maintain trace impedance consistency, it is recommended to avoid stub between pull-down resistor pad and CLK signal trace on PCB layout.

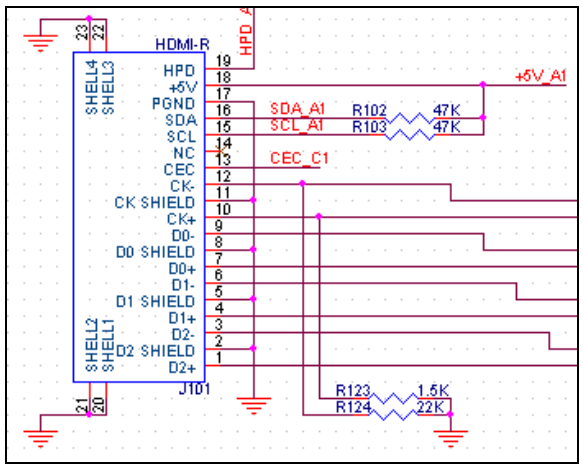


Figure 9: Input CLK External Pull-down of PI3HDMI101 HDMI-HDMI Demo Board Rev.B

In some DVD players, no sink current circuitry is implemented in TMDS. When these DVD players are de-selected, CLK signals stay at high level. To ensure the DVD players can enter idle mode when being de-selected, input CLK+/- pins are pulled down externally. By keeping 1.5kΩ pull-down resistor at CLK+ unchanged, another 22kΩ resistor is added to CLK- to pull CLK to low level when there is no 50Ω termination. HDCP can then be reset by RxSense when the port is being selected back.

Test Results

Few Source and Sink pre-test items are performed on PI3HDMI101 Demo Board Rev.A below. Source pre-test results with three output settings of swing and pre-/de-emphasis are tabulated. These three settings can generate passing eye diagrams with 1-meter cables connecting to both input and output connectors. All the eye diagrams of 15 different output settings are attached in section (d) below for reference.

a. Source Test ID 7-4: TMDS – Rise Time or Fall Time at 3dB Equalization & 1920x1080i Resolution

OC_S[3:0]	Output	T_{RISE}	T_{FALL}	Min Spec	Units
0000	CLK+/-	114.39	115.97	75	ps
	D2+/-	115.60	117.05	75	ps
0001	CLK+/-	112.10	114.09	75	ps
	D2+/-	122.73	151.04	75	ps
0101	CLK+/-	104.83	106.47	75	ps
	D2+/-	108.62	107.69	75	ps

Table 1: Rise/Fall Times of TMDS at J102 when EQ=3dB and Resolution=1920x1080i

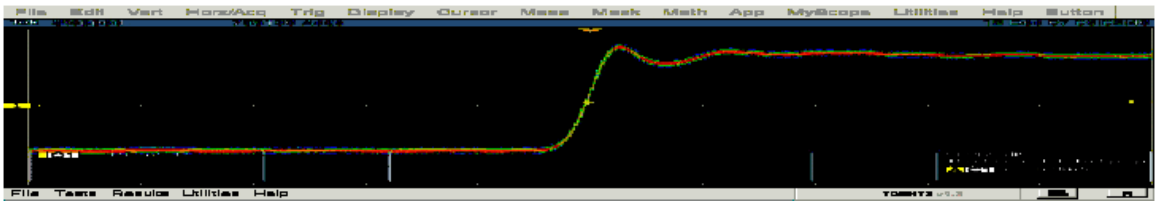


Figure 10a: T_{RISE} of CLK when OC_S[3:0]=0000, EQ=3dB and Resolution=1920x1080i

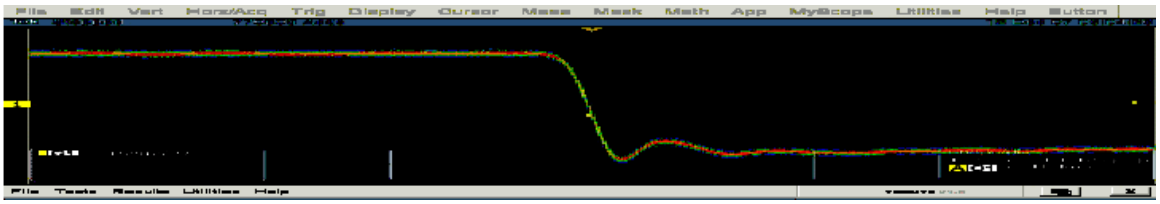


Figure 10b: T_{FALL} of CLK when OC_S[3:0]=0000, EQ=3dB and Resolution=1920x1080i

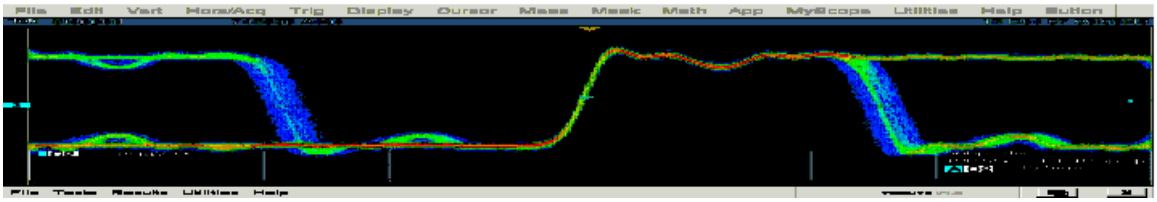


Figure 10c: T_{RISE} of D2 when OC_S[3:0]=0000, EQ=3dB and Resolution=1920x1080i

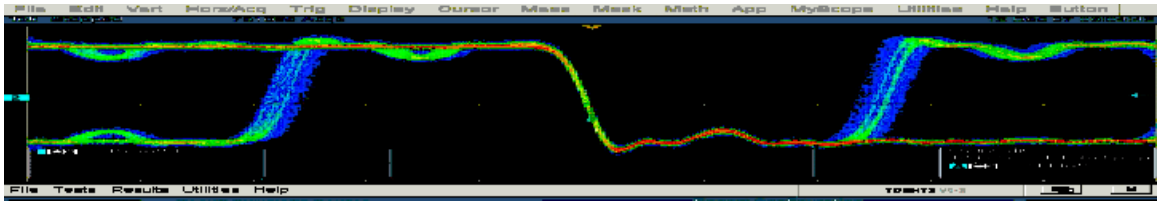


Figure 10d: T_{FALL} of D2 when OC_S[3:0]=0000, EQ=3dB and Resolution=1920x1080i

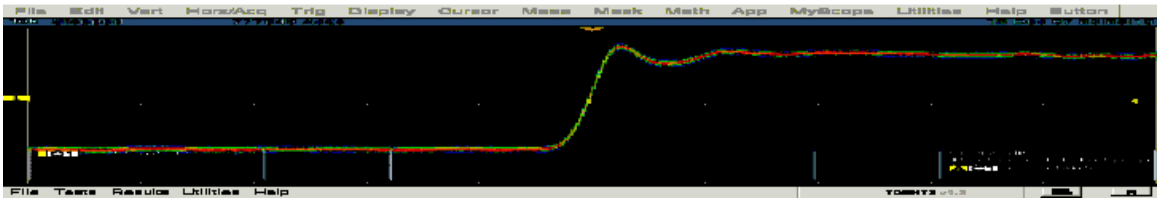


Figure 11a: T_{RISE} of CLK when OC_S[3:0]=0001, EQ=3dB and Resolution=1920x1080i

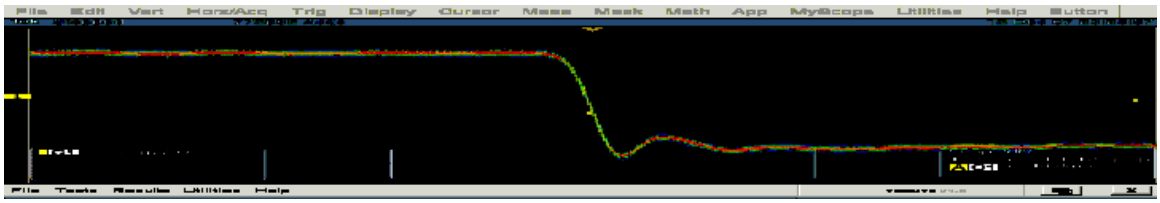


Figure 11b: T_{FALL} of CLK when OC_S[3:0]=0001, EQ=3dB and Resolution=1920x1080i

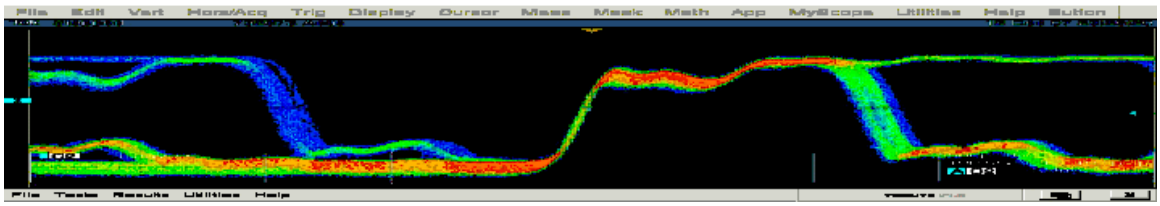


Figure 11c: T_{RISE} of D2 when OC_S[3:0]=0001, EQ=3dB and Resolution=1920x1080i

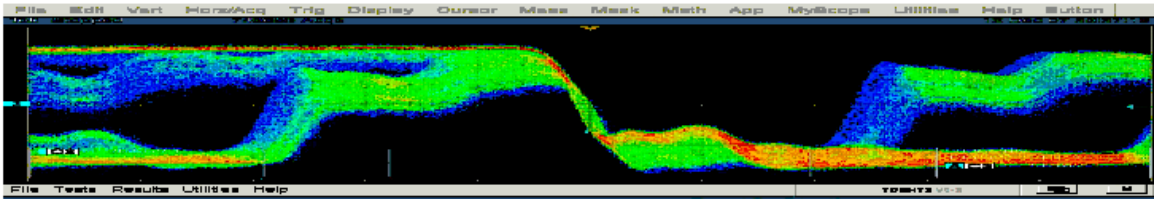


Figure 11d: T_{FALL} of D2 when OC_S[3:0]=0001, EQ=3dB and Resolution=1920x1080i

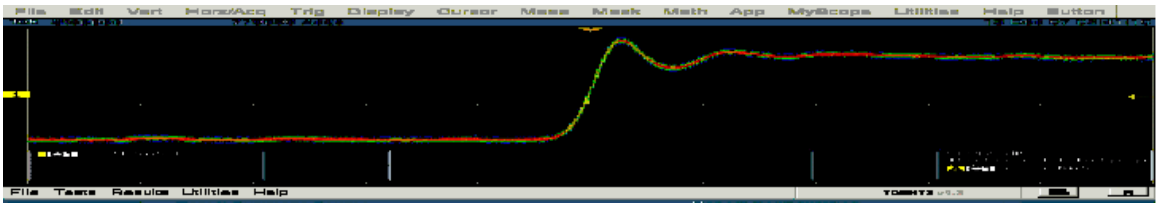


Figure 12a: T_{RISE} of CLK when OC_S[3:0]=0101, EQ=3dB and Resolution=1920x1080i

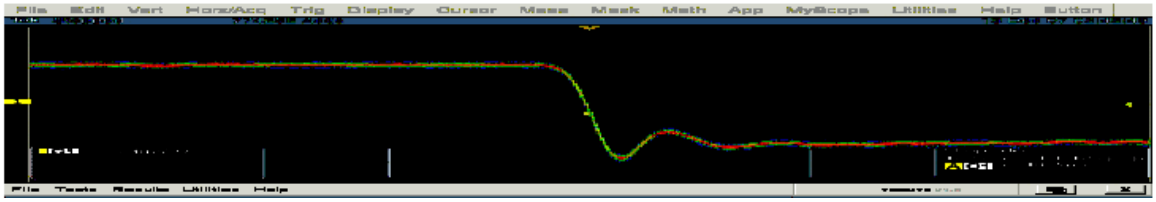


Figure 12b: T_{FALL} of CLK when OC_S[3:0]=0101, EQ=3dB and Resolution=1920x1080i

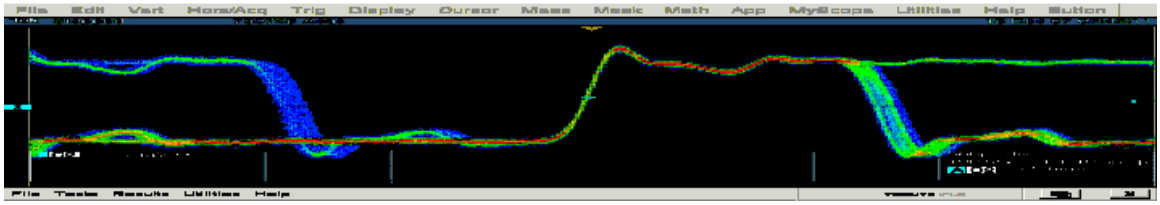


Figure 12c: T_{RISE} of D2 when OC_S[3:0]=0101, EQ=3dB and Resolution=1920x1080i

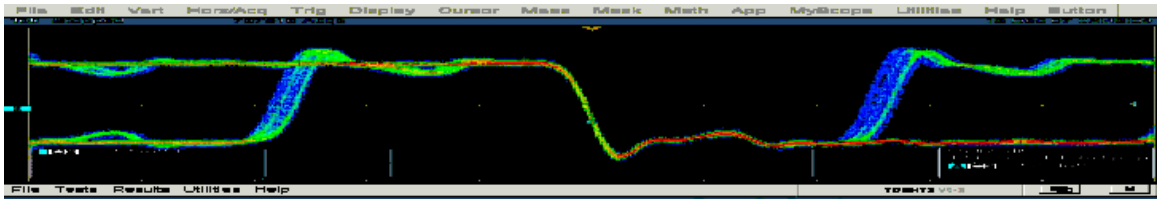


Figure 12d: T_{FALL} of D2 when OC_S[3:0]=0101, EQ=3dB and Resolution=1920x1080i

b. Source Test ID 7-8: TMDS – Clock Duty Cycle at 3dB Equalization & 1920x1080i Resolution

Output	Min Duty Cycle	Max Duty Cycle	Min Spec	Max Spec	Units
CLK+/-	49.38	50.49	40	60	%

Table 2: Clock Duty Cycle at J102 when EQ=3dB and Resolution=1920x1080i

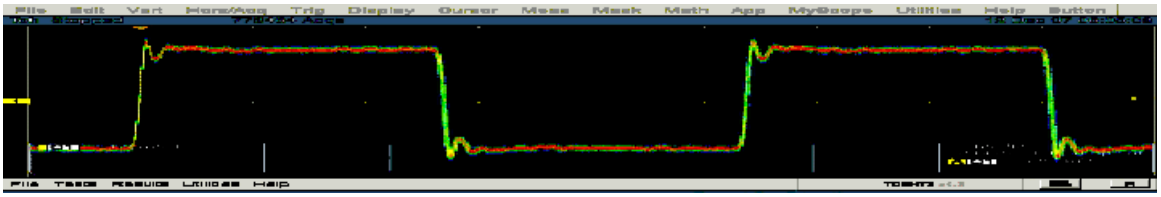


Figure 13a: Max Duty Cycle of CLK when OC_S[3:0]=0000, EQ=3dB and Resolution=1920x1080i

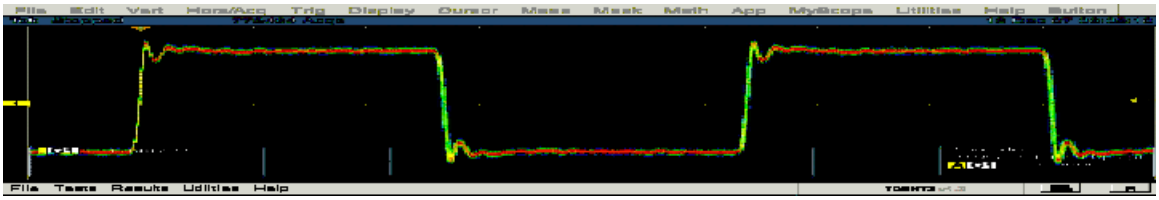


Figure 13b: Min Duty Cycle of CLK when OC_S[3:0]=0000, EQ=3dB and Resolution=1920x1080i

c. Source Test ID 7-9: TMDS – Clock Jitter at 3dB Equalization & 1920x1080i Resolution

OC_S[3:0]	Output	Clock Jitter	Max Spec	Units
0000	CLK+/-	0.105	0.25	T_{BIT}
0001	CLK+/-	0.083	0.25	T_{BIT}
0101	CLK+/-	0.081	0.25	T_{BIT}

Table 3: Clock Jitter at J102 when EQ=3dB and Resolution=1920x1080i

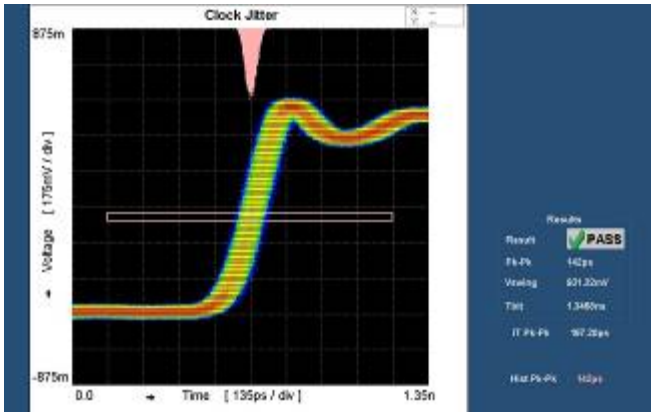


Figure 14: Clock Jitter of CLK when OC_S[3:0]=0000

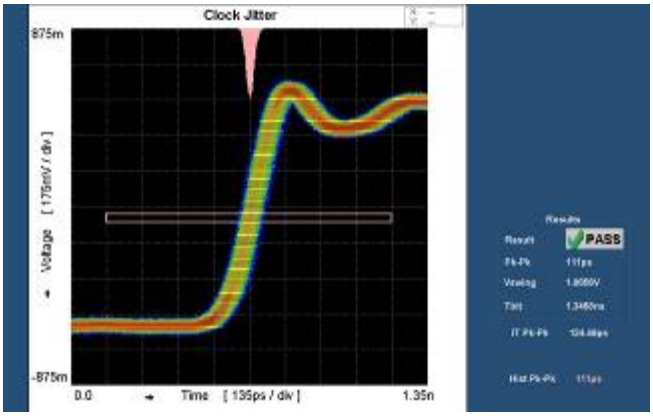


Figure 15: Clock Jitter of CLK when OC_S[3:0]=0001

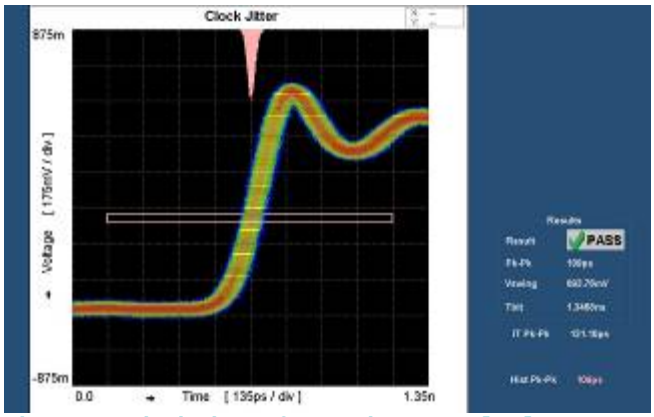


Figure 16: Clock Jitter of CLK when OC_S[3:0]=0101

d. Source Test ID 7-10: TMDS – Data Jitter & Eye Diagrams at 3dB Equalization & 1920x1080i Resolution

OC_S[3:0]	Output	Data Jitter	Max Spec	Units
0000	D2+/-	0.13	0.3	T_{BIT}
0001	D2+/-	0.13	0.3	T_{BIT}
0101	D2+/-	0.16	0.3	T_{BIT}

Table 4: Data Jitter at J102 when EQ=3dB and Resolution=1920x1080i

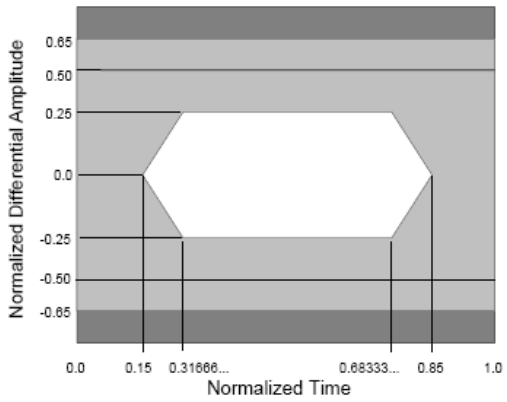


Figure 17: Source Eye Diagram

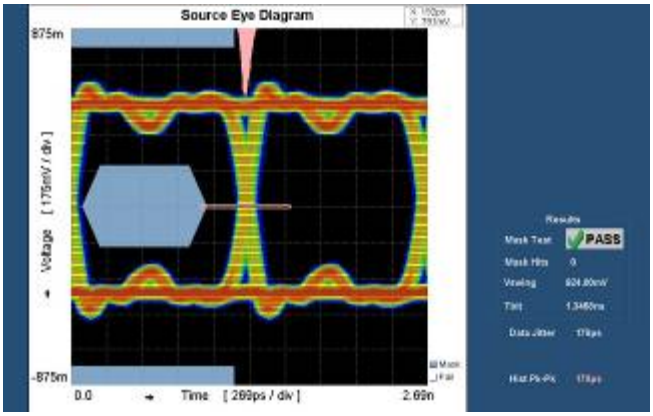


Figure 18: Eye Diagram of D2 when OC_S[3:0]=0000

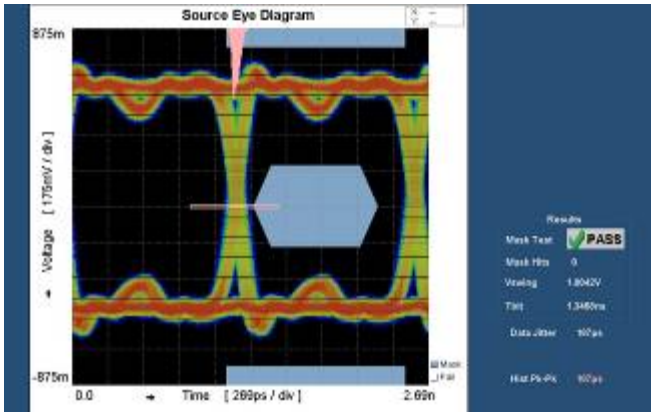


Figure 19: Eye Diagram of D2 when OC_S[3:0]=0001

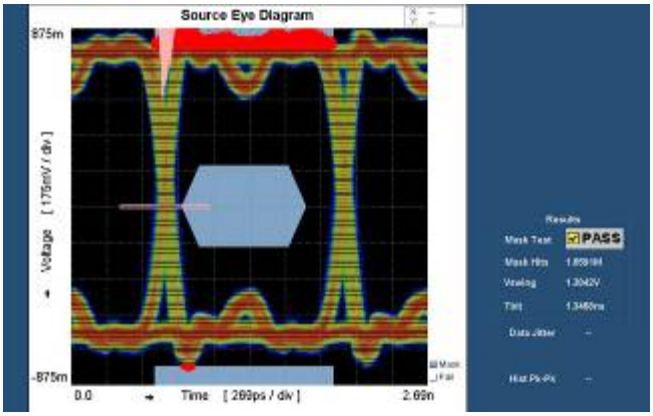


Figure 20: Eye Diagram of D2 when OC_S[3:0]=0010

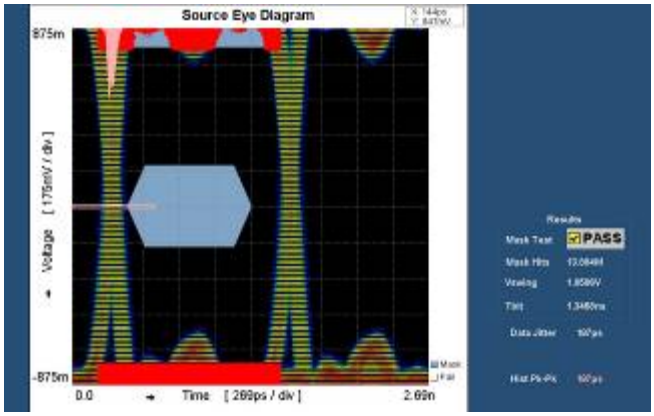


Figure 21: Eye Diagram of D2 when OC_S[3:0]=0011

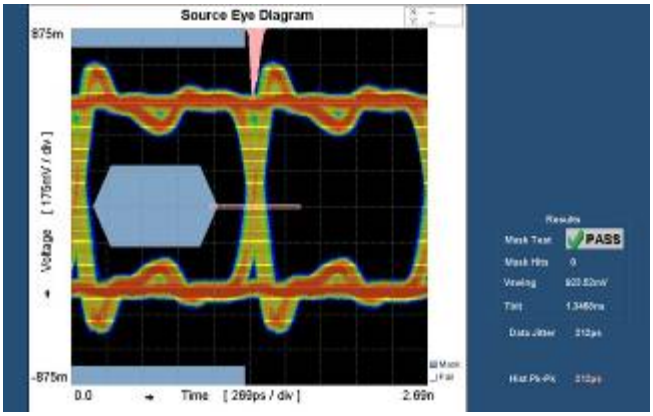


Figure 22: Eye Diagram of D2 when OC_S[3:0]=0101

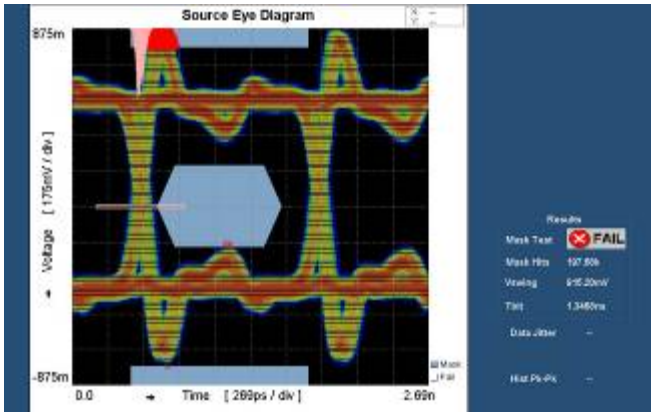


Figure 23: Eye Diagram of D2 when OC_S[3:0]=0110

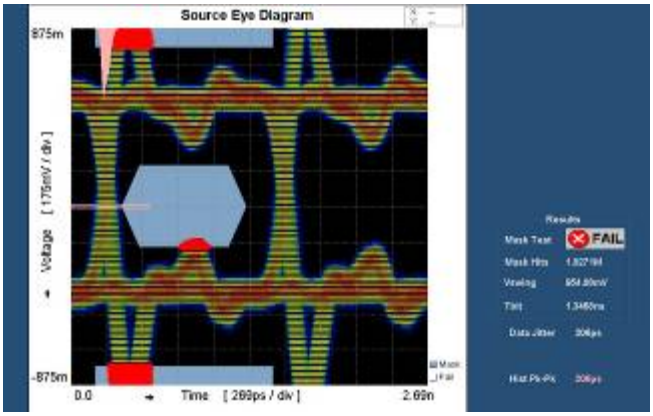


Figure 24: Eye Diagram of D2 when OC_S[3:0]=0111

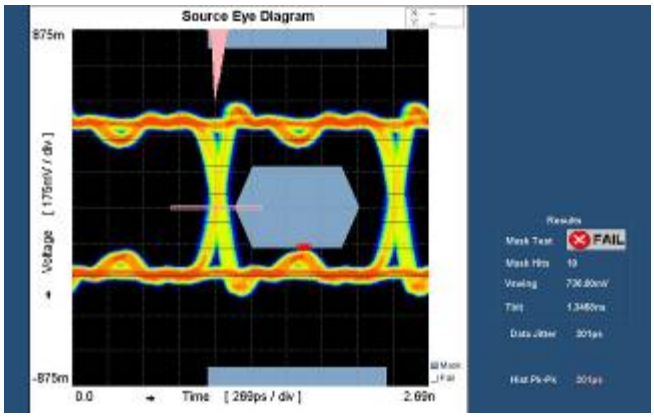


Figure 25: Eye Diagram of D2 when OC_S[3:0]=1000

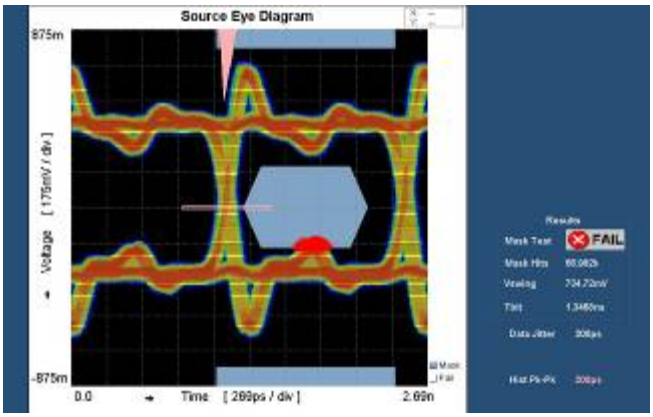


Figure 26: Eye Diagram of D2 when OC_S[3:0]=1001

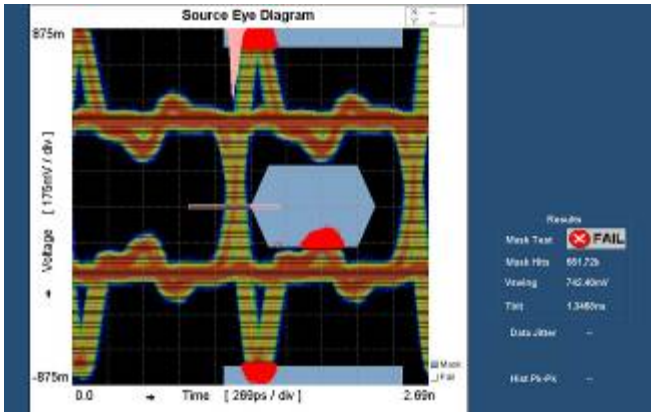


Figure 27: Eye Diagram of D2 when OC_S[3:0]=1010

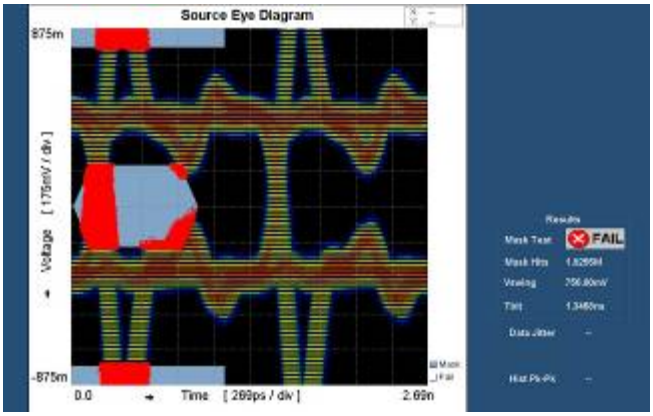


Figure 28: Eye Diagram of D2 when OC_S[3:0]=1011

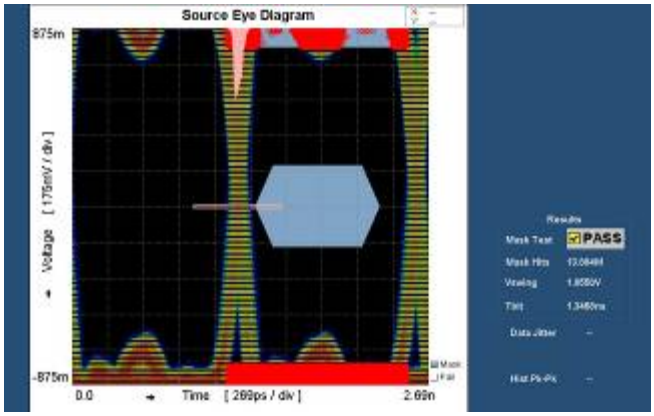


Figure 29: Eye Diagram of D2 when OC_S[3:0]=1100

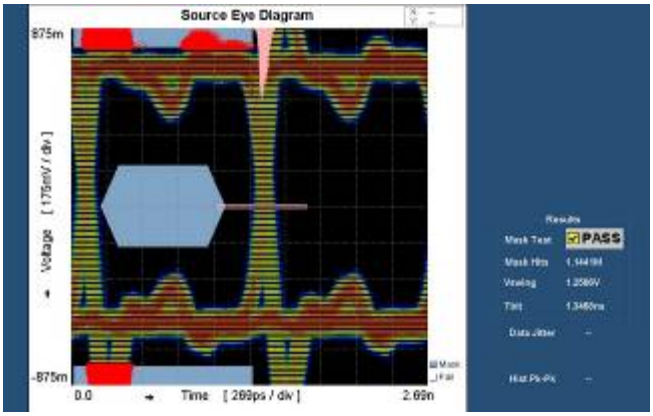


Figure 30: Eye Diagram of D2 when OC_S[3:0]=1101

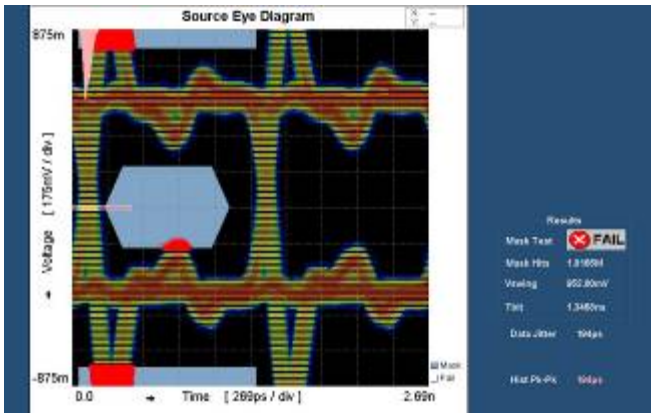


Figure 31: Eye Diagram of D2 when OC_S[3:0]=1110

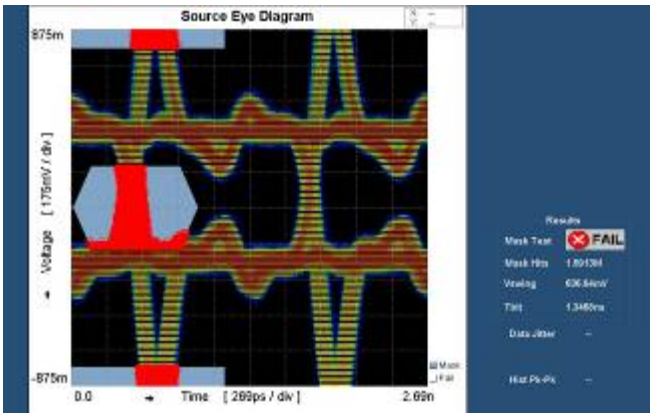


Figure 32: Eye Diagram of D2 when OC_S[3:0]=1111

e. Sink Test ID 8-8: TDR Measurement

Differential impedance of PI3HDMI101 on an HDMI-HDMI demo board is measured to confirm the trace impedance is within the requirement described in Test ID 8-8 in HDMI Compliance Test Specification Version 1.3a.

Test ID 8-8: TMDS – Differential Impedance	
Reference	**Requirement**
[HDMI: Table 4-20] HDMI Sink Impedance at TP2	Through-connection impedance : 100Ω ± 15%* ** A single excursion is permitted out to a max/min of 100 ohms ±25% and of a duration less than 250psecs.* At Termination impedance (when Vicm is within Vicm1 range) 100 ohms ±10%

Table 5: HDMI Pre-test Test ID 8-8 Specification

CDF field Sink_Diff_PowerOn = N for each high speed signal input. At-termination impedance can be measured without powering up PI3HDMI101. The termination of each clock is switched from 50Ω to 250kΩ pull-up when PI3HDMI101 is not powered up. Thus, at-termination impedance cannot be obtained at clock signal.

Through impedance is measured at input side of the HDMI-HDMI demo board. Filter of 180ps is employed throughout the following measurement.
Sink_Term_Distance of CLK = 0.5ns

Through Impedance	D2	D1	D0	CLK	Spec		Units
					Min	Max	
Min	95	90	91	94	85	115	Ω
Max	113	105	104	105	85	115	Ω

Table 6: Through Impedance Result at Connector J101

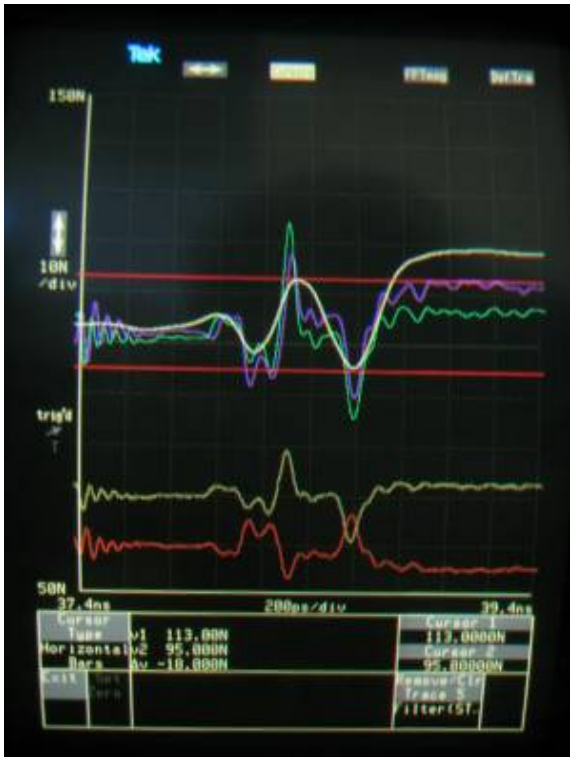


Figure 33a: Through Impedance at D2

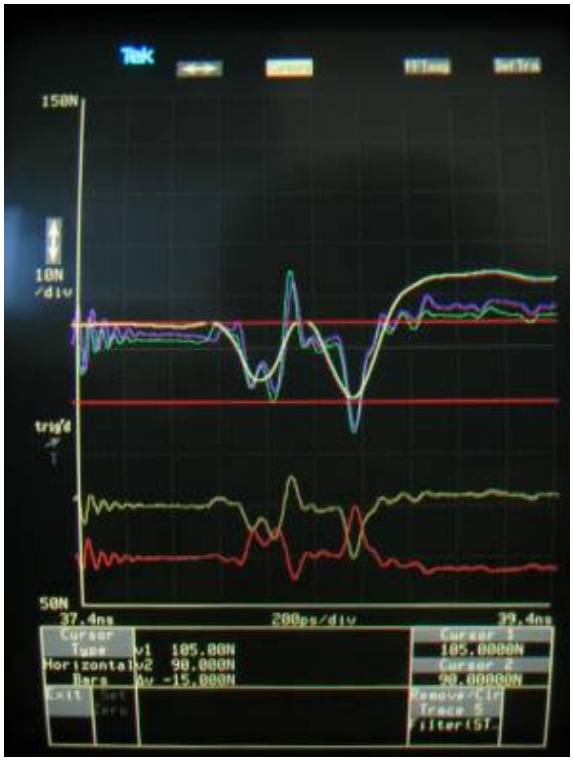


Figure 33b: Through Impedance at D1

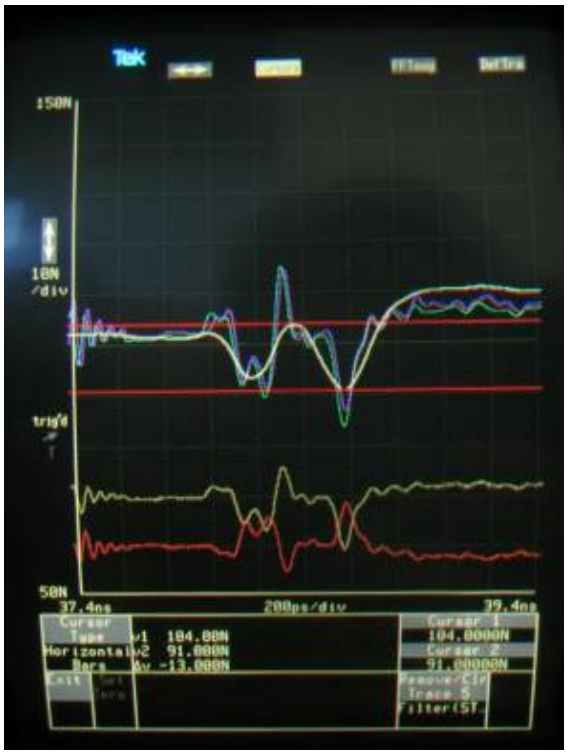


Figure 33c: Through Impedance at D0

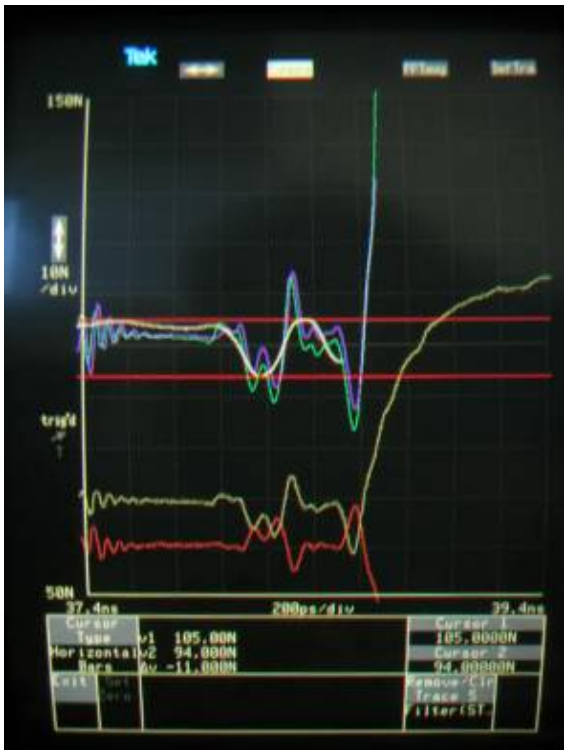


Figure 33d: Through Impedance at CLK

f. Sink Test ID 8-9: DDC/CEC Line Capacitance Measurement

The capacitances of SDA and SCL signals which go through EEPROM AT24C02B are tested. The capacitance of CEC line connecting input to output HDMI is also measured. Results below show that the capacitances are within HDMI CTS V1.3a requirement.

C_{DUT} = C2 – C1
Setting of Impedance Analyzer for measuring capacitance:
For SDA/SCL, Freq=100kHz, DC Bias=2.5V, Power=15dBm (AC~1.8Vpp at DUT), IF BW=1kHz, Sweep Time=1s
For CEC, Freq=100kHz, DC Bias=1.65V, Power=15dBm (AC~1.8Vpp at DUT), IF BW=1kHz, Sweep Time=1s

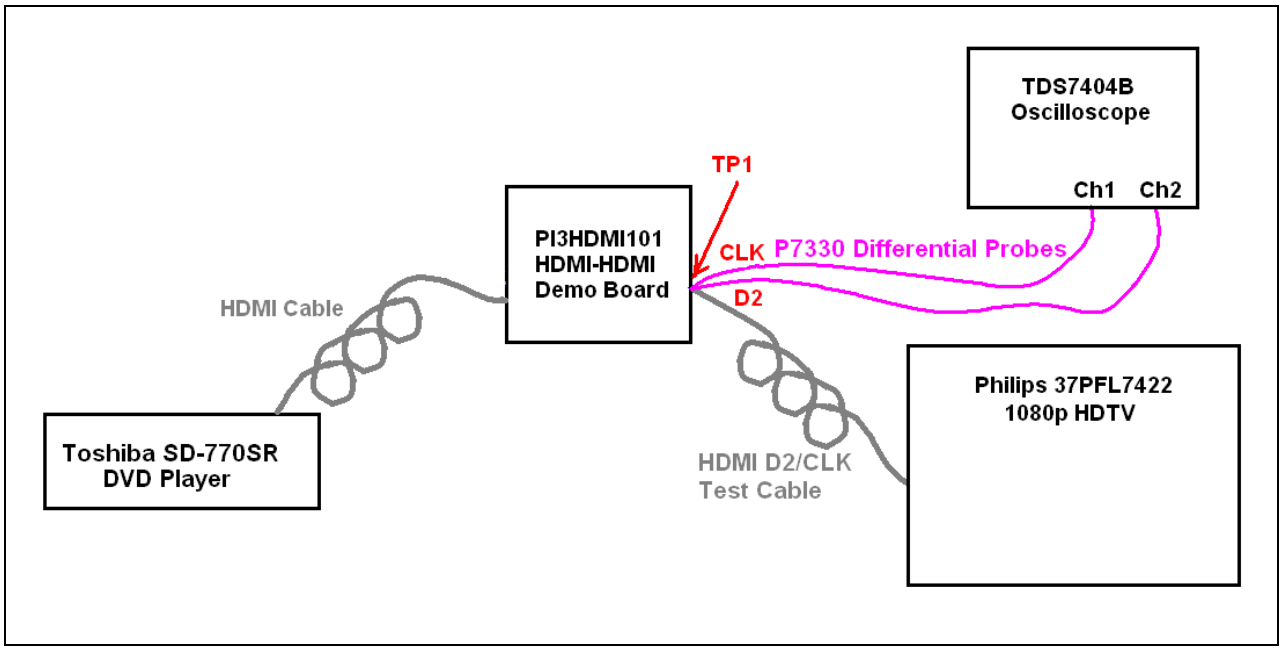
Pin	Parameter	DUT Power		Spec		Units
		Off	On	Min	Max	
SDA	C1	7.2	7.2	NA	NA	pF
	C2	18.3	18.0	NA	NA	pF
	C_{DUT}	11.1	10.8		50	pF
SCL	C1	6.9	6.9	NA	NA	pF
	C2	16.9	16.7	NA	NA	pF
	C_{DUT}	10.0	9.8		50	pF
CEC	C1	7.1	7.1	NA	NA	pF
	C2	14.5	14.6	NA	NA	pF
	C_{DUT}	7.4	7.5		200	pF

Table 7: DDC/CEC Line Capacitance Result at Connector J101

Appendix A: Test Setup

Test setup:

a. For Source Test

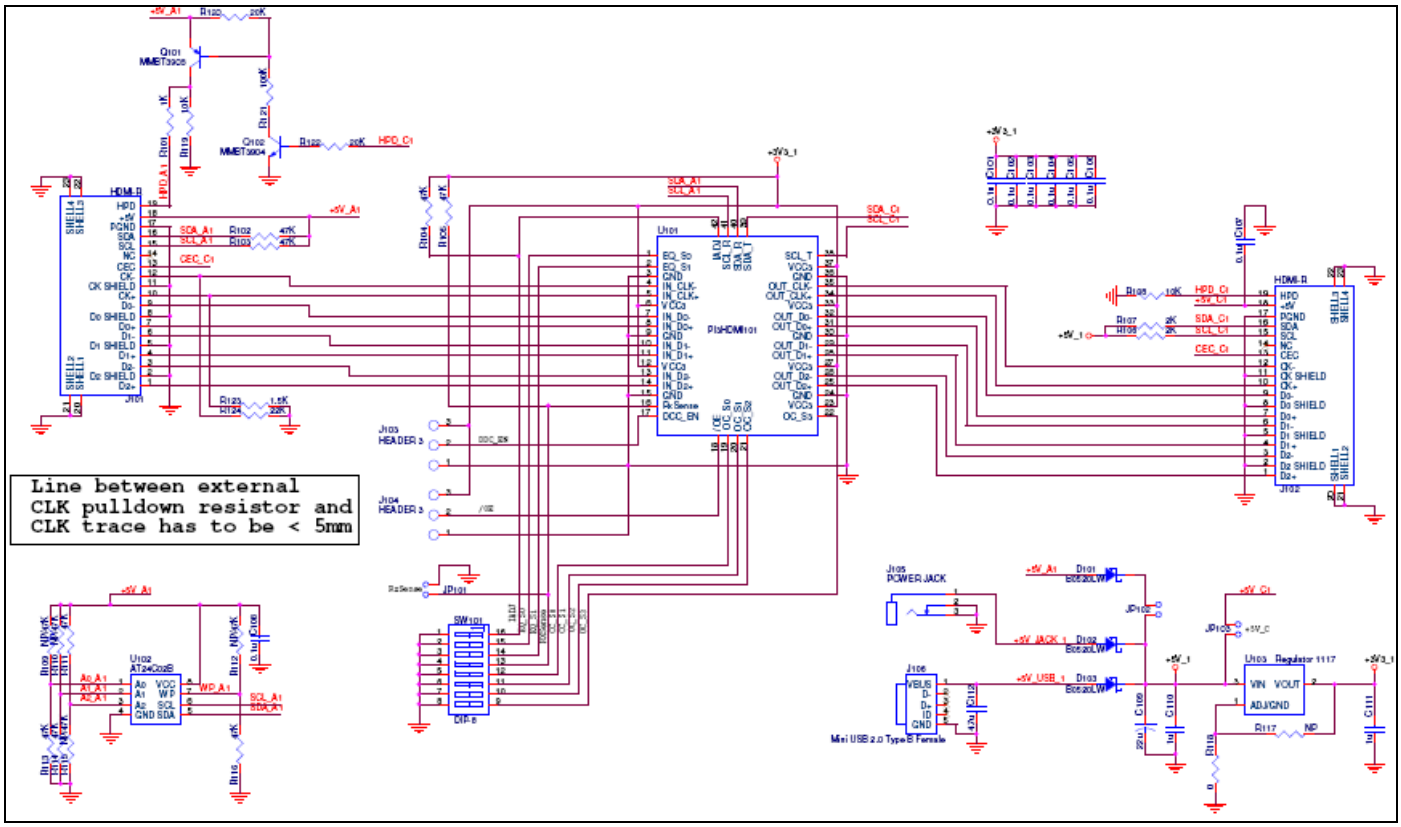


Equipment Use:

a. For Source Test
- TDS7404B Oscilloscope with P7330 Differential Probes
- 1-meter HDMI Cable
- 1-meter HDMI D2/CLK Test Cable
- Toshiba SD-770SR DVD Player
- Philips 37PFL7422 HDTV
- Agilent Power Supply
- 5V DC Adaptor

b. For Sink Test
- Tek11801C Digital Sampling Oscilloscope
- Agilent 4395A Impedance Analyzer with 43961A and 16092A
- SMA Matching Cables
- PSC High BW TDR Test Fixture
- PSC High BW Cap Test Fixture
- Agilent Power Supply
- 5V DC Adaptor

Appendix B: PCB Schematic



Appendix C: PCB Layout Requirements

a. Stack Up:

Plane	Material	Thickness (mil)
Signal		1.9
Prepreg	1080 + 2116	7.3
Ground		1.2
Core		44
Power		1.2
Prepreg	1080 + 2116	7.3
Signal		1.9

b. Isolation Spacing = 30 mil

c. Width & Spacing (W/S) of 100Ω Differential Trace = 9.0 / 10 mil
* W/S for 80 mils before and after contacting the TMDS input/output pads of PI3HDMI101 = 5.0 / 15 mil to compensate the impedance drop of PI3HDMI101 solder pads

Appendix D: BOM List

Item	Quantity	Reference	Description
1	8	C101, C102, C103, C104, C105, C106, C107, C108	0.1uF Capacitor
2	1	C109	22uF Capacitor
3	2	C110, C111	1uF Capacitor
4	3	D101, D102, D103	B0520LW Schottky Rectifier
5	3	JP101, JP102, JP103	2-pin Header
6	2	J101, J102	HDMI Receptacle Connector
7	2	J103, J104	3-pin Header
8	1	J105	Power Jack
9	1	J106	Mini USB Type B Connector
10	1	Q101	MMBT3906 PNP Transistor
11	1	Q102	MMBT3904 NPN Transistor
12	5	R109, R110, R112, R115, R117	NOT AVAILABLE
13	9	R101, R102, R103, R104, R105, R111, R113, R114, R116	47kΩ Resistor
14	2	R108, R119	10kΩ Resistor
15	2	R106, R107	2kΩ Resistor
16	1	R118	0Ω Resistor
17	2	R120, R122	20kΩ Resistor
18	1	R121	100kΩ Resistor
19	1	R123	1.5kΩ Resistor
20	1	R124	22 kΩ Resistor
21	1	SW101	DIP-8 Switch
22	1	U101	PI3HDMI101 HDMI Switch
23	1	U102	AT24C02B EEPROM
24	1	U103	1117 Regulator