PI3HDMI1210
PI3HDMI1210 Demo Board Rev.A User Manual

Introduction
This user manual describes the components and the usage of PI3HDMI1210 demo Board Rev.A.

Figure 1: Top View of PI3HDMI1210 Demo Board

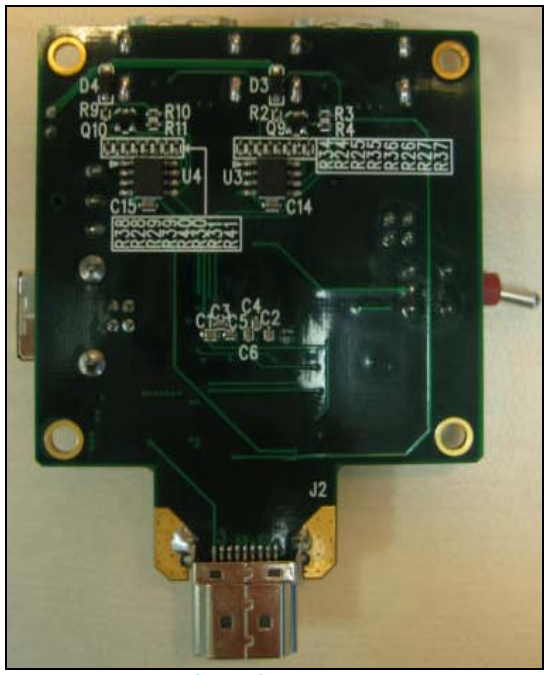


Figure 2: Bottom View of PI3HDMI1210 Demo Board

Key Components / Circuits

a. As PI3HDMI1210 is a 2:1 MUX, a SPDT switch at reference SW1 is used to choose either Port A or B as the input port manually.

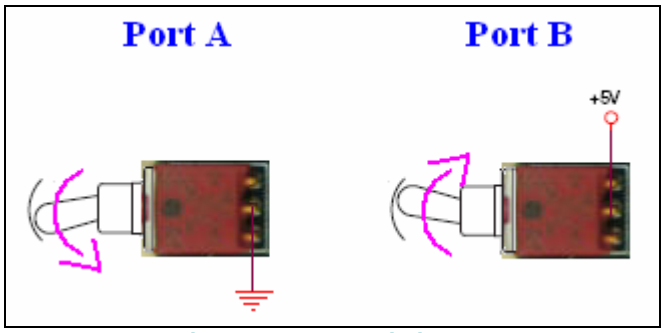


Figure 3: SPDT Switch SW1

When switch SW1 is tied to low, IN and SEL pins of PI3HDMI1210 are set to 0V and 1.5V, respectively, in order to transfer high speed and side-band signals through Port A. When SW1 is switched to high, IN and SEL pins are pulled to 3.3V, Port B is then selected.

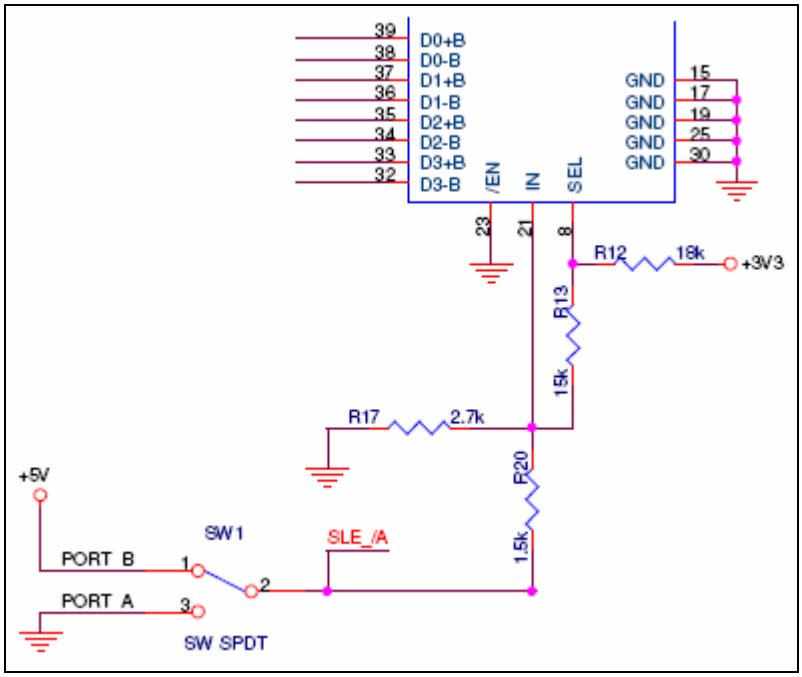


Figure 4: Schematic of Port Selection

b. PI3HDMI1210 demo board can be powered up via three ways, i.e. using 5V supplied from Power Jack (J7), from USB Type B Connector (J8), or from Port A/B (J6). Jumper J6 is not connected at default.

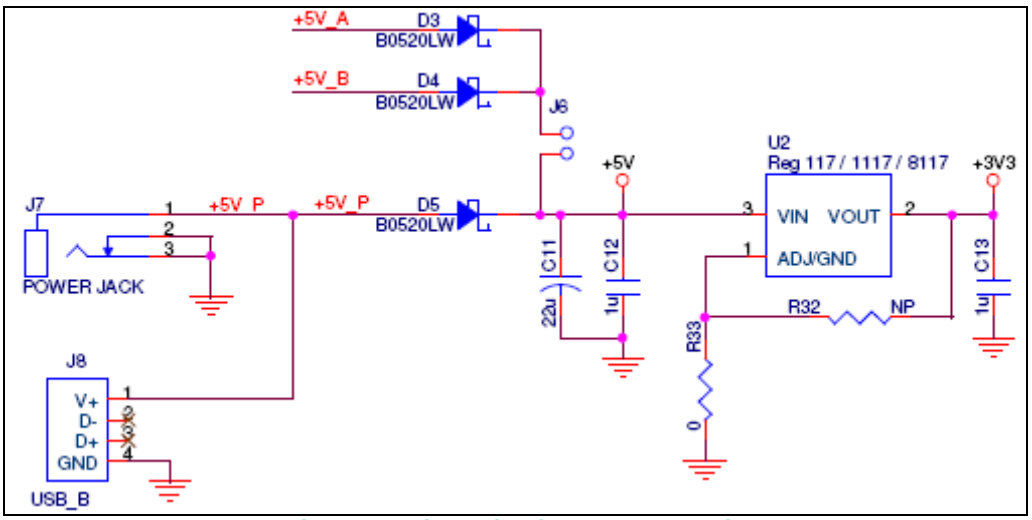


Figure 5: Schematic of 5V Power Supply

c. Two AT24C02B EEPROMs are implemented in PI3HDMI1210 demo board to model I2C application. The EEPROMs are for DDC line capacitance measurement purpose. Please refer to p.8 for measurement result. A0 and A1 address inputs of AT24C02B are pulled to low by external pull-down resistors while address A2 is pulled high. Write protection of the EEPROM is disabled.

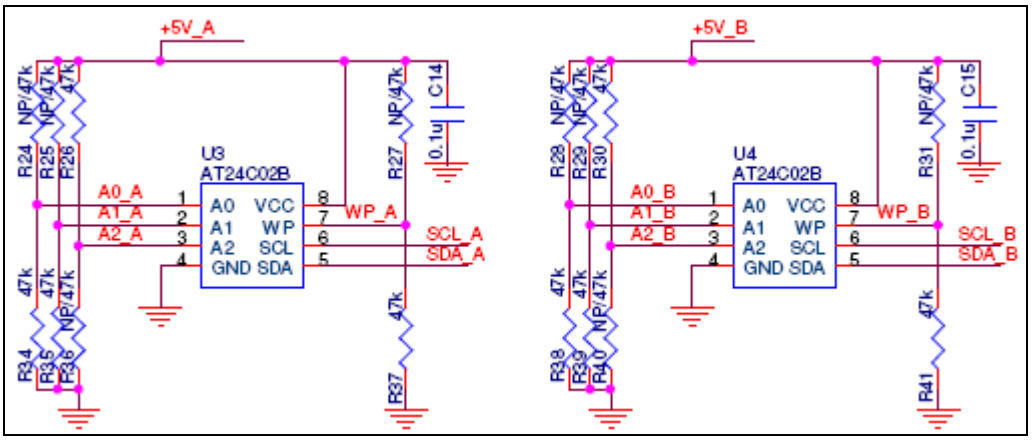


Figure 6: Schematic of EEPROM

d. HPD reset circuitry is implemented at SEL pin. When switching port using switch SW1, a 300ms pulse is sent to reset the HPD pin at the de-selected port so as to reset HDCP Transmitter Link State back to reset state H0. For details, please refer to Application Note AN202 of PI3HDMI1210 for TV Application.

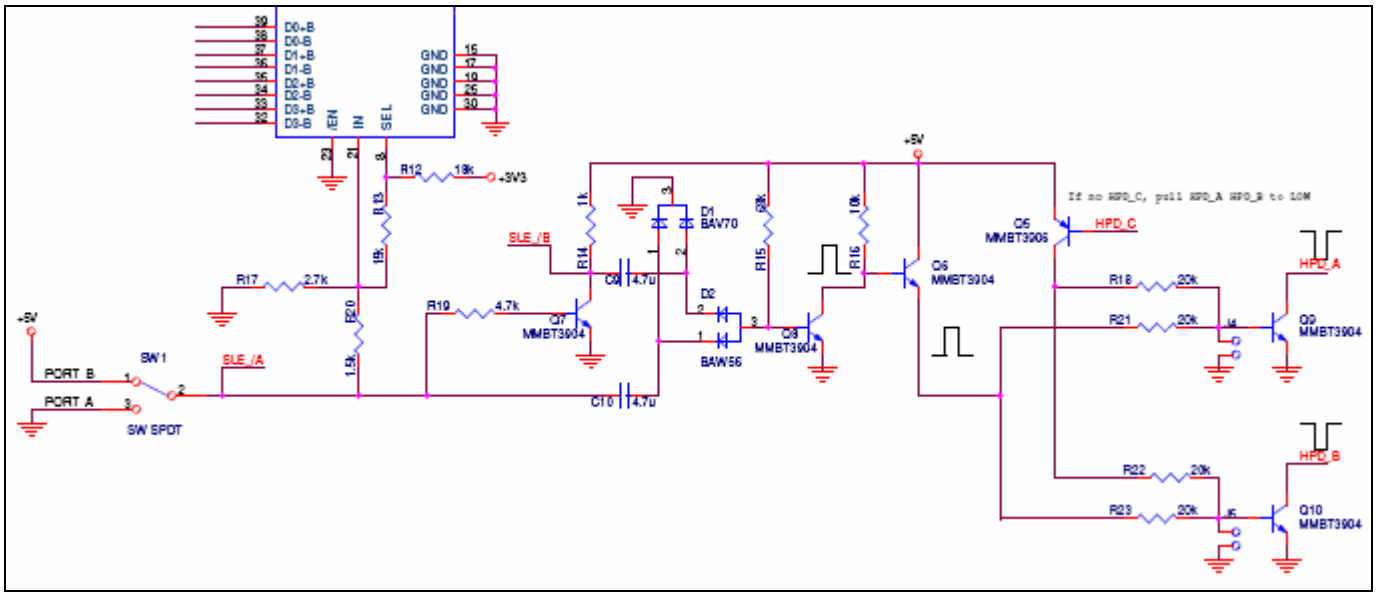


Figure 7: Schematic of HPD Reset Circuit

e. PNP transistors, Q1-Q4 in the schematic below, are used to model RxSense for some DVDs without the ability of sensing the presence of TMDS receiver. This RxSense model removes one pair of TMDS signals externally when the port is de-selected. Without RxSense, DVD will enter reset state H0 and will not fall in long delay special mode. Please refer to Application Note AN202 for details.

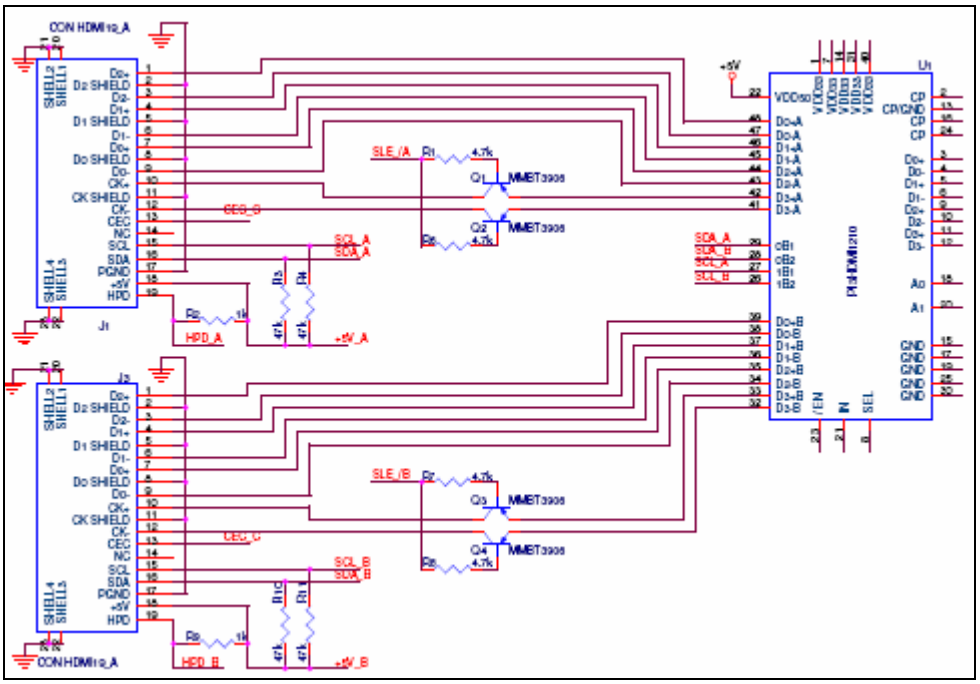


Figure 8: Schematic of RxSense Model

TDR Measurement

Differential impedance of PI3HDMI1210 on a demo board is measured to confirm the trace impedance is within the requirement described in Test ID 8-8 in HDMI Compliance Test Specification Version 1.3a.

Test ID 8-8: TMDS – Differential Impedance	
Reference	**Requirement**
[HDMI: Table 4-20] HDMI Sink Impedance at TP2	Through-connection impedance : 100Ω ± 15%* * *A single excursion is permitted out to a max/min of 100 ohms ±25% and of a duration less than 250psecs.* At Termination impedance (when Vicm is within Vicm1 range) 100 ohms ±10%

Table 1: HDMI Pre-test Test ID 8-8 Specification

CDF field Sink_Diff_PowerOn = Y for this device. This means no termination impedance can be obtained. Filter of 180ps is employed throughout the measurement.

For Port A:

Sink_Term_Distance of D2 = 0.60ns
Sink_Term_Distance of D1 = 0.58ns
Sink_Term_Distance of D0 = 0.58ns
Sink_Term_Distance of CLK = 0.44ns

For Port B:

Sink_Term_Distance of D2 = 0.52ns
Sink_Term_Distance of D1 = 0.53ns
Sink_Term_Distance of D0 = 0.56ns
Sink_Term_Distance of CLK = 0.35ns

Through Impedance		D2	D1	D0	CLK	Spec		Units
						Min	Max	
Port A	**Min**	99	92	92	99	85	115	Ω
	Max	117 (1)	115	115	113	85	115	Ω
Port B	**Min**	99	92	91	98	85	115	Ω
	Max	117 (1)	115	115	115	85	115	Ω

Note: (1) A single excursion which is less than 250ps passes TDR requirement.

Table 2: TDR Through Impedance Result

Figure 9a: TDR at D2 of Port A

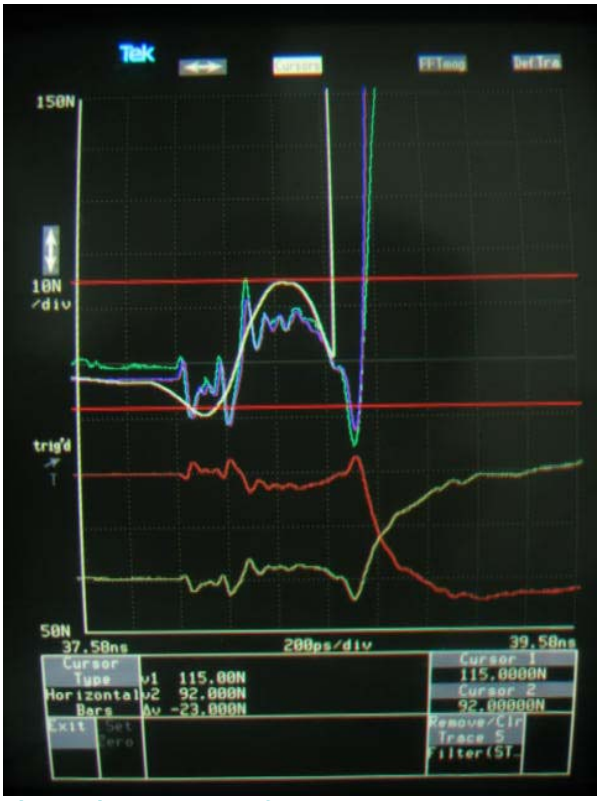


Figure 9b: TDR at D1 of Port A

Figure 9c: TDR at D0 of Port A

Figure 9d: TDR at CLK of Port A

Figure 10a: TDR at D2 of Port B

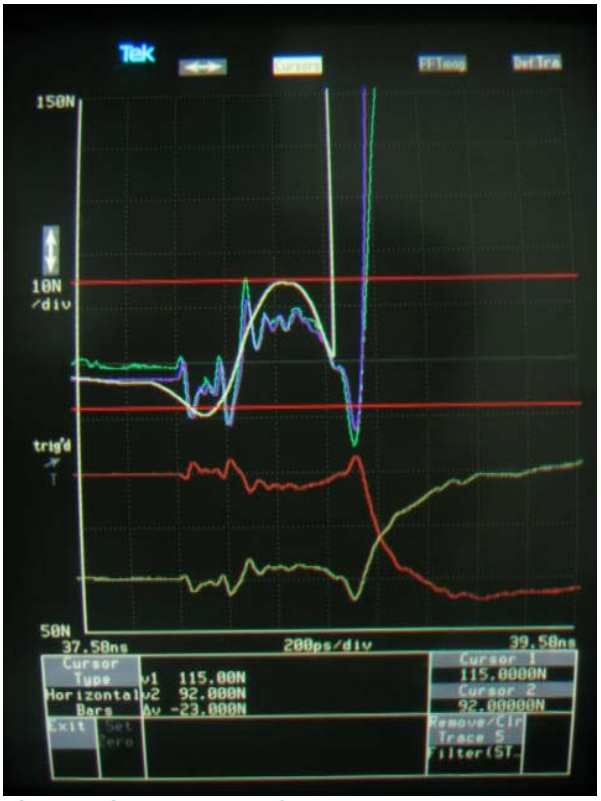


Figure 10b: TDR at D1 of Port B

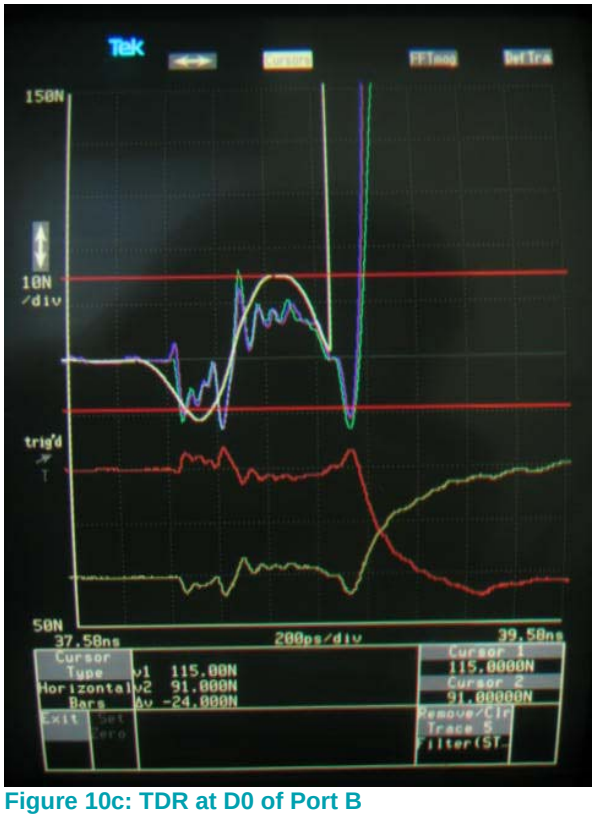


Figure 10c: TDR at D0 of Port B

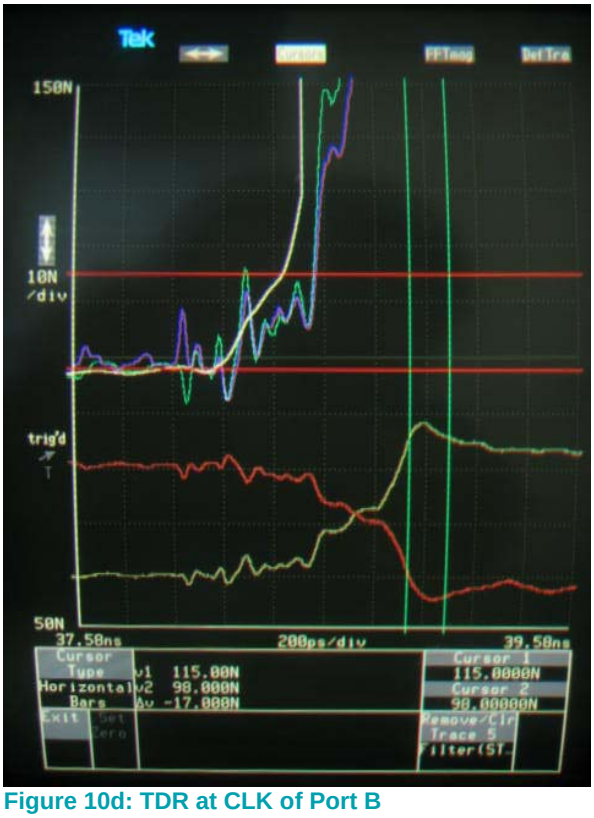


Figure 10d: TDR at CLK of Port B

DDC/CEC Line Capacitance Measurement

The capacitances of SDA and SCL signals which go through EEPROM AT24C02B are tested on a similar PCB design. The capacitance of CEC line connecting input to output HDMI is also measured. Results below show that the capacitances are within HDMI CTS V1.3a requirement.

C_{DUT} = C2 – C1

Setting of Impedance Analyzer for measuring capacitance:

For SDA/SCL, Freq=100kHz, DC Bias=2.5V, Power=15dBm (AC~1.8Vpp at DUT), IF BW=1kHz, Sweep Time=1s

For CEC, Freq=100kHz, DC Bias=1.65V, Power=15dBm (AC~1.8Vpp at DUT), IF BW=1kHz, Sweep Time=1s

Connector J1

Pin	Parameter	DUT Power		Spec		Units
		Off	On	Min	Max	
SDA	C1	7.2	7.2	NA	NA	pF
	C2	17.3	26.4	NA	NA	pF
	C_{DUT}	10.1	19.2		50	pF
SCL	C1	7.4	7.4	NA	NA	pF
	C2	16.9	25.9	NA	NA	pF
	C_{DUT}	9.5	18.5		50	pF
CEC	C1	7.5	7.5	NA	NA	pF
	C2	23.7	23.7	NA	NA	pF
	C_{DUT}	16.2	16.2		200	pF

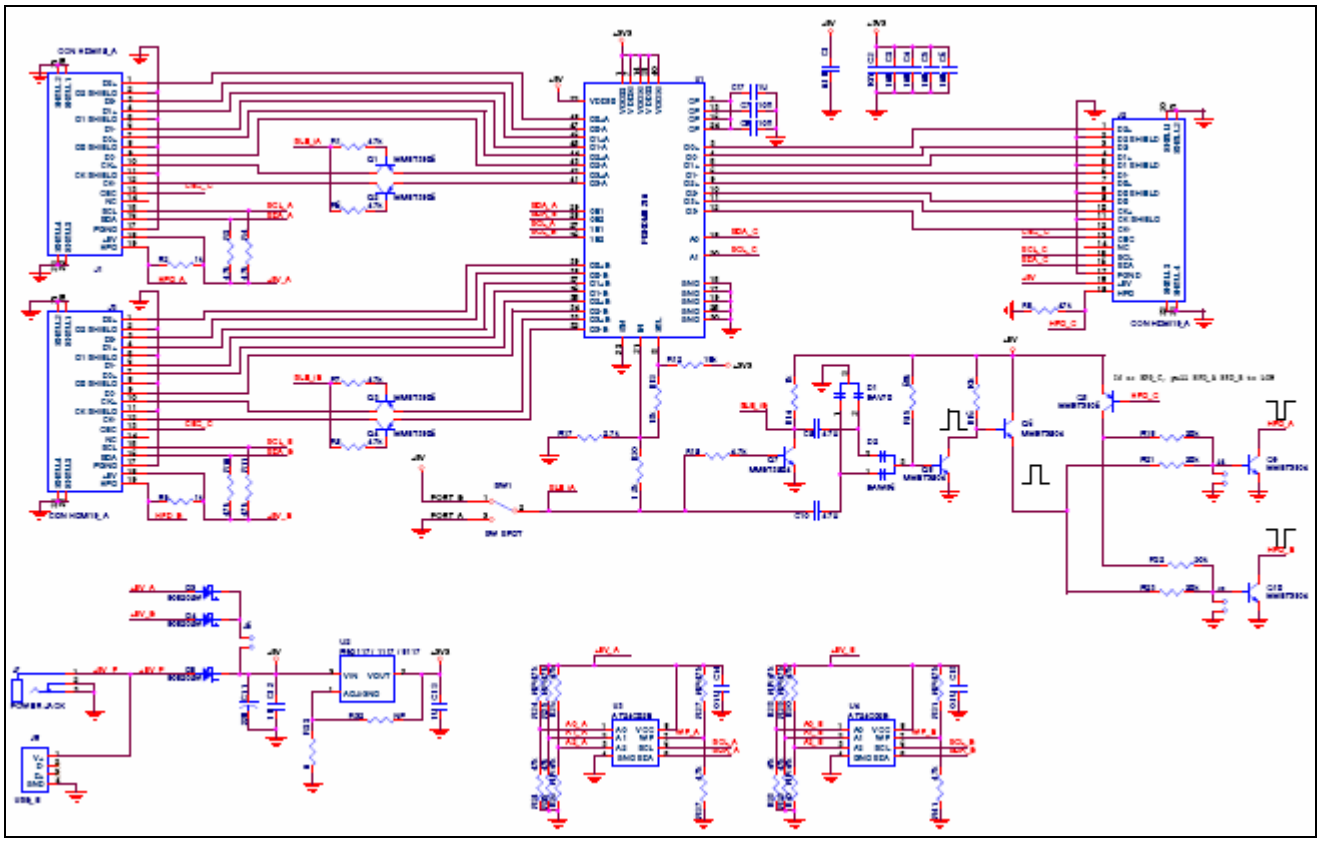
Table 3a: DDC/CEC Line Capacitance Result at Connector J1

Connector J3

Pin	Parameter	DUT Power		Spec		Units
		Off	On	Min	Max	
SDA	C1	7.2	7.2	NA	NA	pF
	C2	16.9	26.1	NA	NA	pF
	C_{DUT}	9.7	18.9		50	pF
SCL	C1	7.4	7.4	NA	NA	pF
	C2	15.4	24.4	NA	NA	pF
	C_{DUT}	8.0	17.0		50	pF
CEC	C1	7.5	7.5	NA	NA	pF
	C2	23.7	23.8	NA	NA	pF
	C_{DUT}	16.2	16.3		200	pF

Table 3b: DDC/CEC Line Capacitance Result at Connector J3

Appendix A: PCB Schematic



Appendix B: PCB Layout Requirements

a. Stack Up:

Plane	Material	Thickness (mil)
Signal		1.9
Prepreg	1080 + 2116	7.3
Ground		1.2
Core		44
Power		1.2
Prepreg	1080 + 2116	7.3
Signal		1.9

b. Isolation Spacing = 30 mil

c. Width & Spacing (W/S) of 100Ω Differential Trace = 9.0 / 11 mil

Appendix C: BOM List

Item	Quantity	Reference	Description
1	3	C1, C14, C15	0.1uF Capacitor
2	7	C2, C3, C4, C5, C6, C7, C8	10nF Capacitor
3	2	C9, C10	4.7uF Capacitor
4	1	C11	22uF Capacitor
5	3	C12, C13, C17	1uF Capacitor
6	1	D1	BAV70 Double Diode with Common Cathodes
7	1	D2	BAW56 Double Diode in Series
8	3	D3, D4, D5	B0520LW Schottky Rectifier
9	2	J1, J3	HDMI Receptacle Connector
10	1	J2	HDMI Plug Connector
11	3	J4, J5, J6	2-pin Header
12	1	J7	Power Jack
13	1	J8	USB Type B Connector
14	5	Q1, Q2, Q3, Q4, Q5	MMBT3906 PNP Transistor
15	5	Q6, Q7, Q8, Q9, Q10	MMBT3904 NPN Transistor
16	5	R1, R6, R7, R8, R19	4.7kΩ Resistor
17	3	R2, R9, R14	1kΩ Resistor
18	13	R3, R4, R5, R10, R11, R26, R30, R34, R35, R37, R38, R39, R41	47kΩ Resistor
19	1	R12	18kΩ Resistor
20	1	R13	15kΩ Resistor
21	1	R15	68kΩ Resistor
22	1	R16	10kΩ Resistor
23	1	R17	2.7kΩ Resistor
24	4	R18, R21, R22, R23	20kΩ Resistor
25	1	R20	1.5kΩ Resistor
26	1	R33	0Ω Resistor
27	8	R24, R25, R27, R28, R29, R31, R36, R40	NOT AVAILABLE
28	1	SW1	SPDT Switch
29	1	U1	PI3HDMI1210 HDMI Switch
30	1	U2	1117 Regulator
31	2	U3, U4	AT24C02B EEPROM