

How to De-bug and Design DDR Memory Modules

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Introduction

The upgrade from Single Data Rate SDRAM to Double Data Rate (DDR) SDRAM is well under way. DDR technology enables memory subsystems to transfer data at twice the frequency of Single Data Rate. Although many things will stay the same for the consumer, this is a major enhancement. For instance, a DDR266 Memory DIMM running at 133MHz will provide 2.1 Gbytes/sec of data transfer. This is good news in that the memory subsystem will be transferring data at twice the clock speed. In this article we will explain some of the history in memory technology, and demonstrate how to design and Debug Registered DDR DIMMs.

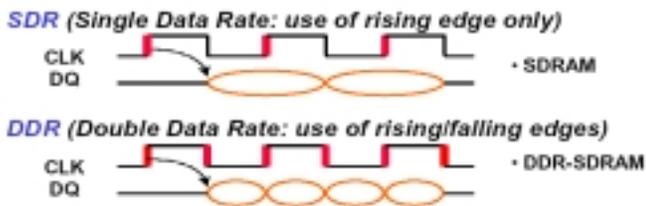


Figure 1. A comparison between Single Data Rate and Double Data Rate

The Challenge of DDR

While the memory controller in the North Bridge is working twice as hard, the same goes for the memory chips, as well as the clock PLL, and the registers on the DIMM. The motherboard is also performing more efficiently as it is now transferring data at 400MHz instead of 100MHz. Let's say an engineer is designing DDR400 DIMMs, a period of which is $1/400\text{MHz} = 2.5\text{ns}$. This is not impossible, but it's making the engineer's life very challenging. The data will have to be driven from the different DRAM chips through the connector to the North Bridge all within 2.5ns. This is not an easy task, and where the challenge lies. No matter how good individuals engineering skills are, there is definitely much less margin for errors. It was not long ago that many chips needed 2 to 3ns just for set-up. Needless to say, it is becoming much more challenging moving forward with little or no margin as relief. Thus, the need to understand advanced memory technology becomes imperative. This document will help provide the nuts and bolts on how to design a DDR Registered DIMM, and how to debug it.

Memory Technology

Memory technology has changed quite a bit in the last ten years. You might remember that we used to have FPM, then we moved to EDO. Then we made a bigger change when we moved to Synchronous DRAM. And now we are working on DDR SDRAM. Progression will not stop here as the industry is actively trying to define DDR2, which will move the frequency up to 533MHz.

FPM Memory

Fast Page Mode. This is the memory technology that was available in the 1980's. It was asynchronous, and the memory controller was working at 33 or 66 MHz. A typical cycle was that you drive the Row Address Strobe and you present the row address. Then you do the same for the column address. After that you wait for an access time and the memory will drive the data for you.

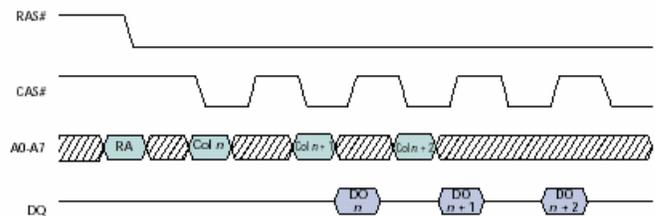


Figure 2 - Typical Cycle of FPM Memory

EDO Memory

This memory was very similar to FPM with the exception of now the Column Address Strobe signal can go high without tri-stating the memory output. This resulted in the data being more available on the North Bridge chip or the CPU, and by consequence will have more time for CAS pre-charge time.

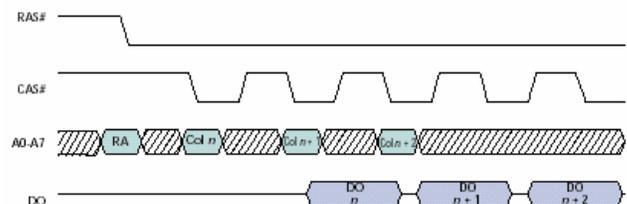


Figure 3 – EDO Memory

SDRAM Memory

Synchronous SDRAM has an external clock to synchronize input commands and addresses to the rising edge of the clock. This synchronization makes timing more precise with other system components such as the North Bridge, CPU and other devices.

SDRAM memory is also Command driven instead of Signal driven. There is a user programmable register that selects CAS Latency (access time), and Burst length and Type.

The basic operation of FPM, EDO, and SDRAM memory technology is the same. The Row is opened by RAS# falling, and the Columns are opened by CAS# falling. For SDRAM these commands must be available on the rising edge of the clock.

During a read cycle, after the Row active and the Column active command, read data will be driven from the rising edge of the clock on the DQ lines after the programmed CAS# latency time. The SDRAM will continue to drive the DQ lines until the next rising edge of the clock.

The signals WE#, CAS#, RAS#, and CS# are used to decode the command to the SDRAM chip. At every rising edge of the clock, the SDRAM will latch and execute the latched command. The signals no longer need to be measured with respect to each other. On the contrary, they are latched on the rising edge of the clock. This is the same for address and data.

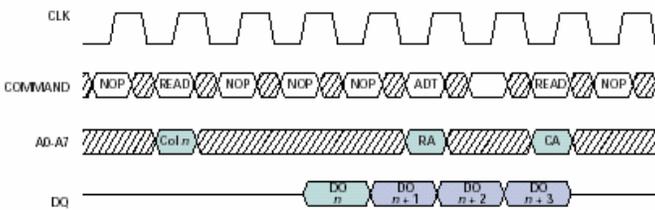


Figure 4 - SDRAM Memory

Double Data Rate (DDR) SDRAM

Aside from a few differences, DDR SDRAM is very similar to SDR. The DDR architecture is source synchronous. The data is captured twice per clock cycle using the bi-directional data strobe signal. This architecture uses a 2n prefetch architecture where the internal data bus is twice the size of the external data bus. The following describes the main differences of the two SDRAM types:

1. SDRAM is a Synchronous Architecture while the DDR SDRAM is a source-synchronous architecture. DDR uses a bi-directional Strobe that is driven by the chip that drives the data.
2. The signal interface is SSTL_2 for DDR while it is LVTTTL

for SDR. Stub Series Terminated Line for 2.5 Volts (SSTL_2) is a standard approved by JEDEC document # EIA/JESD8-9

3. VDD is 2.5V for DDR, while it is 3.3V for SDR. DDR is more compatible with newer process technologies and consumes less power.
4. Vref is an added signal to the DRAM DIMM. Vref is 1.25V and is the reference for differential input signals.
5. CK# is an additional signal. This is necessary since DDR uses a differential clock.
6. DQS is added as a data strobe. This is a bi-directional signal driven by the source and is an architectural change due to DDR being a source synchronous architecture.
7. DM is the Data Mask signal and is an additional pin for DDR. It replaces DQM for SDR DRAMs. This signal is only used to mask write data.

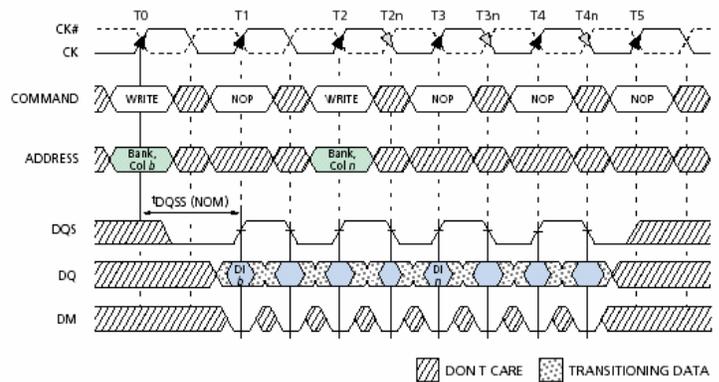


Figure 5

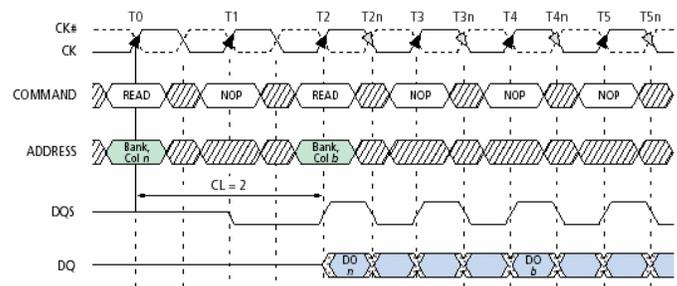


Figure 6

DDR Registered DIMMs are used in numerous Servers, Datacom and Telecom Systems. Many CPUs and chipsets support DDR DRAMs. The following is a system block diagram of a memory subsystem to illustrate how the DDR DIMMs fit into the system. Registered DIMMs are needed for a server because it has registers and a PLL clock driver to make the registered DIMM look like a single load to the Memory controller.

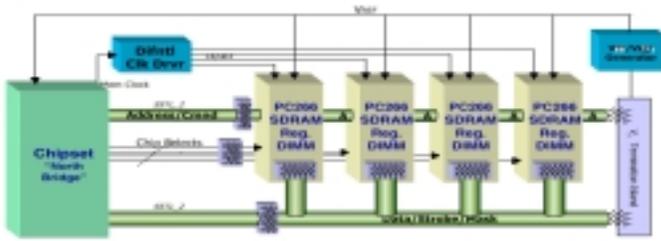


Figure 7 - Block Diagram of a Memory Subsystem

The DDR Registered DIMM offers reduced system loading by including on-board registers for additional signal drive strength, and a zero-delay PLL (Phase-Locked Loop) for clock distribution. These two components are critical in the DIMM design. The Register is required to have a maximum of 2.8 nano-seconds of propagation delay. The PLL is designed to drive 10 output clocks with zero delay from the input with a maximum of 100 pico-seconds skew, and less than 100 pico-seconds of half-period jitter.

These are extremely stringent requirements and they are also the keys to making this technology work. As you know the DIMM connects directly onto the Motherboard.

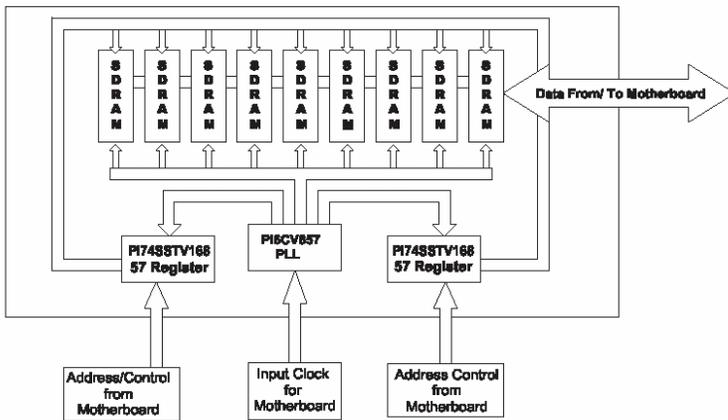


Figure 8 - DDR Registered DIMM Block Diagram

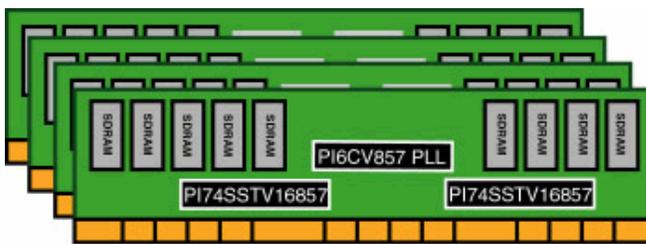


Figure 9 - DDR Registered DIMM Example

DIMM Connector

The DIMM mainly connects with the North Bridge or the Memory Controller Hub on the motherboard. The main signals are the DRAM control address and data busses along with the input clock.

How to test a DDR Registered DIMM

There are many tools to test the DIMM and the first step is to ensure that the PC or the system is able boot. This will verify that you can read and write the correct data in and out of the memory subsystem.

Memory Tester Tool

Memory testing hardware and software allows you to send multiple data streams to the DIMM and display the results on a monitor. It is recommended to run these tests at high /low VCC and temperature to really stress the system. This tool will need an available PCI slot in any PC. A memory tester tool that we have been using is from Ultra -X. This product is the RST Pro (RAM Stress Test Professional).

Winmark

Another stress test is to run the Winmark by MadOnion Corporation. This will access the memory very extensively by displaying high definition graphics on the screen. This test sometimes finds problems that the above hardware was not able to detect.

CST Board

The CST board will enable you to power up the DIMM without plugging it into a PC. This is mainly useful in debugging the PLL. With this board you can measure the clock phase offset, skew, and jitter.

Registered DDR timing budgets

DDR SDRAM will improve overall system performance and bottlenecks in our computing systems. This will also make the net margin very small which will make it easy to find some compatibility problems between different systems and DIMMs. The table below will explain the margin for error that we have available. This data is based on the maximum specification for the PLL and the Register. It is also based on DIMM PCB Simulation. You can see that the margin is about 270 pico-seconds. This is not very much margin, but it has been achievable and DDR333 is in production now.

Parameter	Setup Timing	Hold Timing
TClock Period	6.0ns	NA
TPD (register clock to out)	-2.8ns	1.1ns
T net delay (flight time)	-1.39ns	.28ns
Treg (reg clock shift)	-.1	.1
T setup/hold (DRAM)	-.8	-.75
Tskew (clock jitter /skew)	-0.275	-0.2
Tss (simultaneous switch effect)	-0.266	NA
TXTLK (crosstalk)	-0.1	-0.1
Margin	0.269ns	0.230ns

Table 1: DDR333 timing margin based on Pericom's PI6CV857 PLL, and PI74SSTVF16857 Register

How to Debug DDR DIMMs

After testing and figuring out that a DIMM problem exists, an examination of the various components is required to narrow down and discover how to fix the problem. All chips in the system are important and they all have to work within their specification.

PLL Tuning and Debug

The PLL will receive one differential clock input and drive ten differential clock outputs while connected to the DRAMs as well as the registers. The CST reference board is a good start to debugging the clock. The clock also has feedback signals. These signals have a feedback capacitor to tune the Phase Offset from the input to the output. This feedback capacitor can help you to move the clock by few hundred pico-seconds to see if this fixes the problem. Changing the feedback capacitor can change the clock inputs to the DRAMs.

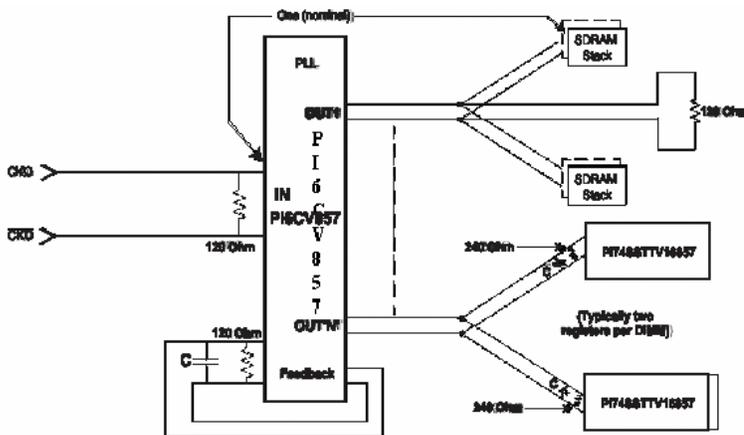


Figure 10 – PLL connection on the Registered DIMM

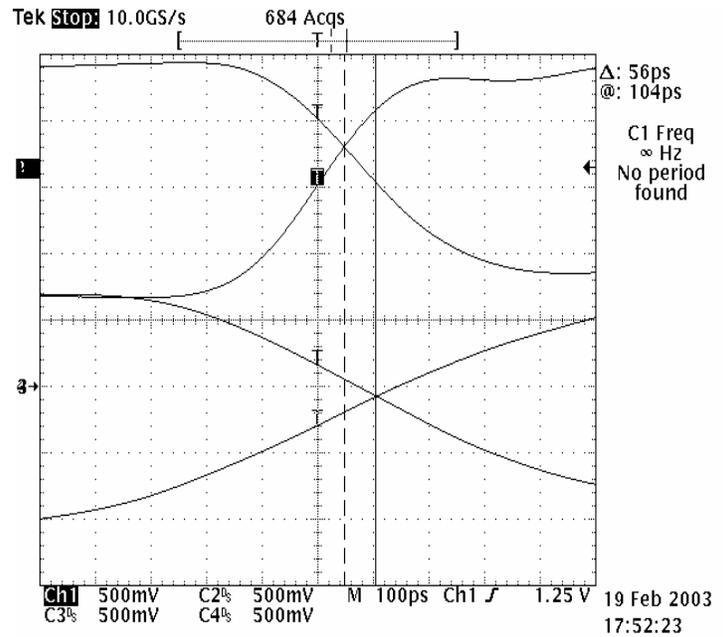


Figure 11. Timing for CLK_IN to MEM_IN on 512MB. R @ FB = 120-ohm, C @FB = 0pF, R @ CLK_IN = 120-ohm, R @ REG_IN = 240-ohm. Top signals: Clk_in/Clk_in# input to the PLL, Bottom signals: Memory_in/memory_in#, input to the memory

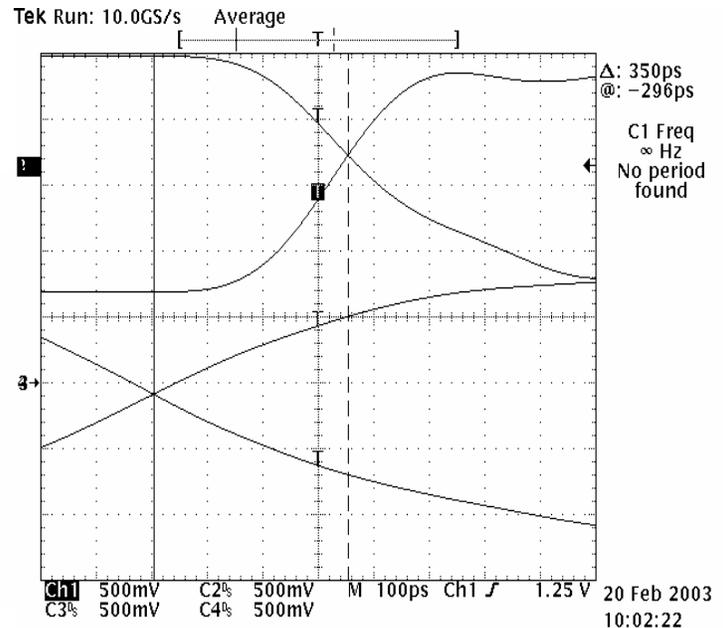


Figure 12. Timing for CLK_IN to MEM_IN on 512MB, R @ FB = 120-ohm, C @FB = 8pF, R @ CLK_IN = 120-ohm, R @ REG_IN = 240-ohm. Top signals: Clk_in/Clk_in# input to the PLL, Bottom signals: Memory_in/memory_in#, input to the memory

Notice that in Figure 11 when the feedback capacitor is 0 picofarad, the clock at the memory in chip is lagging the clock at the PLL by 56ps. By changed the CF_In to 8pF, the clock at the memory in chip is leading the clock at the PLL by 350ps. That is a total difference of 406ps and the result of adding an 8pF capacitor at the feedback_in input to the PLL Chip. The feedback_in capacitor should be tuned so that the clock at the input to the PLL and the Clock at the input to the memory is 0ps thus making these two clocks aligned. These numbers are specific to this DIMM design.

Termination Resistor

The DDR DIMM specification recommends a 120-ohm resistor be placed on the destination input for the clock. The resistor is placed between the two differential signals. This resistor needs to be 240-ohms for each of the registers since there is typically two registers per DIMM for DDR I. These resistors will play an important role for clock timing as changing these resistors will alter the timing of the clock. For example, if you need more set-up time for the register, you need to select a different value register. Please see the waveforms below.

When comparing Figures 11 and 13, you will notice that in Figure 11 the clock at the memory was lagging by 56ps. While in Figure 13 the clock at the memory is leading by 102ps. This is a 158ps difference caused by changing the resistor at the feedback_in of the PLL from 120-ohm to 0-ohm. You can also change the resistor at other components such as the memory_in or the register_in clock input. This will allow you to add more setup or hold margin on these specific systems. Changing the feedback resistor value is not recommended by JEDEC. This is only a method that can be used to debug the DIMM and find out why it might be failing.

Register Debug

The simple register is a key component on the DIMM and can make a big difference in performance. Table 1 above reveals that a large amount of the clock period is taking by the register. The register has 2.8ns maximum propagation delay and is about 46 % of the period. Notice that DDR333 has only 269ps of margin. The register latches the memory Control and address signals. Depending on how strong the Memory Controller Hub is driving these signals and the clock, this might have be a problem.

Scope out the input and output data from the register. Also ensure that the register is providing the address and control signals to the output of the register within less than 2.8ns. If this is not happening, move the clock of the register to lead the clock of the DRAMs in order to compensate for the register providing late address and control signals to the DRAMs. The propagation delay from the register input clock to the Memory input data measure to be 2.44ns.

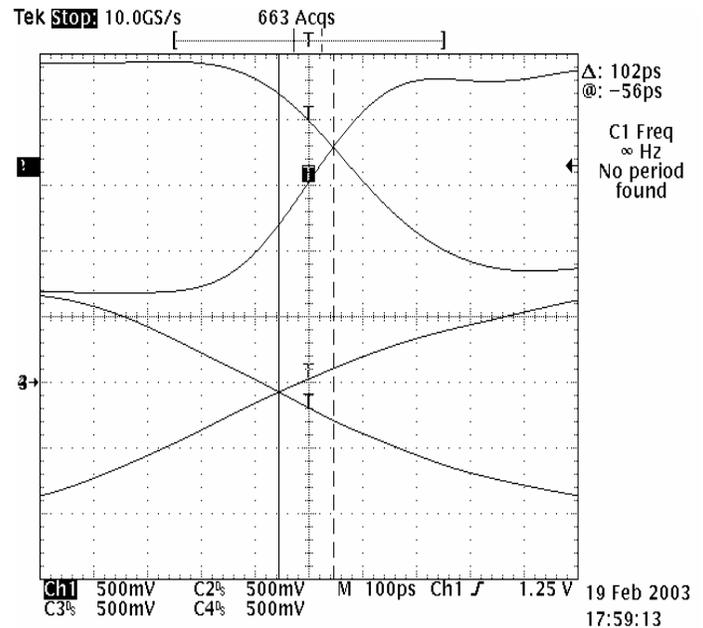


Figure 13: Typical DIMM design. Figure 13. Timing for CLK_IN to MEM_IN on 512MB. R @ FB = 0, C@FB = 0pF, R@CLK_IN = 120-ohm, R@REG_IN = 240-ohm. Top signals: CLK_in/CLK_in# input to the PLL, bottom signals: Memory_in/memory_in#, input to the memory

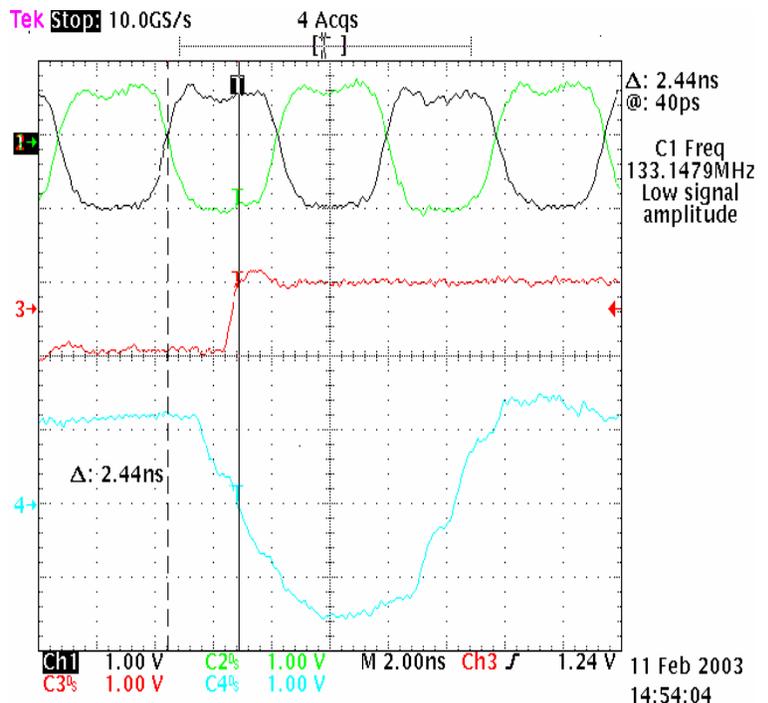


Figure 14: Top signal: Clock_in at the register Middle signal: Register input data Bottom signal: register output data at the Memory input.

Conclusion

DDR DIMMs provide a much needed performance boost to systems while at the same time render the system design more challenging by providing less margin for error. Pericom Semiconductor Corp. provides an innovative Register and PLL portfolio for the DDR Registered DIMM market. Design, testing, and debugging is performed in-house at the factory headquarters in San Jose, California. Pericom is also quite involved in the definition of the DDRII standard being defined by the JEDEC committee.

References

- ❑ Procedure for DDR Clock Skew and Jitter Measurements, Pericom Semiconductor Corp.
- ❑ Design Guidelines for Registered DDR DIMM Module using PI74SSTV16857 Registers & PI6CV857 PLL Drivers, Pericom Semiconductor Corp.
- ❑ Migrating from FPM/EDO to SDRAM, Micron
- ❑ DDR SDRAM Registered DIMM Design Specification revision 0.9, JEDEC