Introduction
The Pericom PI7C8150 PCI-to-PCI bridge evaluation board demonstrates the bridge and allows testing of key features either before or during design / layout stages. The PI7C8150 PCI bridge complies with PCI Local Bus specification 2.2, as well as PCI bridge specification 1.1.

<table>
<thead>
<tr>
<th>SW2</th>
<th>Signal</th>
<th>Default</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>bpcce</td>
<td>Off</td>
<td>&quot;off&quot; Enables bus/power clock control function (BPCCE is high)</td>
</tr>
<tr>
<td>* 2</td>
<td>cfg66</td>
<td>Off</td>
<td>&quot;Off&quot; selects Bridge is 66 MHz capable.</td>
</tr>
<tr>
<td>3</td>
<td>p_M66en</td>
<td>Off</td>
<td>Reference board can be used in either 66 or 33 MHz motherboard slot.</td>
</tr>
<tr>
<td>4</td>
<td>s_M66en</td>
<td>Off</td>
<td>&quot;Off&quot; sets Secondary bus is 66 MHz capable (S_M66EN is high)</td>
</tr>
<tr>
<td>* 5</td>
<td>reserved</td>
<td>On</td>
<td>Reserved, this switch must be &quot;on&quot;</td>
</tr>
<tr>
<td>* 6</td>
<td>arbctrl</td>
<td>On</td>
<td>&quot;On&quot; Internal arbiter is selected</td>
</tr>
<tr>
<td>7</td>
<td>Not used</td>
<td>On</td>
<td>No effect in either position</td>
</tr>
</tbody>
</table>

1) 3 standard and one straddle mount PCI connector.
2) Pin 1 on the golden PCI edge connector faces left when looking down on the component (bridge IC).
3) Secondary bus Vio select : 3.3V or 5V
4) Headers for sampling signals on the primary PCI bus
5) GNT# and REQ# selection jumpers for the first 3 slots
6) Auxiliary power connector
7) External arbiter socket
8) Switches to set bus speed, control clocks, and some misfunctions

This board comes already configured to support:

a) Primary PCI voltage (p_VIO) can be either 3.3V or 5V keying.
b) Secondary PCI voltage is set to 3.3V at J2
c) 66 or 33 MHz primary (ie M66EN is high)
d) 66 MHz secondary if all cards on the secondary bus are 66 MHz capable (ie secondary bus M66EN is high)
e) internal arbiter and internal clock source are enabled no need to connect external power in most applications; the host PCI bus generally can power all 4 secondary bus slots.
Default and (*) important switch settings at a glance:
1) SW1 there is no SW1 
2) SW3 pin 6 must be set to ON (turns on secondary bus feedback clock signal).
3) Normally 1-5 are off. These turn off unused secondary bus clocks.

**Defaults for Jumpers**

<table>
<thead>
<tr>
<th>J1</th>
<th>not connected</th>
<th>normally, the reference board draws all power from the motherboard</th>
</tr>
</thead>
<tbody>
<tr>
<td>J2</td>
<td>jumper 2-3</td>
<td>3.3 V secondary bus VIO</td>
</tr>
<tr>
<td>J3</td>
<td>jump 2-10, 4-12, 7-15</td>
<td>assigns REQ#6 to slot 2, REQ#3 to slot 1, REQ#2 to slot 0</td>
</tr>
<tr>
<td>J4</td>
<td>jump 2-10, 4-12, 7-15</td>
<td>assigns GNT#6 to slot 2, GNT#3 to slot 1, GNT#2 to slot 0</td>
</tr>
<tr>
<td>J5</td>
<td>not connected</td>
<td></td>
</tr>
<tr>
<td>J6</td>
<td>not connected</td>
<td></td>
</tr>
<tr>
<td>J7</td>
<td>jumper 1-2</td>
<td>edge connector on primary bus supplies p_VIO</td>
</tr>
</tbody>
</table>

**Before Powering the Board**

Using the switch SW2, **choose the speed setting for the secondary bus** based upon the input primary bus speed:

<table>
<thead>
<tr>
<th>SW2</th>
<th>33/33</th>
<th>66/33 secondary</th>
<th>66/66</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>2-2 CONFG66</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>2-3 M66EN pri</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td>2-4 M66EN sec</td>
<td>On</td>
<td>On</td>
<td>Off</td>
<td>Off</td>
</tr>
</tbody>
</table>

(***Note:** When primary bus is 33 Mhz, regardless of how the bridge reference board is configured the bridge will be dynamically set to 33 Mhz primary and 33 Mhz secondary, with S_M66EN driven low by the bridge.)

Also, in the case of the **motherboard** having 5V keying and 66 Mhz at the slot connector where our card will plug in, you may choose to shift J7 jumper down by one pin to cover the center pin and J6. Where the 66 Mhz PCI slot is keyed for 3.3V, this jumper does not need to be moved.

b) **Seat the board into a PCI slot on the main system board.**
Looking from the front of the motherboard, the small lip on our reference board points to the back of the motherboard and the component side with the PI7C8150 bridge chip is on the left hand side. Normally you won’t need to connect power to the reference board through header J1, unless you are cascading bridges. Otherwise the motherboard PCI connector is adequate to powering the board with a few add-in cards.

c) **Connect any PCI cards desired on the secondary PCI bus.**
For all PCI connectors on our reference board, when looking down onto the bridge IC, pin 1 is on the left side of the board. Notice that the external arbiter socket on the front and the auxiliary power connector on the back are closest to PCI connector pin 1. This also applies to the top mounted “straddle” connector. Putting in any cards backwards will short 5V to ground through the PCI connector. Also each PCI connector has A1, B1, A62, B62 at the 4 corners of each slot, as a reminder where pin 1 is on each connector.

At this point, the Pericom PI7C8150 reference board is ready for you to use.
Switch listing
SW1: (does not exist)

<table>
<thead>
<tr>
<th>SW2</th>
<th>Signal</th>
<th>Default</th>
<th>Description</th>
</tr>
</thead>
</table>
| 1   | bpcce   | Off     | "Off" Enables bus/power clock control function (BPCCE is high)
      |         |         | "on" puts a low at this signal. (This influences turning off PCI clocks under ACPI power management.) |
| 2   | cfg66   | Off     | "Off" selects Bridge is 66 Mhz capable. |
| 3   | p_M66en | Off     | When "On" the bridge is set to 33 Mhz on both primary and secondary buses. |
| 4   | s_M66en | Off     | "Off" sets P_M66EN high. Reference board can be used in either 66 or 33 Mhz motherboard slot. |
| 5   | reserved| On      | "Off" sets Secondary bus is 66 Mhz capable (S_M66EN is high) |
| 6   | arbctrl | On      | "On" forces 33 Mhz secondary bus even if primary bus is 66 Mhz. (S_M66EN low) |
| 7   | Not used| On      | No effect in either position |

U1 Pericom 8150 bridge
U2 Philips/SigneticsN74F166-D
U3 not stuffed
U4 Philips/SigneticsN74F166-D
U6 PI3B3257-W Mux/Demux bus switch
U7 socket for optional external arbiter

SW2 speed, options selection
SW3 secondary clock control
J1 auxiliary power
J2 secondary bus Vio select
J3 Grant# selection for slots 1..3
J4 Req# selection for slots 1..3
J5 not used
J6 forces 3.3V on primary Vio
J7 primary Vio follows motherboard

TABLES:
a) Tables on the front remind shipping defaults for SW2, SW3.
b) The back side of the board has a silkscreened table of test points T1..T11 and TP9..11, TP14.
c) Right side of board has JP1, JP2, JP3 list
Normally, at power on, the 2 components U2 and U4 report which secondary PCI connectors have the PRSNTx_1 and PRSNTx_2 pins pulled low, implying there is a device at that location and it’s power requirements. Switching 1 through 5 on simply forces the unused clocks on. The Feedback clock MUST be turned on, if our bridge is generating the secondary bus clock outputs.

Jumper block listing

**J1 External Power**  
Connector.  left to right [ground, ground, ground, +3.3V, +3.3V, +5V]  
This does NOT need to be connected in order to use the bridge. *Pin 1 is +5V, pins 4-6 GND*

**J2 Vio Select** 3-2 3.3V (left) 1-2 5V (right)  
This sets Vio for the secondary bus. The PCI bridge will drive control signals to this voltage on the secondary bus. This should already be configured for you.

**J3 Grant Assignments** to secondary PCI bus connector slots 1, 2, and 3.  
The 3 ordinary PCI connectors have GNT# (and REQ#) assigned by jumpers.  
Notice that to the left of these are stenciled brackets; you may select only ONE of the possible jumper positions within a pair of brackets `[ ]`  
Thus, on our reference board, for the slot closest to the bridge, (which is mounted on the back of the board)  
\{Gnt0 OR Gnt2 OR Gnt4\}  
jump one only of these 3 choices  
we can monitor the grant signal for this slot at TP14.

For the next slot up \{Gnt1 OR Gnt3 OR Gnt5\}  
jump only 1 of the 3 choices  
Monitor at TP 11

For the third slot up \{Gnt6 OR Gnt7\}  
jump only 1 of the two choices  
Monitor at TP10

Top slot is fixed at Gnt8. Monitor at TP9

**J4 Req assignments**  
These must match the positions chosen in J3!  
From bottom slot to top,  
\{Req0 or Req2 or Req4\} monitor at TP16  
\{Req1 or Req3 or Req5\} monitor at TP15  
\{Req6 or Req7\} monitor at TP13  
fixed at Req8 top slot monitor at TP12

**J5 Not used.**

**J6 3.3V pin**  
J6 allows a method to force the bridge to use 3.3V signalling for communicating with a 66 Mhz motherboard without disturbing the motherboard’s Vio, which is only useful when an older motherboard has a 66 Mhz PCI bus keyed for 5V. *(This signal is NOT bused into the motherboard Vio.)*

**J7 P_Vio select**  
The topmost pin at J7 is P_Vio from the motherboard and the center pin goes to our bridge.

Primary bus test points JP1, JP2, JP3:  
These allow a logic analyzer or oscilloscope to monitor signals on the path between the 8150 and primary bus.  
There are 3 rows of 16 header pins each, labeled JP1, next JP2, next JP3:

(A copy of this table is present on the right hand side of the component side of the reference board.)
Test points description:
These allow convenient sampling of signals by logic analyzer or oscilloscope:

| T1  | Primary TRST GPIO   | TP1 | ground | | TP11 | Gnt to 2nd slot |
|-----|---------------------|-----|--------|| TP12 | Req to 4th (top) slot |
| T2  | Primary TCK GPIO    | TP2 | ground | | TP13 | Req to 3rd slot |
| T3  | Primary TMS GPIO    | TP3 | ground | | TP14 | Gnt to 1st (bottom) slot |
| T4  | INTA#               | TP4 | ground | | TP15 | Req to 2nd slot |
| T5  | Primary TDO GPIO    | TP5 | ground | | TP16 | Req to 1st (bottom) slot |
| T6  | Primary TDI GPIO    | TP6 | ground | |       |                   |
| T7  | INTB#               | TP7 | ground | |       |                   |
| T8  | Primary clock input | TP8 | ground | |       |                   |
| T9  | INTC#               | TP9 | Gnt to top (4th) slot | |       |                   |
| T10 | INTD#               | TP10| Gnt to 3rd slot | |       |                   |
| T11 | Primary Reset#      |     |        | |       |                   |

OPTIONAL External Arbiter:
For internal arbiter, SW2 -6 is CLOSED. This is the default.

For external arbiter, a number of changes are made to the board:
1. Remove the 0 Ohm resistors at R35, R36, R37, R38
2. Stuff 0 Ohm resistors into R121, R122, R123, R124, R127, R128
3. Verify that J4-8 (assigning REQ#0 to secondary bus slot 0) is open.
4. Instead, put the jumper at J4-7.
5. Verify that J3-8 (assigning GNT#0 to secondary bus slot 0) is open.
6. Instead, put the jumper at J3-7.
7. Finally, stuff socket U5 with an appropriately programmed Xilinx XC9572 CPLD
   (availability of code TBD)