Schematic & Board Layout Recommendations for PI7C7300

by Glenn Sanders

This application note will provide recommendations for how to connect miscellaneous signals to and from the Pericom PCI-PCI bridge. The PI7C7300 3-port PCI-PCI bridge from Pericom Semiconductor has the standard PCI signals as well as some unique control signals that might need clarification as to proper connection. In this application note we will list all of the non-standard signals and how to connect them. We will also list some recommendations for layout as exemplified by our reference board design

Miscellaneous Signal Connections

In the following table, verify that the miscellaneous signals listed are connected to the proper value:

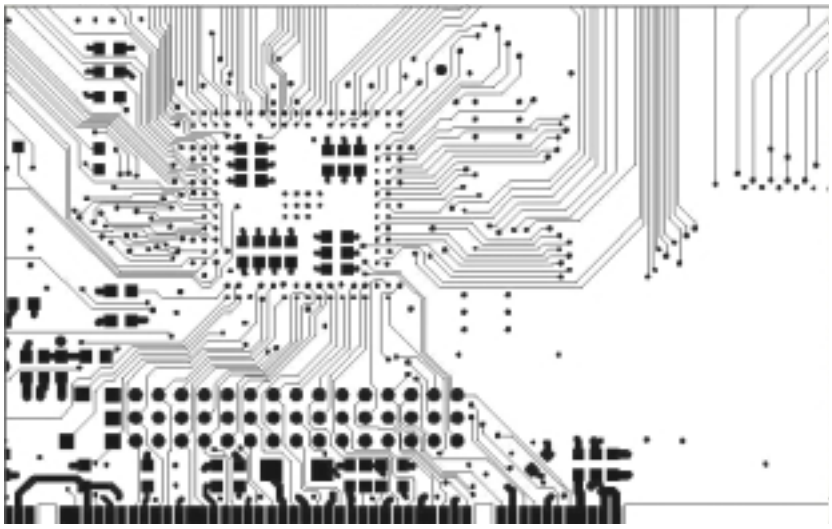
Pin name	Location	Requested Value
S2_M66EN	W5	Pull HIGH through 10 Kohm resistor
P_M66EN	V18	Pull LOW through 4.7 Kohms for 33 MHz, or leave NC for 66 MHz capable
S1_M66EN	D7	Pull HIGH through 10 Kohm resistor
BYPASS	Y4	Pull HIGH
PLL_TM	Y3	Pull LOW
S_CLKIN	V5	Pull LOW
SCAN_TM#	V4	Pull HIGH
SCAN_EN	U5	Pull LOW
HS_EN	U6	Pull to ground if no hot swap; or Pull HIGH to enable hot swap
ENUM#	R4	NC if no hot swap
S1_EN	W3	Pull HIGH
S2_EN	W4	Pull HIGH
S_CFN#	Y2	Pull LOW
HS_SW#	T2	This pin is REQ#7 for bus S2 when hot swap is not enabled (ie when pin U6 is low)
LOO	U1	This pin is GNT#7 for bus S2 when hot swap is not enable (ie when pin U6 is low) When enabled, theis pin drives directly the hot swap LED

Pin name	Location	Requested Value
JTAG pins		Internally pulled within our bridge chip
For each bus:		
LOCK#		Pull UP
PERR#		Pull UP
SERR#		Pull UP
STOP#		Pull UP
FRAME#		Pull UP
TRDY#		Pull UP
IRDY#		Pull UP
DEVSEL#		Pull UP
For each slot:		
REQ#		Pull HIGH to V_{DD} through external resistor
ACK64#		Pull UP
REQ64#		Pull UP
SDONE	(A40)	Pull UP
SBO#	(A41)	Pull UP

Where “Pull” is used, please use a 10 Kohm resistor to pull UP or 1Kohm resistor to pull DOWN.
Sixteen thermal balls J12-J9 through M12-M9: These go **directly to ground plane**. They carry no electrical signal.

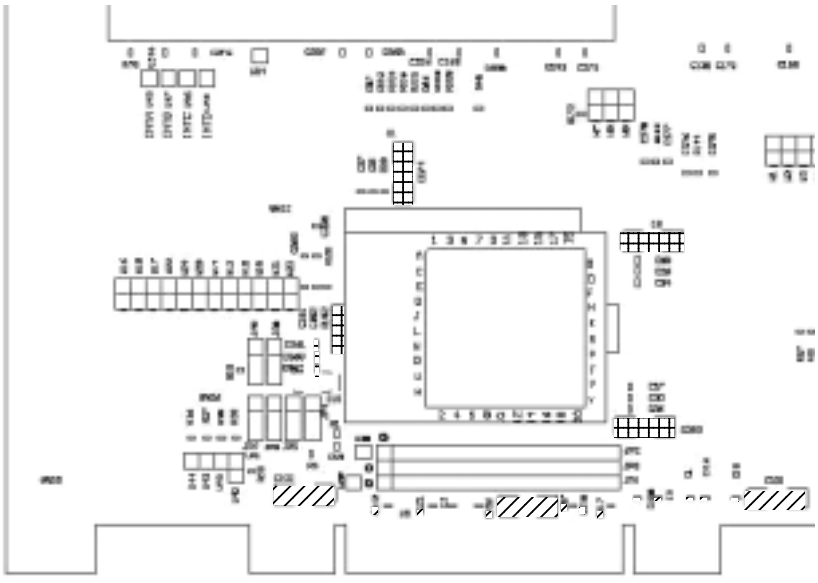
Power Decoupling

Four sets of decoupling capacitors on top and bottom sides of the PCB must be positioned as close as possible to each corner of bridge BGA. Each of the 4 corners should have values of [0.1µF, 0.01µF, 0.001µF] on bottom side of the PCB (see picture below):



Bottom layer detail showing decoupling capacitors directly under each corner of the BGA.

On top side of PCB, place four sets of four capacitors [10µF, 0.1µF, 0.01µF, 0.001µF] as close as possible to each edge of the chip. They extend decoupling at the PCI primary interface & secondary slots as needed per PCI Spec 2.2, Sec. 4.4.2.1 **"Power Decoupling."**



Top Silkscreen

Power decoupling capacitors surrounding a large mechanical socket ▦.

There are additional power decoupling capacitors at the PCI primary interface ▨.

Regarding AVDD & AGND

For an add-in card, these signals may be tied to digital V_{DD} and GND.

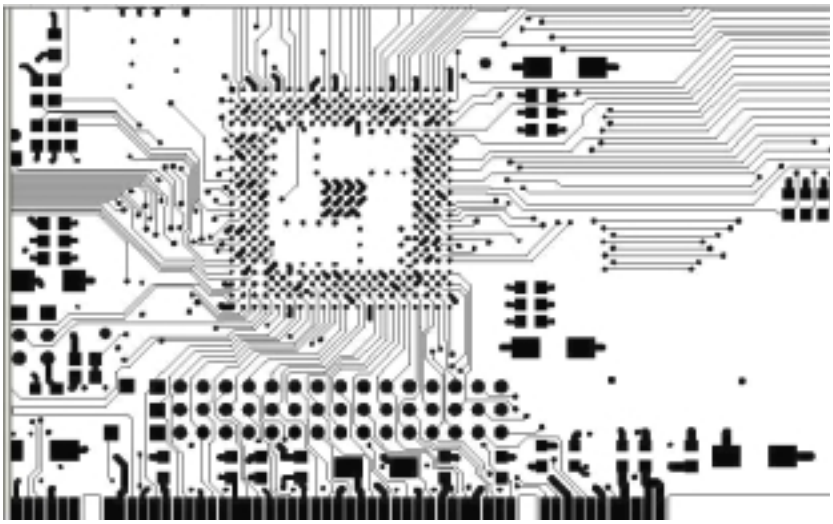
Also, please add the following decoupling capacitors at the edge connector for 3.3V and 5V pins with values [0.1µF, 0.01µF, 0.001µF].

Six Layer Board Stacking Recommendation

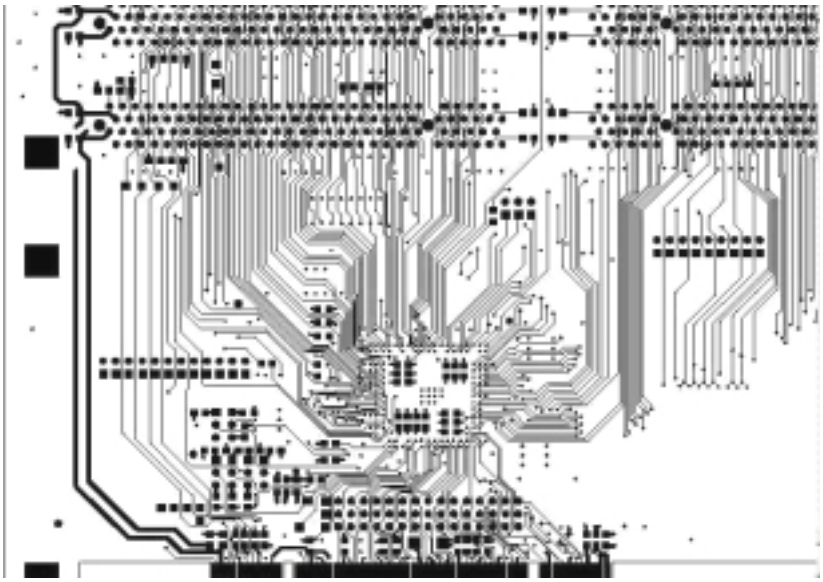
Signal layers should be seperated by ground planes with no signals routed between ground and power planes. We prefer FR-4 material. for board fabrication. Our reference board is arranged as follows:

Top	Route clock & other critical signals on top
Internal Plane 1	Ground
Internal Plane 2	3.3 V
Internal Plane 3	5 V (only needed for pass through power to 5V PCI slots)
Internal Plane 4	Ground
Bottom	Signal connections

Do NOT route high-frequency bus signals under the bridge.



Top Layer Detail: CLK signals to secondary buses; B side primary PCI bus connector. Critical control signals such as IRDY#, TRDY#, FRAME#, STOP#, etc to secondary buses.



Bottom Layer Detail: Shows traces to PCI slots: AD bus, A side primary bus connector Misc signals – JTAG, INTx, etc.

A motherboard that requires the use of analog circuitry might be arranged as follows:

Top	Route clock and other critical signals on top
Internal plane 1	Analog Ground
Internal plane 2	3.3V
Internal plane 3	5 V at PCI connectors with 3.3V AVDD island under BGA
Internal plane 4	Digital Ground
Bottom	Signal connections

General Layout Guidelines

1. Limit trace lengths. Longer traces display more resistance and induction and introduce more delays. They also limit the bandwidth which varies inversely with the square of trace length.
2. Use higher impedance traces. Raising impedance increases bandwidth. We advise 65-ohm impedance with ±10% tolerance.
3. Do not use any clock signal loops. When possible, keep clock lines straight.
4. For related clock signals that have skew specifications, match clock trace lengths.
5. Do not route signals in the ground and V_{CC} planes.
6. Do not route signals close to the edge of the PCB board.
7. Make sure there is a solid ground plane beneath the PI7C7300.
8. The power plane should face the return ground plane. No signals should be routed between power and ground.
9. Route clock signals on top layer & avoid vias for these signals. Vias change impedance & introduce more skew and reflections.
10. Do not use any connectors on clock traces.
11. Use wide traces for power and ground.
12. Keep high-speed noise sources away from the PI7C7300.
13. Remember that, per PCI spec 2.2 sec 4.4.3.1, the PI7C7300 should have a primary PCI edge connector to BGA pad trace distance of not more than 1.5 inches (37.5 mm) for signals coming from the primary PCI interface. Secondary interface signals would then be limited as in PCI motherboard layout rules.

References:

1. Pericom Semiconductor ApNote 22, "*Solutions to Current High-Speed Board Design.*"
2. PCI Local Bus Specification 2.2, Section 4.4 "*Expansion Board Specification*" [*decoupling* through *routing recommendations* and *impedence* sections] p150-152.
3. PCI Local Bus Specification 2.2, Section 4.2.6 *"Pinout Recommendation"* p131.
4. PCI Local Bus Specification 2.2, Section 4.3.3 *"Pull-ups"* p136.
5. Compact PCI PICMG 2.0 R3.0 p17-20 "*Electrical Requirements.*"

Reference schematic available at end of our PI7C7300 data book. **Gerber** and **Schematic** in electronic format available upon request.