Frequently Asked Questions on DDR Applications

by Rakesh Bhatia

1) What is the DDR clock driver?

The DDR clock driver is a 2.5v driver designed to meet the new technology needs of high-speed data transfers. The concept is that data is clocked on both the rising as well as the falling edge of the clock. This results in double data rate (DDR) transfers. Typically, the PI6C857 DDR clock driver is used in DIMM applications to distribute the system clock to SDRAMs.

2) What specs should be carefully reviewed when selecting a DDR device?

Since the entire concept of using DDR devices depends on clocking at the falling edge of the clock, the clock devices used in DDR applications must be carefully selected. Some of the specs that need to be reviewed are the half-period jitter, the reference to SDRAM skew (Phase shift) in DIMM applications (and crosspoint delta). Of these, the half-period jitter has gained increased importance due to the fact that data is clocked on the falling edge also.

3) What is half-period jitter and cycle to cycle jitter?

Half-Period Jitter is the measure of maximum change in a clock's output transition from its ideal position during one-half period. This type of jitter is considered in double data rate (DDR) transfer applications. It is measured as:

Tjit (hper) = Thalfperiod – 1/2Fo, where Fo is the frequency of the input signal. Consider a 20Mhz clock and a 25.1ns half cycle, the half-period jitter will be measured as,

Tjit(hper) = 25.1 –25 = 0.1ns (or 100ps)

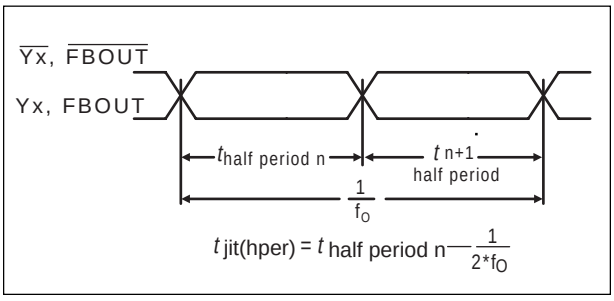

Figure 1. Half- Period Jitter.

Cycle to cycle jitter is the difference in the clock's period between 2 consecutive cycles and is expressed in units of +_ ps. This is because it can be either leading or lagging from the ideal output waveform.

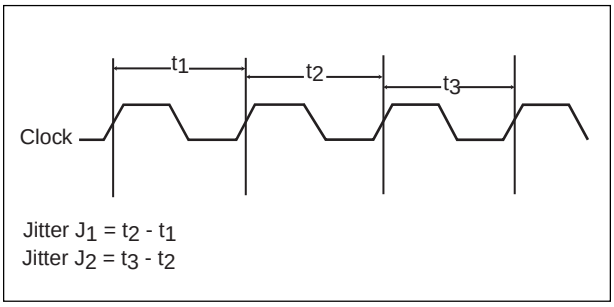

Figure 1. Cycle-to-Cycle Jitter = T2-T1, T3-T2

4) What is the importance of threshold voltage and crosspoint voltage?

In a typical DDR system that involves SDRAMs, the commands are entered on a single ended clock and data buffered is clocked on both positive and negative edges of the clock. It becomes important that the difference between the threshold of the single ended clock and the threshold of the differential clock is within a certain spec. For the differential clock this threshold is usually the crossover point. Comparatively, the threshold for the single ended clock is at VDD/2. In an effort to synchronize and correlate these 2 threshold voltages, the crossover point spec is defined as VDD/2 +-200mv.

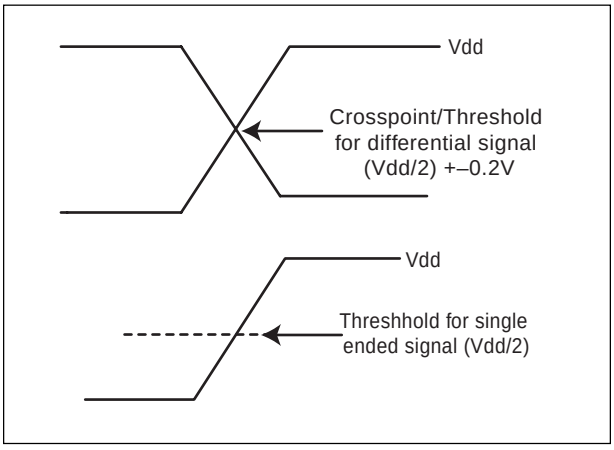

Figure 3. Crosspoint and Threshold

5) What does a typical DIMM application include?

The most common application for double data rate transfers is DIMM modules. These typically include a driver and a buffer. For high-end applications such as servers, a switch may also be used to reduce the load on the data bus. Some of the first industry's DDR products include the PI6C857; a 1:10 clock driver with low skew and low jitter. The PI74SSTV16857 is a 14-bit registered buffer designed for DDR memory applications. The PI2BV3867 switch is typically used in x8 DDR memory modules and the PI2BV3877 is typically used in the x4 DIMMs.

8) Between the different technologies or standards available such as PC133, DDR1, DDR2 and Rambus, what are the key differences?

Overall, most studies conducted on Rambus have proven it to have a comparatively lower performance with respect to DDR. Other aspects such as the difficulty to debug, price concerns have driven many different manufacturers to support DDR products. Some of the key differences are highlighted in Table 1.

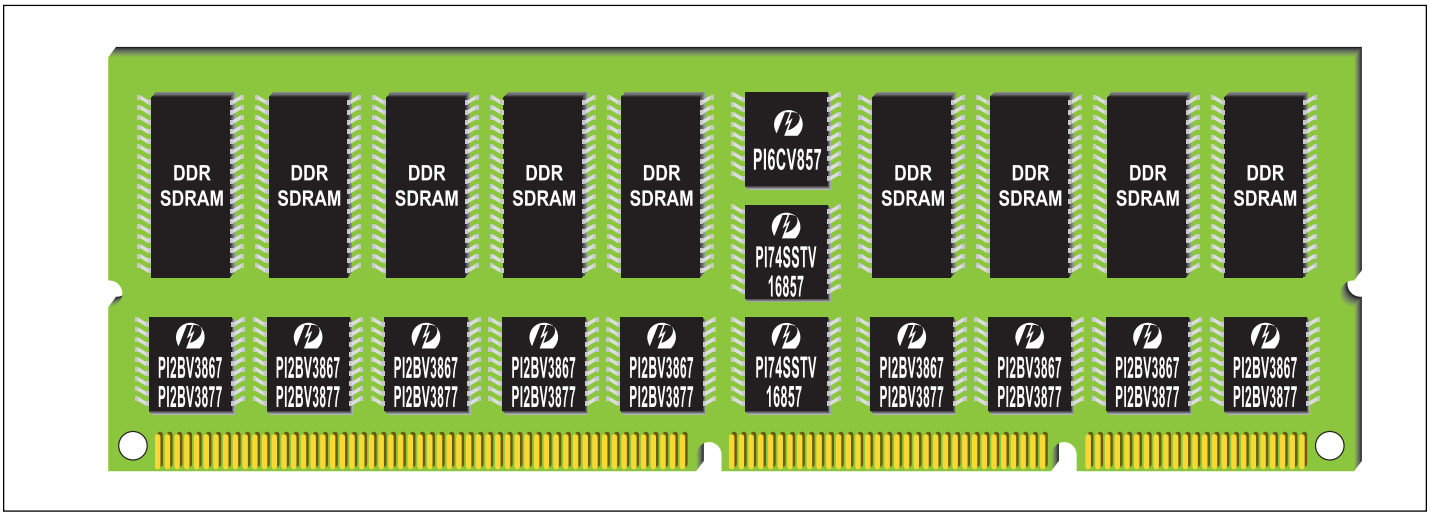

Figure 4. A Typical DIMM Module Using Pericom Parts.

6) What is the difference between the PI6C850 and the PI6C857?

The PI6C850 provides for output enable and functional control by using the I2C control interface. Using this feature, individual output pairs can be tri-stated. This feature is not offered in the PI6C857. Also, the PI6C850 is typically used in motherboard applications, whereas the PI6C857 is used in DIMMs. Both the PI6C850 and PI6C857 are PLL based devices and have almost zero propagation delay.

7) How is the time delay from Reference clock input to SDRAM tuned?

The spec for time delay from the driver's reference clock input to clock at SDRAM is 100ps. This spec is met by Pericom's PI6C857 without any external capacitor on a typical DIMM module. However certain constraints such as trace length may cause this parameter to exceed spec. Although actual values of the feedback capacitor will vary for different applications, a feedback capacitor of 3.3pf is tested and recommended for DIMM applications. For more details on terminations, please refer to Pericom's application note #22, Solution to current high-speed board design.

Table 1. Comparison Between Different Standards Available

Parameter	PC133	DDR1	DDR2	Rambus
Bus speed	133Mhz	266Mhz	532Mhz	800Mhz
Clock input	Single ended 133Mhz	Differential 133Mhz	Differential 266Mhz	Differential 400Mhz
Vdd	3.3v	2.5v	1.8v	3.3v

9) What is the Ref_in to SDRAM skew for PI6C857?

The phase shift measured on a typical DIMM module from a major manufacturer is approx. 87ps without any feedback capacitor. With a feedback capacitor value of 3.3pf, this skew is measured to be approx. 4.3ps The Jedec spec on this parameter is 200ps.

Since the skew is measured between the differential Reference input pins of the 857-clock driver and the 120-ohm resistor of the differential output pins, there is a certain amount of trace length involved. Variation in this trace length can cause the actual measured Ref_in to SDRAM skew to vary.

A more important parameter is the skew between the FBIN and clock reference pins. The PI6C857 meets the Jedec spec of 120ps on this parameter; the actual measured value of this skew is approx. 60ps.

10) How are the PI2BV3877 and PI2BV3867 different from other Pericom switches?

The PI2BV3877 and PI2BV3867 switches were specifically designed for DDR applications. Both switches offer very low capacitance and almost no propagation delay. The most common use of these switches would be in server applications where multiple cards are used. These switches provide for protection in hot swap applications by isolating the data buses.

11) How is the phase error measured in a DDR application?

Since the DDR clocks have differential inputs and differential outputs, it becomes very important to measure the phase error on differential signals. The phase error is measured from the crosspoint of the input reference signals to the crosspoint of the output signals. For example , in the Pericom PI6C857 clock driver, the phase error is measured from CK and CK/ input pins to FBIN and FBIN/ pins. Therefore, all 4 probes of a typical oscilloscope are used. Consider Figure 5 below :

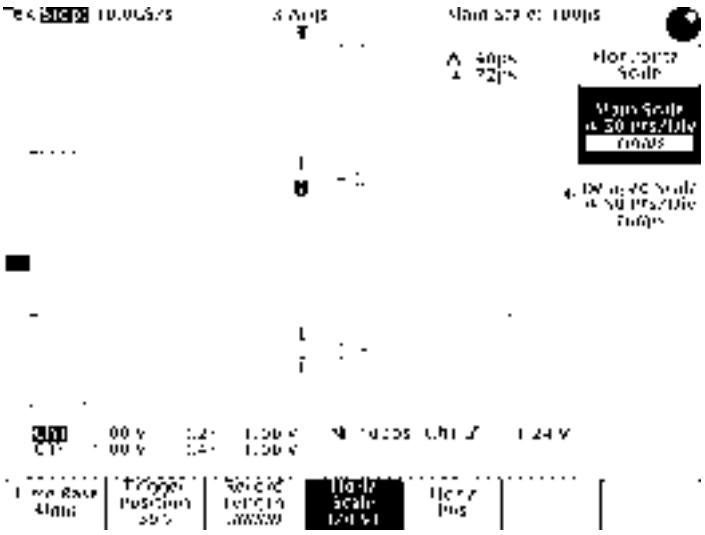

Figure 5: Measurement of phase error for typical DDR application

Here, channel 1 and 2 represents the differential input reference signal. The vertical scale is 1.00v/div and the horizontal scale is 100ps. If the crosspoints of both input and output signals are not considered, i.e. a single-ended signal measurement is done, the potential error could be as high as 100ps per volt difference and the data gathered will not be accurate. Since the phase error spec from Jedec is close to 100ps (120ps at the time this document is written); an error of 100ps is outright unacceptable.

Although there are alternate ways suggested by some vendors, most of these require averaging readings and are therefore not accurate.

12) Where can additional data on DDR parts be found?

Pericom offers a complete DDR solution, which includes clock drivers, registers and switches. For datasheets or more information on these products, please visit **www.pericom.com.**

Additional information and samples can be requested from the web site or by contacting Pericom marketing group:

Sergis Mushell for clock products at 408-435-0800 xtn 301,
and Refugio Jones at 408-435-0800 xtn 266 for switches and buffers.

Jedec specs for DDR clocks can be found at www.jedec.org

References:

1. Tisani, Mohamad, “Solution to current High-Speed Board Design.” Pericom Semiconductor Corp., AN22, 2000.
2. http://www.jedec.org/
3. http://www.inqst.com/
4. Yen, Mike, “Design guides of PC133/100 registered SDRAM module.” Pericom Semiconductor Corp., AN20, 1999.