Designing for Minimal Jitter when using PI49FCT3805D/32805 Clock Buffers

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Introduction
When designing today’s high-speed digital boards, timing margin is very low and, consequently, jitter specifications must be kept to a minimum. Some clock buffers are capable of providing jitter as low as 150ps. To achieve low jitter, strict design rules must be followed. This article provides guidelines to minimize jitter when designing with clock buffers. A good example is a dual-bank, non-inverting clock buffer (see Figure 1).

Causes of jitter in board level design:
When trying to minimize jitter, here are the real issues:
- VCC Ripple
- Propagation delay changes with VCC variation
- Threshold changes with VCC variation
- Jitter caused by cross talk interference

1. VCC Ripple
If there are no sufficient bypass capacitors on the PC board and no capacitors directly connected to the VCC pins, there could be significant VCC ripple on the VCC pins to the chip. These could be caused by the rising and falling edges of the output signals. High VCC ripple will cause high jitter that will be analyzed below.

2. Propagation delay changes with VCC Variation
The propagation delay depends on the VCC level. This means that if VCC changes, the propagation delay will also change.

The waveforms in figure 2 is captured in lab experiments with a non-inverting clock buffer (Figure 1) using common CMOS technology.

Figure 2. Simplified diagram of propagation delay versus VCC.
The input pulse at INB input pin is 44.7 MHz. The group pulses are the output measured at OB0 output pin when VCC steps up from 2.4V to 3.6V.

The waveforms in figure 2 is captured in lab experiments with a non-inverting clock buffer (Figure 1) using common CMOS technology.

Figure 2 shows that the higher the VCC, the shorter the propagation time delay. In Figure 2, the widest pulse is at the lowest VCC, 2.4V, and the narrowest pulse is at the highest, VCC, 3.6V. The propagation delay is changing with the VCC level. When the VCC voltage increases from 2.40V to 3.60V, the propagation delay difference between VCC 2.4V and VCC 3.6V is about 1.0ns to 1.2ns.

Figures 3 and 4 show how VCC ripple can cause jitter. Assuming that there are 0.8V peak to peak VCC ripples on the VCC pin, and assuming the 0.8V peak to peak VCC ripples will add about +0.4V peak to peak (see Figure 3) and –0.4V peak to peak (see Figure 4) ripples onto the VCC pin.
3. Threshold changes with \( V_{CC} \) Variation

The curve in figure 5 is the test result of the non-inverting clock buffer (figure 1) using common CMOS technology.

Figure 5 illustrates how the input threshold changes with the \( V_{CC} \) level. The threshold depends on the \( V_{CC} \) level, the higher the \( V_{CC} \) the higher the threshold.

Figure 6 shows that assuming there is a –0.60V ripple on \( V_{CC} \), the input threshold will drop from 1.50V to 1.20V. Therefore, the output rising edge at the –0.60V \( V_{CC} \) ripple will come earlier than at 3.30V \( V_{CC} \). Later, when the –0.60V \( V_{CC} \) ripple moved away, since it is random, the output will go back to normal as jitter occurs.

The –0.4V ripple added to \( V_{CC} \), when the output is falling, will make the propagation delay more than the normal propagation delay at \( V_{CC} = 3.30V \) (see Figure 4). The falling edge of the output comes later than normal. This will also make the output wider.

If the \( V_{CC} \) ripple is periodic and the ripple always occurs at the same time, it will cause the output to be skewed, but if the \( V_{CC} \) ripple is random, it will introduce jitter as opposed to skew.

If the \( V_{CC} \) ripple is a +0.4V peak to peak \( V_{CC} \) ripple on the clock rising edge, while a –0.4V peak to peak \( V_{CC} \) ripple on the clock falling edge at the same clock will double the jitter.

Propagation delay that changes with \( V_{CC} \) ripple is the main contributor to jitter. Typically, as observed in lab experiments, jitter caused by it with heavy \( V_{CC} \) ripple (0.8V peak-to-peak) could be as high as 1.5ns.
4. Jitter caused by cross talk interference

Figure 8 shows that cross talk noise causes more jitter on a slow rising edge than on a fast rising edge. The crystal’s slow edged sine wave is easier to be affected by cross talk interference.

**Suggested Solution**

To achieve low jitter, an engineer must design a board with minimal VCC ripple and cross talk interference.

**Guidelines to minimize jitter in clock application designs** (see Figure 9)

1. Use different dedicated VCC and dedicated GND layers on the PC board.
2. Use a sufficient bypass capacitor (C1) on the VCC main power connector to reduce the ripples of the VCC power source, and spread the bypass capacitors (C6, C7, C8, C9 and C10) on the surface of the PC Board.
3. Add 0.47µf and 0.047µf bypass high speed chip capacitors (C2, C3, C4, C5, or at least the 0.47µf C2 and C4) on each VCC pin of the IC chip. The combination of 0.47µf and 0.047µf capacitors was the best test result for VCC ripple in lab experiments tested with Non-inverting clock buffer (figure 1) with 150mA Icc and 44.7mhz input signal. The capacitance could be smaller with less Icc.

The shorter the trace length between the chip capacitors and the VCC pins the better. This is because it takes time for the VCC ripples to travel between the VCC pins and the chip capacitors, plus there is reflection effect which is not covered in this topic. If the trace in between is too long, there will not be enough time for the chip capacitors to absorb the high speed ripples on the VCC pin. To reduce the trace length between the capacitors and the IC pins, chip capacitors and IC chip should be on the same side of the PCB. This will minimize VCC ripple.