Designing for Minimal Jitter when using PI49FCT3805D/32805 Clock Buffers

by Paul Li

Introduction

When designing today's high-speed digital boards, timing margin is very low and, consequently, jitter specifications must be kept to a minimum. Some clock buffers are capable of providing jitter as low as 150ps. To achieve low jitter, strict design rules must be followed.

This article provides guidelines to minimize jitter when designing with clock buffers. A good example is a dual-bank, non-inverting clock buffer (see Figure 1).

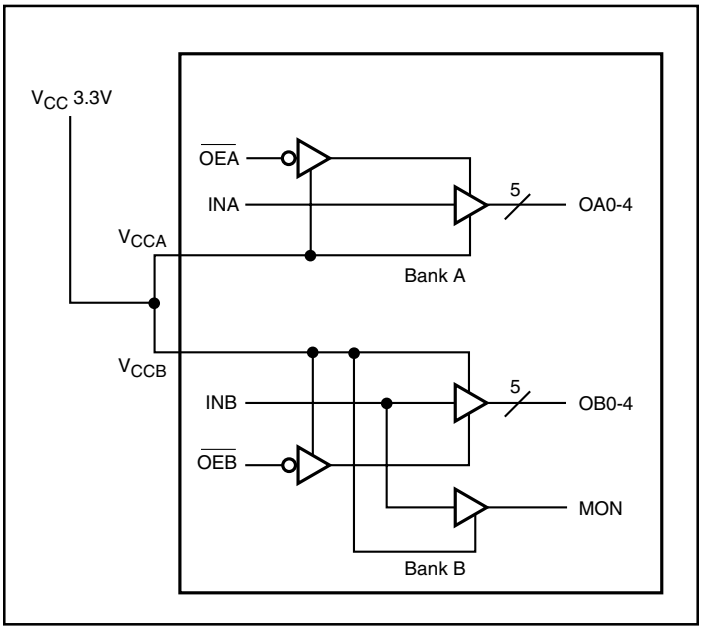

Figure 1. Non-Inverting Clock Buffer PI49FC3805D/32805

Causes of jitter in board level design:

When trying to minimize jitter, here are the real issues:

- **V_{CC} Ripple**
- **Propagation delay changes with V_{CC} variation**
- **Threshold changes with V_{CC} variation**
- **Jitter caused by cross talk interference**

1. V_{CC} Ripple

If there are no sufficient bypass capacitors on the PC board and no capacitors directly connected to the V_{CC} pins, there could be significant V_{CC} ripple on the V_{CC} pins to the chip. These could be caused by the rising and falling edges of the output signals. High V_{CC} ripple will cause high jitter that will be analyzed below.

2. Propagation delay changes with V_{CC} Variation

The propagation delay depends on the V_{CC} level. This means that if V_{CC} changes, the propagation delay will also change.

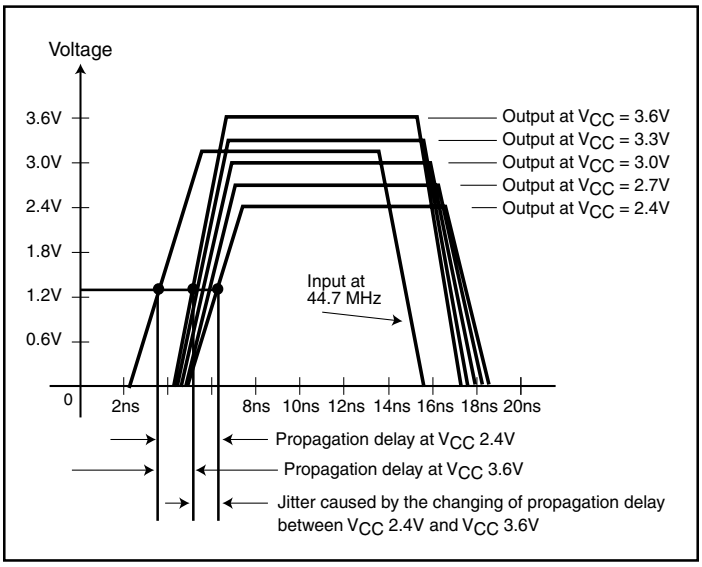

Figure 2. Simplified diagram of propagation delay versus V_{CC}. The input pulse at INB input pin is 44.7 MHz. The group pulses are the output measured at OB0 output pin when V_{CC} steps up from 2.4V to 3.6V.

The waveforms in figure 2 is captured in lab experiments with a non-inverting clock buffer (Figure 1) using common CMOS technology.

Figure 2 shows that the higher the V_{CC}, the shorter the propagation time delay. In Figure 2, the widest pulse is at the lowest $V_{CC,}$ 2.4V, and the narrowest pulse is at the highest, $V_{cc,}$ 3.6V. The propagation delay is changing with the V_{CC} level. When the V_{CC} voltage increases from 2.40V to 3.60V, the propagation delay difference between V_{CC} 2.4V and V_{CC} 3.6V is about 1.0ns to 1.2ns.

Figures 3 and 4 show how V_{CC} ripple can cause jitter. Assuming that there are 0.8V peak to peak V_{CC} ripples on the V_{CC} pin, and assuming the 0.8V peak to peak V_{CC} ripples will add about +0.4V peak to peak (see Figure 3) and –0.4V peak to peak (see Figure 4) ripples onto the V_{CC} pin.

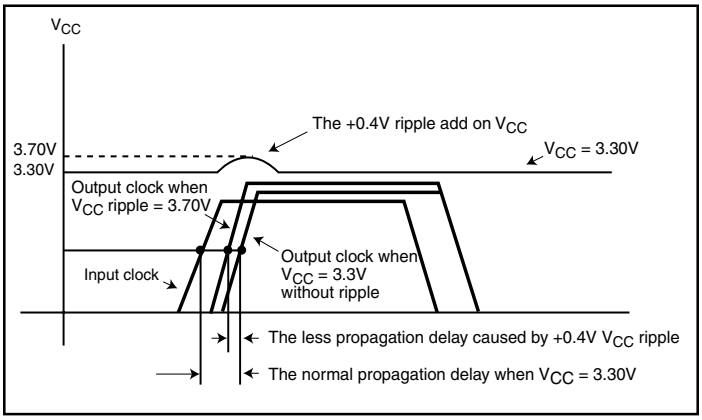

Figure 3. +0. 4V V_{CC} ripple versus output propagation delay

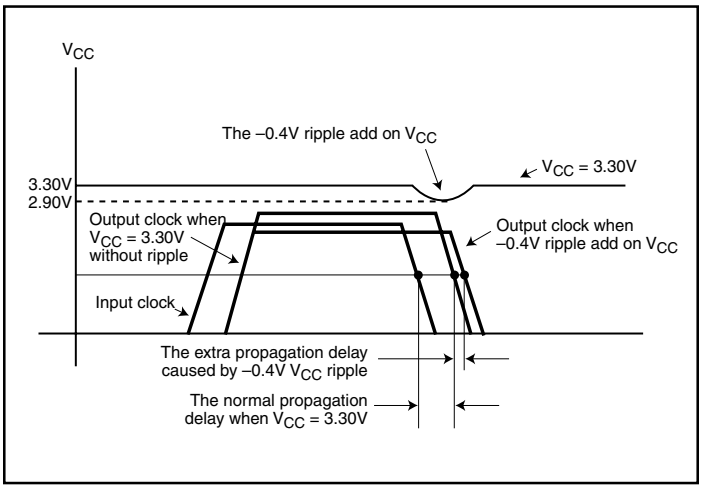

Figure 4. –0. 4V V_{CC} ripple versus output propagation delay

The +0.4V ripple on the rising edge of the output will reduce the normal propagation delay at V_{CC} = 3.3V (see Figure 3). The rising edge of the output comes earlier than normal. This will increase the output pulse width.

The –0.4V ripple added to V_{CC}, when the output is falling, will make the propagation delay more than the normal propagation delay at V_{CC} = 3.30V (see Figure 4). The falling edge of the output comes later than normal. This will also make the output wider.

If the V_{CC} ripple is periodic and the ripple always occurs at the same time, it will cause the output to be skewed, but if the V_{CC} ripple is random, it will introduce jitter as opposed to skew.

If the V_{CC} ripple is a +0.4V peak to peak V_{CC} ripple on the clock rising edge, while a –0.4V peak to peak V_{CC} ripple on the clock falling edge at the same clock will double the jitter.

Propagation delay that changes with V_{CC} ripple is the main contributor to jitter. Typically, as observed in lab experiments, jitter caused by it with heavy V_{CC} ripple (0.8V peak-to-peak) could be as high as 1.5ns.

3. Threshold changes with V_{CC} Variation

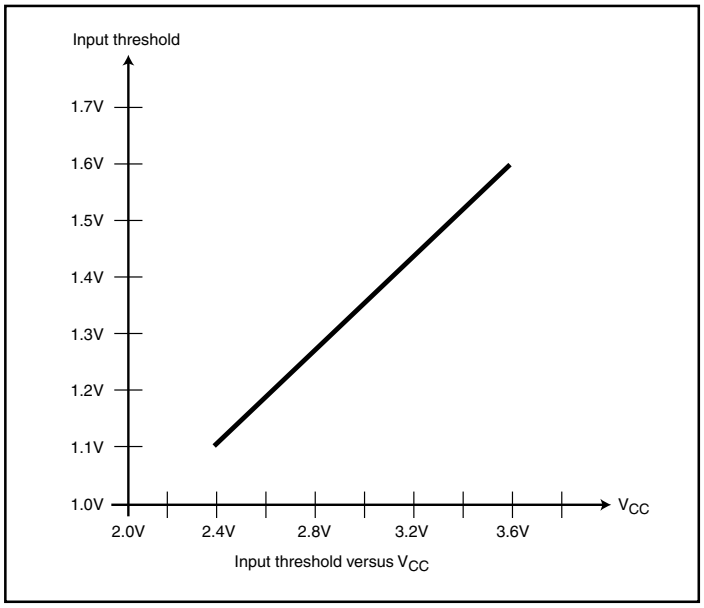

Figure 5. Threshold changes with V_{CC}

The curve in figure 5 is the test result of the non-inverting clock buffer (figure 1) using common CMOS technology.

Figure 5 illustrates how the input threshold changes with the V_{CC} level. The threshold depends on the V_{CC} level, the higher the V_{CC} the higher the threshold.

Figure 6 shows that assuming there is a –0.60V ripple on V_{CC}, the input threshold will drop from 1.50V to 1.20V . Therefore, the output rising edge at the –0.60V V_{CC} ripple will come earlier than at 3.30V V_{CC}. Later, when the –0.60V V_{CC} ripple moved away, since it is random, the output will go back to normal as jitter occurs.

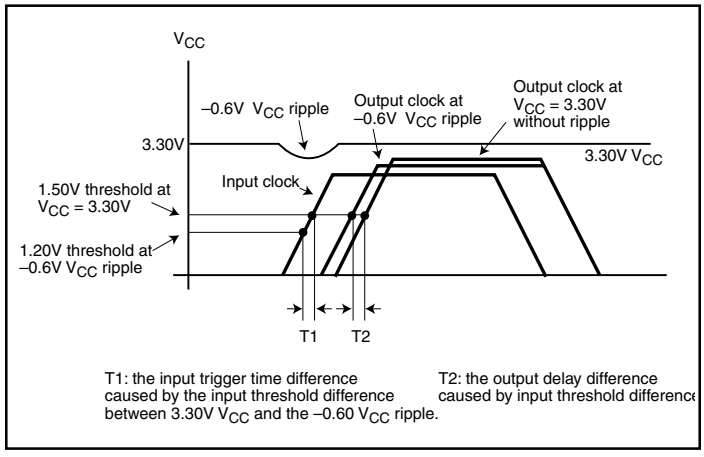

Figure 6. Jitter caused by threshold difference between 3.30V V_{CC} (without ripple) and –0.60V V_{CC} ripple

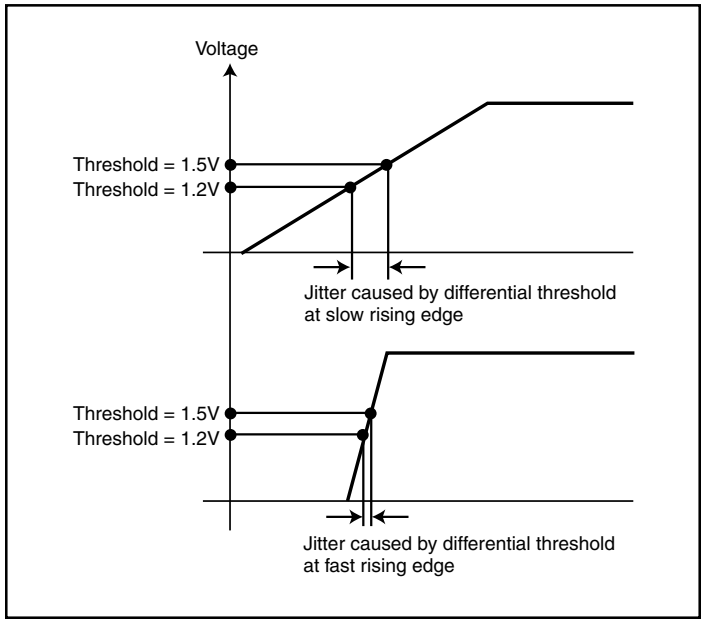

Figure 7. Jitters caused by threshold difference on slow and fast rising edges. The 1.5V threshold is at V_{CC} 3.30V; the 1.20V threshold is caused by a –0.6V V_{CC} ripple

In Figure 7, the 1.50V threshold is at V_{CC} 3.30V without ripple and the 1.20V threshold is caused by a –0.6V V_{CC} ripples. The 0.30V threshold difference between threshold at 1.5V and 1.2V generates more jitter on a slow rising edge than on a fast rising edge. The threshold difference is a much less effective vector for jitter than the changing of propagation delay as observed in lab experiments. The changing of propagation delay and the differential threshold worked together to cause jitter.

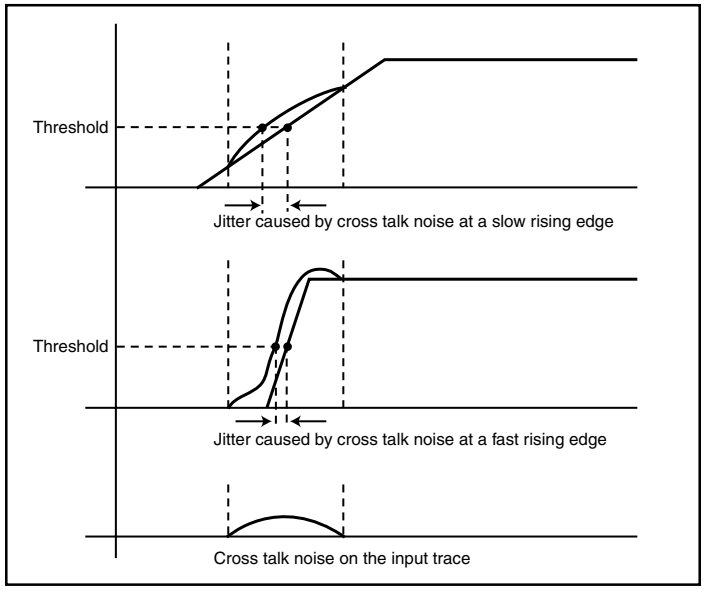

Figure 8. Jitter caused by cross talk noise on slow and fast rising edges. Overshoots are ignored.

4. Jitter caused by cross talk interference

Figure 8 shows that cross talk noise causes more jitter on a slow rising edge than on a fast rising edge. The crystal's slow edged sine wave is easier to be affected by cross talk interference.

Suggested Solution

To achieve low jitter, an engineer must design a board with minimal V_{CC} ripple and cross talk interference.

Guidelines to minimize jitter in clock application designs (see Figure 9)

1. Use different dedicated V_{CC} and dedicated GND layers on the PC board.
2. Use a sufficient bypass capacitor (C1) on the V_{CC} main power connector to reduce the ripples of the V_{CC} power source, and spread the bypass capacitors (C6, C7, C8, C9 and C10) on the surface of the PC Board.
3. Add 0.47µf and 0.047µf bypass high speed chip capacitors (C2, C3, C4, C5, or at least the 0.47µf C2 and C4) on each V_{CC} pin of the IC chip. The combination of 0.47µf and 0.047µf capacitors was the best test result for V_{CC} ripple in lab experiments tested with Non-inverting clock buffer (figure 1) with 150ma I_{CC} and 44.7mhz input signal. The capacitance could be smaller with less I_{CC}.

   The shorter the trace length between the chip capacitors and the V_{CC} pins the better. This is because it takes time for the V_{CC} ripples to travel between the V_{CC} pins and the chip capacitors, plus there is reflection effect which is not covered in this topic. If the trace in between is too long, there will not be enough time for the chip capacitors to absorb the high speed ripples on the V_{CC} pin. To reduce the trace length between the capacitors and the IC pins, chip capacitors and IC chip should be on the same side of the PCB. This will minimize V_{CC} ripple.

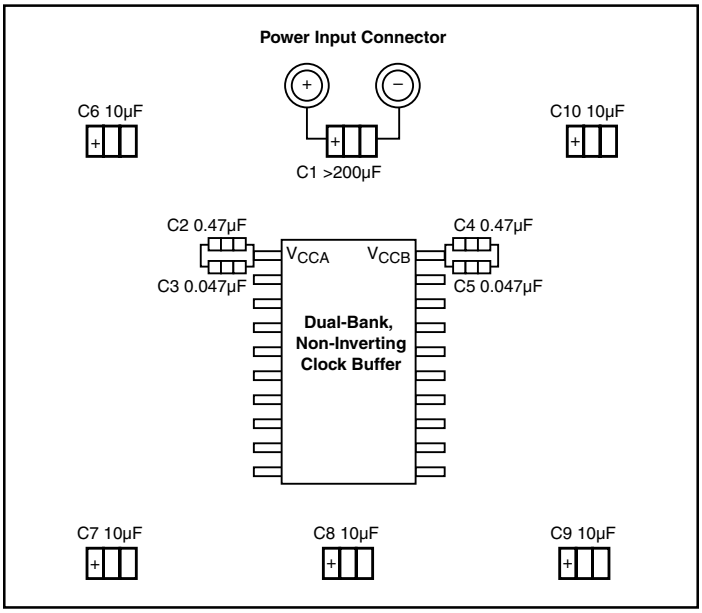

Figure 9. Example of a layout to reduce jitter