

Bus Load Isolation

Using A High Density 3.3V Bus Switch

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Introduction

Bus architectures require low capacitance loading of the bus. For example, the PCI bus requires that each load have a limit of 10pF with the maximum allowable being roughly 50pF. In multiprocessor systems, the processors can drive a high capacitance onto the bus and violate the specified limits, making it difficult for loading. Such systems require bus bridge devices that extend the number of loads without exceeding the specs. An alternative is to use fast bus switches to isolate the loads or the processors.

Application Description

To solve this problem, use Pericom's PI3B16861 3.3V, 16-bit, 2-port bus switch (see Figure 1). The device (when disabled by the bus controller) isolates access to the bus and minimizes capacitance loading. Additionally, PI3B16861's flow-through pinout makes it ideal for board mounting and routing. Alternatively, the PI3B16215 can be used in applications where its B port prebiasing can minimize hot-insertion noise. Also, the low switch propagation delay (Tpd = 0.25ns) adds no appreciable delays into the system.

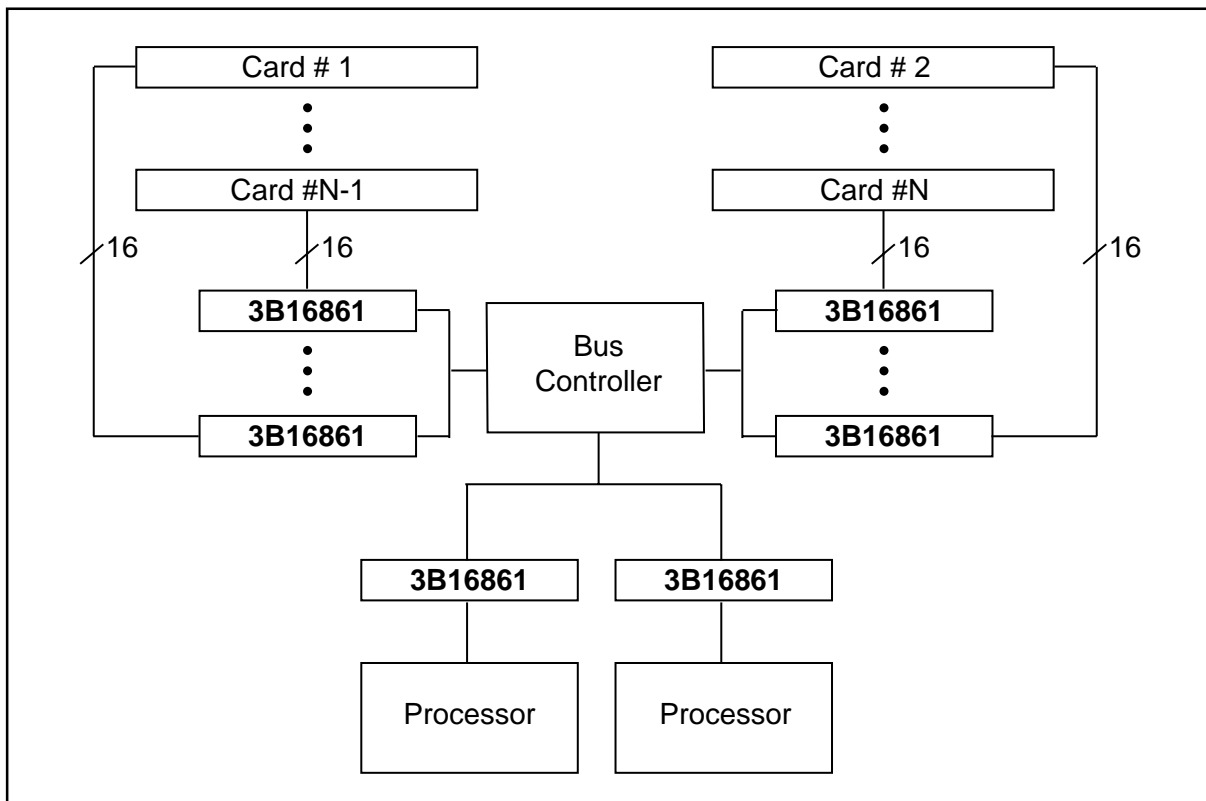


Figure 1. Using 3V Bus Switches for Bus and Load Isolation