Clock Termination Techniques

by Cameron Katrai

Introduction

Clock generation and distribution have become more difficult as the speed and performance of microprocessors increase to higher limits. Controlled and precise clocking distribution techniques are needed to maintain a synchronous system. Clock signal quality and skew are the two major problems with distributing clock signals. With higher frequencies with the associated fast edge rates, long traces behave like transmission lines. Ring back, overshoot, and undershoot occur as a result of poor termination of transmission lines. They contribute to bad signal quality, false switching, and they can cause damage in extreme cases.

Termination Techniques

There are four techniques to terminate a transmission line: Series, Parallel, Thevenin, and AC. For most TTL devices, the driver output impedance is less than the transmission line characteristic’s impedance. When such a TTL driver is driving a small number of devices, series termination is recommended. The advantage of series termination is that it is simple, consumes low power, and uses only one resistor. The disadvantage of series termination is that it increases the rise and fall times of the signal. By eliminating secondary reflection off the driver end, series termination helps with signal quality. The next three termination methods eliminate reflection at load end. Figure 1 below illustrates the series termination method. In most designs, a value of $R = 25\Omega$ to $30\Omega$ is recommended.

Thevenin termination consumes less power than parallel termination, however, it requires two resistors. Figure 3 depicts the Thevenin termination.

AC termination is shown in the figure 4 below. AC termination adds a capacitive load to the driver and delay due to RC time constant, however, it consumes low power.

Pericom Semiconductor Corporation

2380 Bering Drive • San Jose, California 95131 • 1-800-435-2336 • Fax (408) 435-1100 • http://www.pericom.com