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Diodes high speed data line ESD protector D1213A provides excellent USB2.0 protection with minimal impact on the signal integrity.

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Introduction

Minimum degradation of high-speed line's signal integrity (SI) is an important criterion when selecting the ESD protection diode for USB2.0 connected devices. This Application note provides a quick introduction to the 'eye-diagram' test which is the method of choice for many USB system designers to assess the suitability of an ESD diode. Procedure for the 'eye-diagram' test and the measurement results are then presented to demonstrate that the Diodes low-capacitance ESD diode D1213A has extremely low impact on the high speed data signals.

USB2.0 protection and signal integrity

USB ports are used on almost every modern communication or entertainment device. Even in modern cars the USB connection is used to connect portable electronics devices like music players and mobile phones to the infotainment center.

This widespread use of USB ports make them exposed to harsh conditions and the highest level of ESD protection is often just good enough to make the device survive.

In addition to providing excellent ESD protection, the ESD protector should have minimum impact on the signal integrity (SI) of the full speed USB 2.0 data transmissions during normal operating conditions.

In order to satisfy the aforementioned requirements, Diodes protection family of D1213A devices are specifically designed for USB2.0 applications with conserving signal integrity in mind.

Exceeding system level IEC 61000-4-2 Level 4 ESD protection combined with minimal impact on the signal performance of the high speed USB2.0 data lines makes it a perfect choice for a reliable, worry free system protection concept.

The many package options available will suit a wide range of application specific needs. As an example D1213A is available in the extreme small DFN1006 package (1.0x0.6 mm) or as a flow through, easy to route, USB data line protector in SOT23 package.

Eye diagram measurement

To expose any signal integrity issue in the USB data lines, the measurement method 'eye diagram', also known as 'eye pattern', is used.

The eye diagram superimposes a series of digital signal pulses that provide maximum and minimum voltage levels and signal jitter.

Figure 1: Simplified data stream

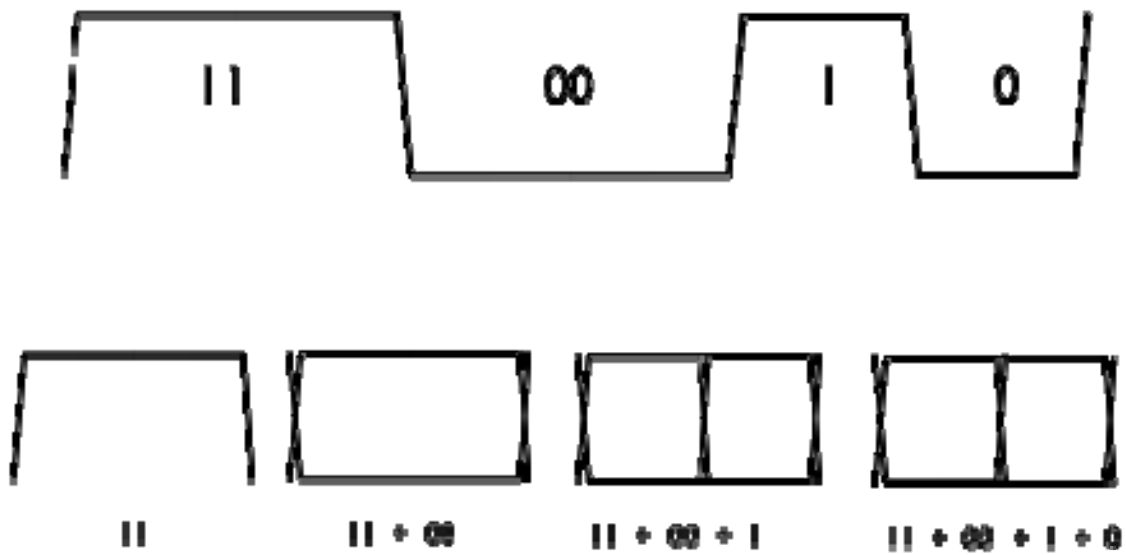
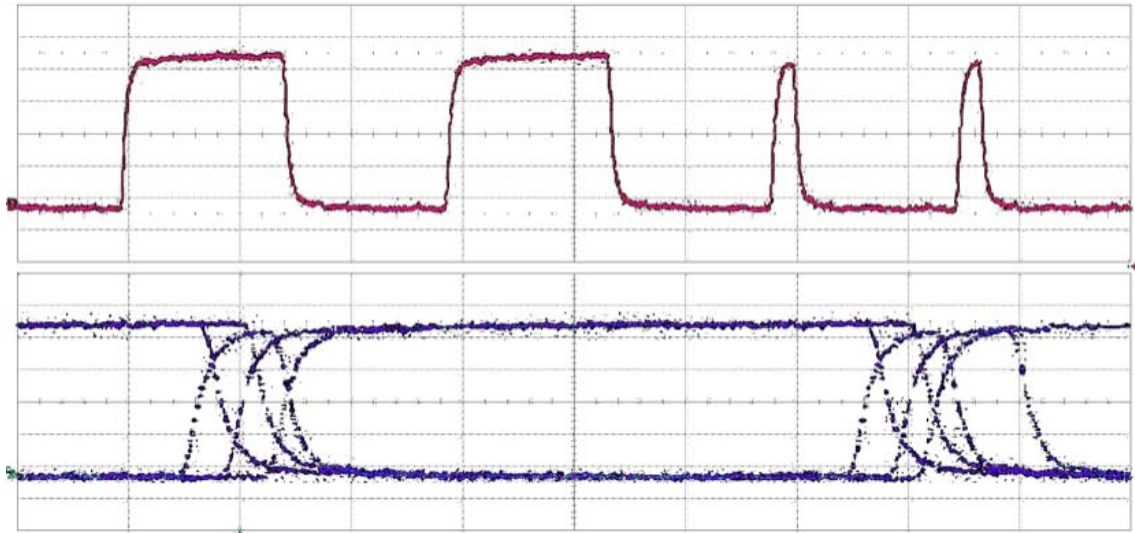


Figure 1 shows a simplified eye diagram where the eye is formed by trapezoid like pulses with flanks determined by the rise time of the pulse. No variances are visible. In reality the pulse will have different rise times and the amplitudes will have also variances due to overshoots or short pulse width.

Figure 2 shows an eye diagram that incorporates signal jitter. Extreme signal variances were used in this example to make the resulting impact on the eye-diagram more visible.

Figure 2 simple eye diagram

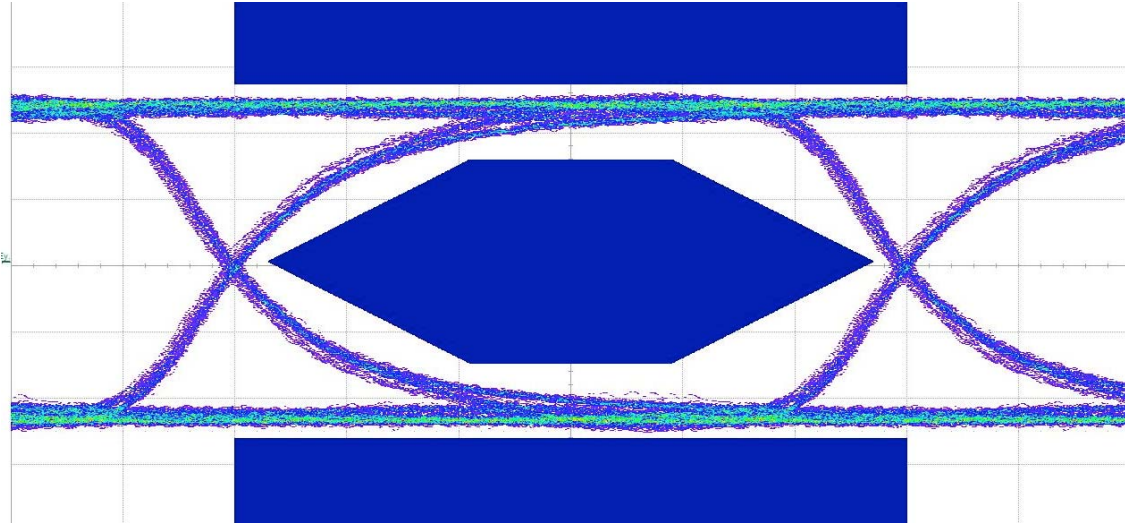


As clearly shown in the eye diagram (blue curve) the rise and fall times do differ and will result in a less defined transition area between high and low signal. The signals also have slightly different amplitude, which results in a reduction of the eye height.

Of course the above is a very simplified example for the purpose of explaining how eye diagram is build.

For real eye-diagram analysis a much longer period of the data stream is collected, consequently harvesting more bits and transitions to get a well-defined pattern.

Figure 3: Example of an USB2.0 eye diagram



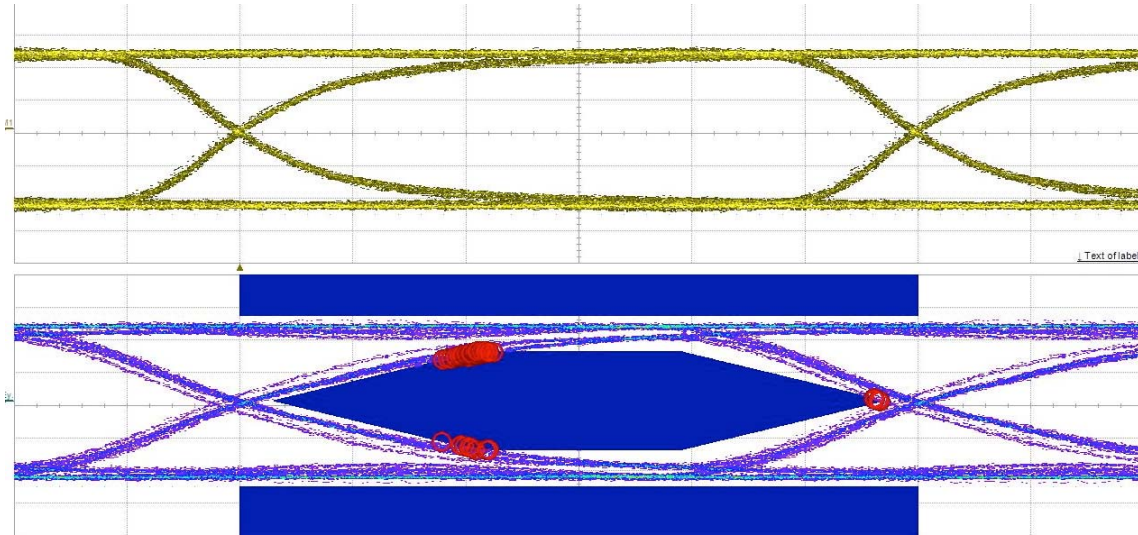
The blue geometries on top, bottom and inside the eye are called the eye-mask.

The eye-mask determines the maximum and minimum size of the acceptable eye opening for the specific protocol (here USB 2.0, full speed 12.0Mbit/s, far end).

The above simple introduction to an eye-diagram generation has the only purpose to give a first understanding of the eye diagram. For detail information please refer to the references at the end of this document.

A first order criterion is to make sure that the eye will not touch the eye mask. For demonstration purpose, the D5V0L universal bidirectional ESD clamp was mounted on the D+/D- data lines. This family of TVS product has 16pF of IO capacitance and therefore will not be suitable for USB2.0 high speed lines protection. Figure 4 shows the eye-pattern of D5V0L that fails the SI test.

Figure 4: Example of a failing eye

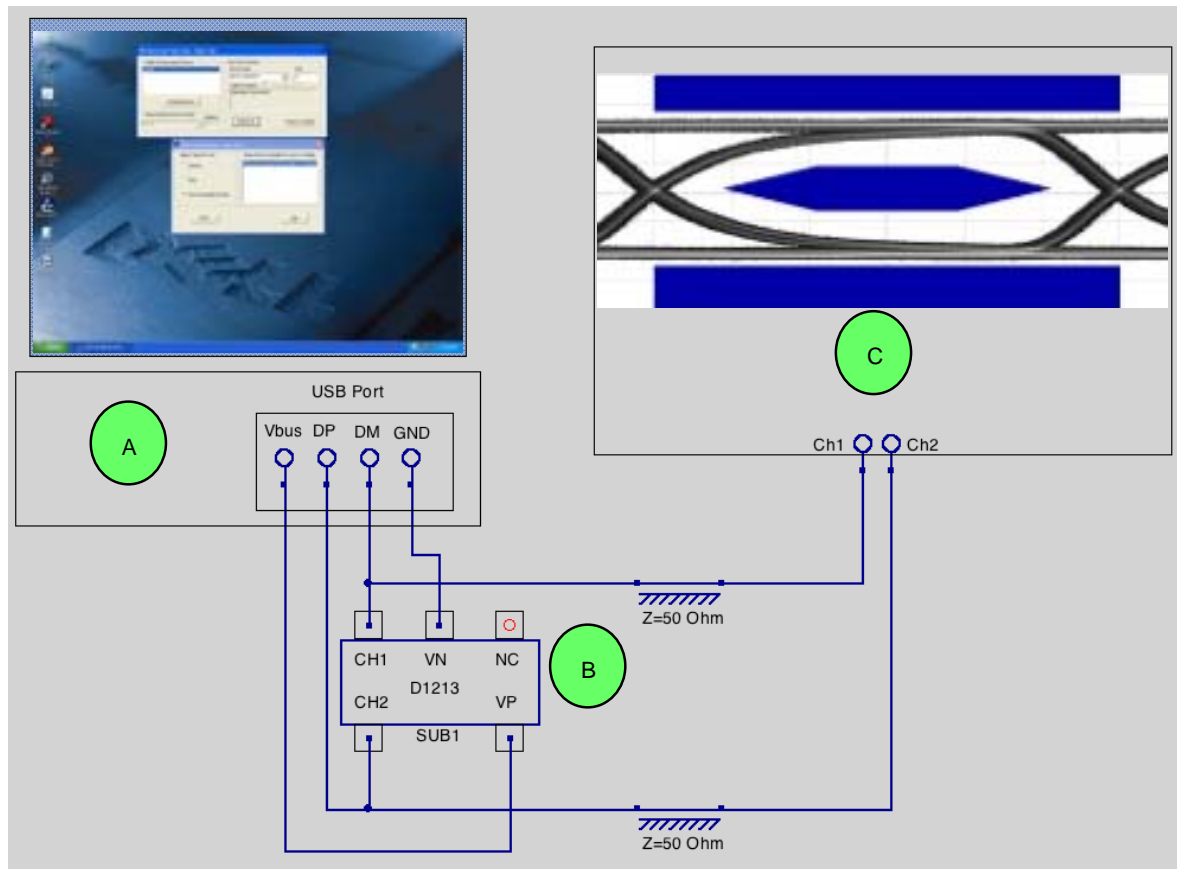


The red marker indicates where the eye diagram is touching the mask. In this case the high capacitance of the ESD device is slowing down the rising and falling edge of the signal, causing the eye to touch the flanks of the inner mask and not to reach the full amplitude of the signal.

USB2.0 Eye diagram measurements

Figure 5 shows measurement set up for capturing the eye-diagram.

Figure 5: Schematic of Setup



The EHCI HSETT software generates the test pattern, which is streamed through the USB port.



The signal is sent to the PCB where the Diodes ESD protector D1213A is mounted.



The eye diagram is an overlay of signal transitions and is generated from the differential signal lines D+ and D-

Figure 6: D+ and D- eye pattern signals

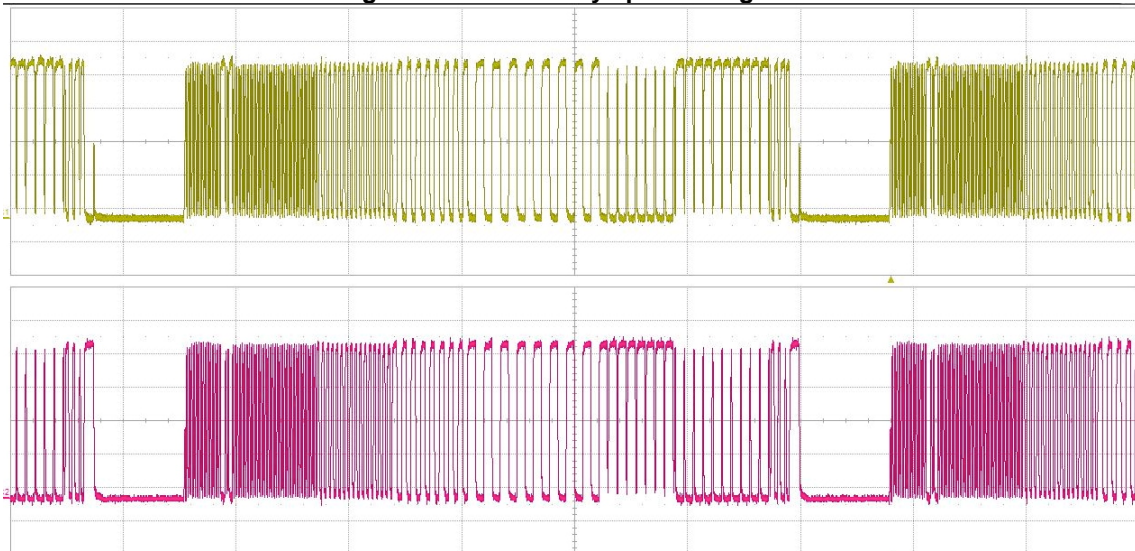


Figure 6 shows a zoomed out view of the D+ and D- pattern generated by the EHCI software during the test. Overlaying one or more of such data “packages” generates the eye-diagram.

To evaluate the influence of the D1213 ESD protector, the eye diagram measurement was done in two steps. A board without the device was first evaluated as reference. Comparing the eye patterns demonstrates the degradation caused by the ESD protection device.

Figure 7 shows the result pattern without the protection diode whilst Figure 8 shows the eye-diagram measurement with D1213A. Table 1 shows the readout of the eye-diagrams and the degradation caused by D1213A. The result shows that Diodes low capacitance ESD protection device has an extremely low impact on the USB2.0 data signals.

Figure 7: USB2.0 eye-diagram without D1213A

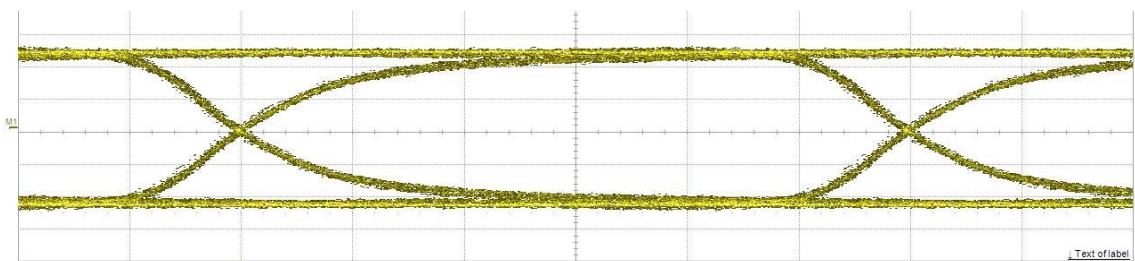


Figure 8: USB2.0 eye-diagram with D1213A protection diode

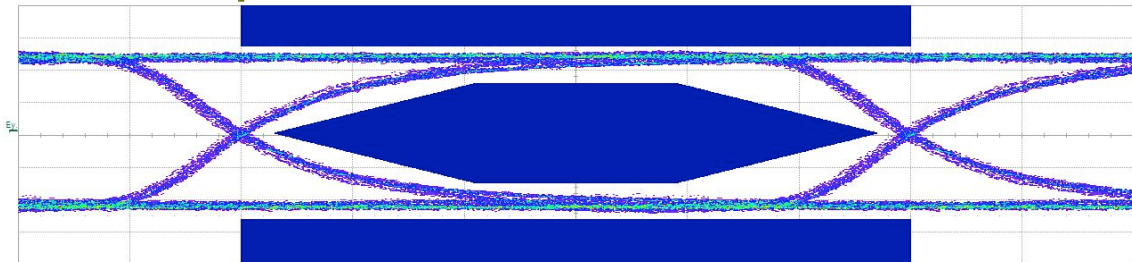


Table 1 USB2.0 eye diagram comparison

	Eye-Width	Eye-Height	Eye jitter
without D1213	1995 ns	756.9 mV	95 ps
with D1213	1980 ns	742.6 mV	99 ps
Delta (abs)	15 ns	14.3 mV	4 ps
Delta (%)	1%	2%	4%

Note:

The eye-mask in the measurement above is for “chip output” measurements. However the test setup reassembles a “far end” situation. Despite this, the eye passes still without fails.

For more details about eye mask for “far end” or “chip output” please refer to the USB 2.0 documentation available from www.usb.org.

Conclusions

This application note describes how the impact of the low-capacitance ESD protection diode D1213A on the signal integrity of the full speed USB2.0 port can be evaluated with the 'eye-diagram' test. The 'eye-diagram' evaluation result shows that the D1213A has extremely low impact on the USB2.0 data signals. This gives system and hardware designers some margin for additional capacitance on the USB2.0 lines.

Appendix

EHCI HSETT Software is available for free download from www.usb.org

The USB2.0 specification can be downloaded from www.usb.org

Simple demonstration on how an eye-diagram is generated on [YouTube](https://www.youtube.com/watch?v=...) (An eye is born)

Equipment used for eye-diagram analysis:

EHCI HSETT Software generating USB 2.0 pattern via PC USB2.0 port

Oscilloscope: Lecroy SDA 820 Zi-A

PCB board with D1213 mounted on D+ and D- lines

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