Table of Contents

65W PD3.0 Adaptor TID 605

Chapter 1. Summary

1.1 General Description

The 65W USB PD 3.0 Adaptor Evaluation Board EV1 is composed of three main parts, AP3108L PWM controller offers with high voltage soft startup circuit, a high voltage LDO makes the Vcc working range more wider, with a X-cap discharge function and a frequency fold back functional for improving Eff. The APR346 is a Synchronous Rectification Controller, as well as AP43770T16 is a USB 3.0 protocol decoder that is based on monitoring CC1 & CC2 signals and interprets the desired voltage and current requested from secondary side, and then feeds back the information to primary side AP3108L controller for getting well regulated voltage and current as well as related protection functions.

1.2 Key Features

1.2.1 System Key Features

- SSR Topology Implementation with an Opto-coupler for Accurate Step Voltage Controlling
- USB PD 3.0 Compliance
- Meet DOE 6 and CoC Tier 2 Efficiency Requirements
- <30mW No-Load Standby Power

1.2.2 AP3108L Key Features

- Current Mode PWM Controller
- Frequency Shift function changes frequency per line loading
- Frequency fold back for high average efficiency
- Integration of High-Voltage Start-Up Circuit to enable low standby power
- Integration of 120V LDO, X-Cap discharge for minimal system BOM components
- Constant load output current during output short circuit
- Rich Protection Functions: , Precise Secondary Side OVP, UVP, OLP, BNO, FOCP, SSCP, External Programmable OTP

1.2.3 APR346 Key Features

- Synchronous Rectification operating at DCM, CCM and QR mode for Flyback topology
- Eliminate Resonant Ringing Interference
- Fewest External Components used

1.2.4 AP43770T16 Key Features

- Type-C USB PD DFP (Downstream Facing Port)
- USB PD2.0, PD 3.0 Protocol Decoding
- 10-Bit ADCs for voltage and current monitoring
- Built in Shunt Regulator for Constant Voltage and Constant Current
- Programmable OVP/UVP/OCP/OTP
- Internal Discharge MOS
- Internal Vbus Load Switch Driver
- 3V- 30V Operation Voltage without External Regulator
- Package 16-Pin TSSOP
- Silicon IC USB PD3.0 PPS Compliance Certified number TID # 11090017- 07-18-2018, for power brick TID 605

1.3 Applications

- USB PD 3.0 Wall Adaptor
- USB PD 3.0 Car Charger

1.4 Main Power Specifications (CV & CC Mode)

Parameter	Value
Input Voltage	90Vac to 264Vac
Input standby power	< 30mW
Main Output Vo / Io	5V/3A, 9V/3A, 12V/3A, 15V/3A, 20V/3.25A
Efficiency	90%
Total Output Power	65W
Protections	OVP, UVP, OLP, BNO, FOCP, SSCP, OTP
XYZ Dimension	60 x 60 x 25mm
ROHS Compliance	Yes

1.5 Evaluation Board Picture

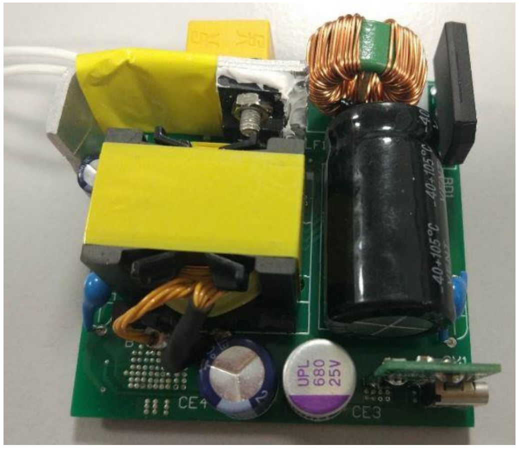


Figure 1: Top View

Figure 2: Bottom View

Chapter 2. Power Supply Specification

2.1 Specification and Test Results

Parameter	Value	Test Summary
Input Voltage	90V_{AC} to 264V_{AC}	
Input Voltage Frequency	47Hz to 64Hz	
Input Current	<1.5$A_{AC(RMS)}$	
Standby Power	<30mW; no-load	**PASS,** 26mW@230VAC/50Hz
5V Average Efficiency	DoE VI Eff >81.39%	**PASS,** 89.67% @115VAC/60Hz, 87.93% @230VAC/50Hz
	Tier2 Eff>81.84%	
5V/0.3A Efficiency (10% Load)	Tier2 Eff>72.48%	**PASS,** 82.69% @115VAC/60Hz, 80.58% @230VAC/50Hz
9V Average Efficiency	DoE VI Eff >86.62%	**PASS,** 90.87% @115VAC/60Hz, 90.05% @ 230VAC/50Hz
	Tier2 Eff>87.3%	
9V/0.3A Efficiency (10% Load)	Tier2 Eff>77.3%	**PASS,** 84.74% @115VAC/60Hz, 79.17% @230VAC /50Hz
12V Average Efficiency	DoE VI Eff >87.4%	**PASS,** 90.42% @115VAC/60Hz, 90.97% @ 230VAC/50Hz
	Tier2 Eff>88.3%	
12V/0.3A Efficiency (10% Load)	Tier2 Eff>78.3%	**PASS,** 85.44% @115VAC/60Hz, 81.32% @230VAC /50Hz
15V Average Efficiency	DoE VI Eff >87.73%	**PASS,** 90.48% @115VAC/60Hz, 90.96% @ 230VAC/50Hz
	Tier2 Eff>88.85%	
15V/0.3A Efficiency (10% Load)	Tier2 Eff>78.85%	**PASS,** 85.65% @115VAC/60Hz, 82.28% @230VAC /50Hz
20V Average Efficiency	DoE VI Eff >88.0%	**PASS,** 90.19% @115VAC/60Hz, 91.42% @ 230VAC/50Hz
	Tier2 Eff>89.0%	
20V/0.325A Efficiency (10% Load)	Tier2 Eff>79.0%	**PASS,** 85.53% @115VAC/60Hz, 83.54% @230VAC /50Hz
Conducted EMI	< 6dB Margin; according to FCC / EN55022 Class B	

2.2 Compliance

Parameter	Test conditions	Low to High	High to Low	standard	Test Summary
Output Voltage Transition time	5V/3A to 9V/3A	68ms	61ms	275mS <	Pass
Output Voltage Transition time	9V/3A to 12V/3A	49ms	56ms	275mS <	Pass
Output Voltage Transition time	12V/3A to 15V3A	44ms	48ms	275ms <	Pass
Output Voltage Transition time	15V/3A to 20V/3A	74ms	71ms	275mS <	Pass
Output Voltage Transition time	5V/0A to 20V/0A (Worst Case)	206ms	244ms	275mS <	Pass
Output Connector	USB Type C	-	-	-	
Temperature	90Vac , 20V / 3.25A @90Vac and 264Vac	-	-	-	Pass
Dimensions (W /D/ H)	L60mm x 60mm x 25mm	-	-	-	
Safety	IEC/EN/UL 60950 Standard	-	-	-	
EMI Conduction	FCC/EN55022 Class B	-	-	-	Pass

Chapter 3. Schematic

3.1 EV1 Board Schematic

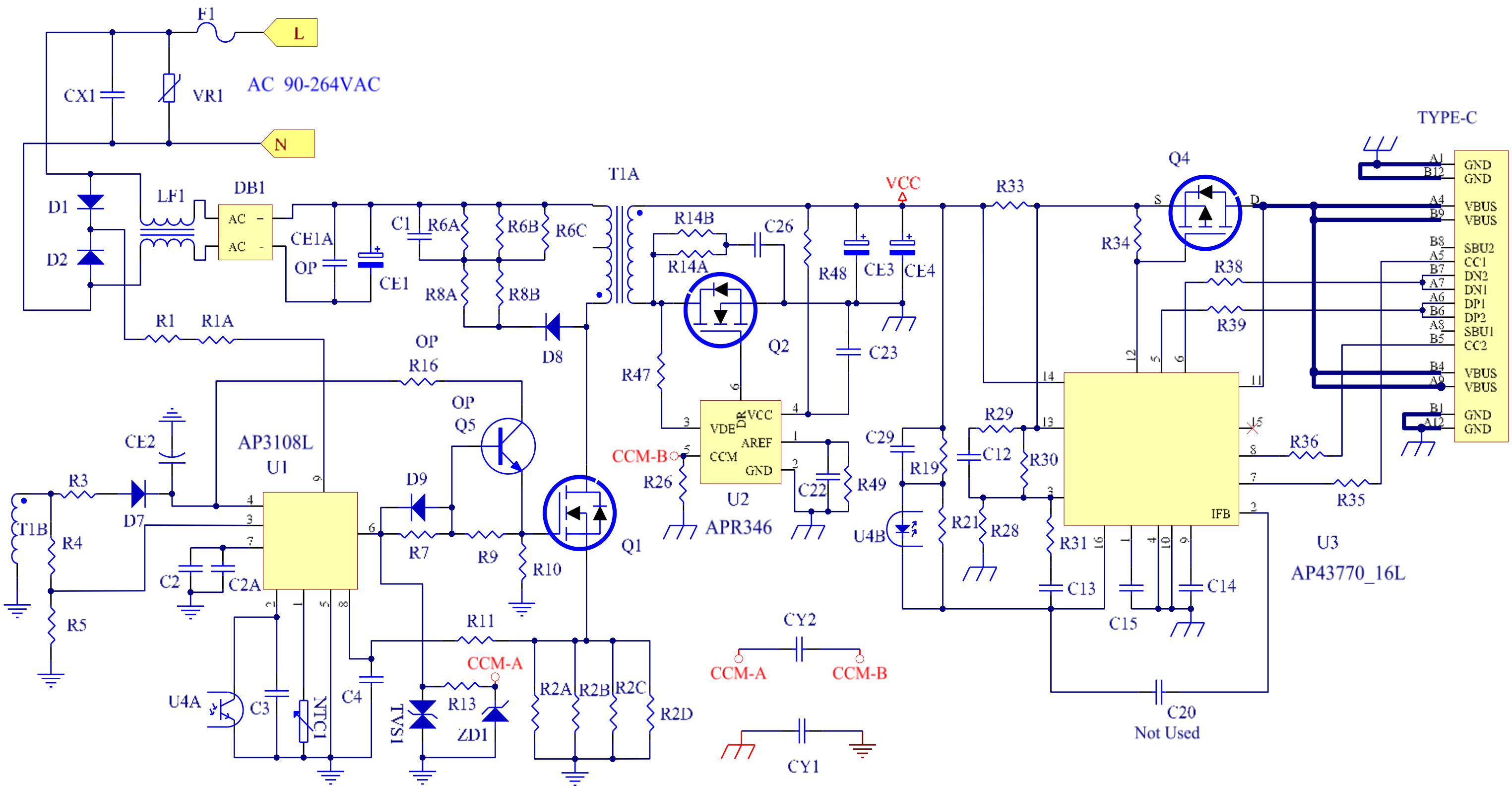


Figure 3: Evaluation Board Schematic

3.2 Bill of Material (BOM)

Designator	Description	Manufactory	Footprint	Quantity
C1	1nF/1KV	Yageo	C1206	1
C4	220pF/25V	Yageo	C0603	1
C2	6.8uF/35V	Yageo	C0805	1
C3	1.2nF/50V	Yageo	C0603	1
C26	2.2nF/200V	Yageo	C0805	1
C23,C2A	100nF/50V	Yageo	C0603	1
C22	15nF/25V	Yageo	C0603	1
C29, C12	1nF/50V	Yageo	C0603	2
C13	68nF/50V	Yageo	C0603	1
C14	100nF/25V	Yageo	C0603	1
C15	10uF/7.5V	Yageo	C0805	1
C20	Not Used		C0603	
C13A	Not Used		C0603	
C16,C17, C18,C19	Not Used		C0603	

CX1	330nF/275VAC, X-CAP			1
CY1	2.2nF/300VAC, Y-CAP		CY-10.0	1
CY2	10PF/300VAC, Y-CAP		CY-10.0	1
CE1	120UF/400V,E-CAP			1
CE2	22uF/100V,E-CAP			1
CE3	680UF/25V,Solid Cap			1
CE4	680UF/25V, E-Cap			1
T1	T-PQ2620, Lp=600uH		PQ2620	1
VR1	Varistor, '561			1
F1	T3.15A/250V			1
J1	USB TYPE-C Connector			1
LF1	Common Chock, Lp > 20mH			1
R1, R1A	10K,1206	Yageo	R1206	2
R6A, R6B,R6C	510K,1206	Yageo	R1206	3
R8A, R8B	33R,1206	Yageo	R1206	2
R9	10R	Yageo	R0603	1
R7	33R	Yageo	R0603	1
R2A, R2B, R2C,R2D	1.3R	Yageo	R1206	4
R11, R29	1K	Yageo	R0603	2
R10	47K	Yageo	R0603	1
NTC1	100K NTC Resistor		R0603	1
R3	2.2R	Yageo	R0805	1
R4	270K	Yageo	R0603	1
R5	20K	Yageo	R0603	1
R13	2K	Yageo	R1206	1
R14A, R14B	47R	Yageo	R0805	2
R47, R48, R35, R36,R38,R39	20R	Yageo	R0603	6
R49, R30	91K	Yageo	R0603	2
R26	3K	Yageo	R0603	1
R19	3K	Yageo	R1206	1
R28	10K	Yageo	R0603	1
R31, R21	4.7K	Yageo	R0603	2
R33	10mΩ/2W, ±1%	SART FUSE	R1206	1
R34	100K	Yageo	R0603	1
R16	Optional		R1206	
D1, D2, D7	**S1MWF-7**	**DIODES**	**SOD-123**	**3**
D8	**S3MB-13-F**	**DIODES**	**SMB**	**1**
D9	**1N4148WS-7-F**	**DIODES**	**SOD-323**	**1**
DB1	**GBL410**	**DIODES**	**GBL**	**1**
TVS1	**DESD1LIN2WSQ**	**DIODES**	**SOD-323**	**1**

U1	**AP3108LGSSTR-G1**	**DIODES**	**SSOP-9**	**1**
U2	**APR346K6TR-G1**	**DIODES**	**SOT23-6**	**1**
U3	**AP43770T16-13**	**DIODES**	**SSOP-16**	**1**
ZD1	**MMSZ5248B**	**DIODES**	**SOD-123**	**1**
Q2	**DMT10H010LPS-13**	**DIODES**	**POWERDI5060-8**	**1**
Q4	**DMP3007SCG-7**	**DIODES**	**DFN3*3**	**1**
Q5	**FMMT493**	**DIODES**	**SOT23**	**Optional**
U4	Photo coupler, TCLT1006	VISHAY		1
Q1	TK11A65W	TOSHIBA	TO-220	1

3.3 Transformer Design Specification

PQ2620（Ae=118mm2）							
NO	NAME	TERMINAL NO.		WINDING			
		START	FINISH	WIRE		TURNS	Layers
1	**Np1**	3（**Add Tube**）	2	Φ 0.37*2		20	2
2	**Na**	6（**Add Tube**）	5（GND）	Φ 0.18*2		15	1
3	**Ns1**	A	B	Φ 0.45TIW *2 （**Triple Insulated Wire**）		6	1
4	**Ns1**	A	B	Φ 0.45TIW *2 （**Triple Insulated Wire**）		6	1
5	**Shield2**	3	NC	Φ 0.14*1		28	1
6	**Np2**	2	1(Add Tube)	Φ 0.37*2		20	2

Primary Inductance	Pin 3-1,all other windings open, measured at 20kHz, 0.4VRMS	600µH±5%
Primary Leakage Inductance	Pin 3-1, all other windings shorted, measured at 20kHz, 0.4VRMS	20µH (Max.)
Note	1，Core connect to Pin5 2，Core：PC40	

3.4 Schematics Description

3.4.1 AC Input Circuit & Differential Filter

There are three components in this section. The Fuse F1 protects against over-current conditions which occur when some of the main components fail. The LF1 & CX1 are common mode choke filters for the common mode noise suppression filtering due to each coil with large impedance. The DB1 is a AC-DC rectifier, and converts alternating current & voltage into direct current & voltage.

3.4.2 AP3108L PWM Controller

The AP3108L PWM controller U1 and Opto-Coupler U4 as well as Q1 are the power converting core components. Connected to filtered output after bridge circuit, R1 & R1A resistor path will provide start-up voltage and current during starting up through HV (Pin 9). Subsequent VCC power will be provided by voltage feedback from the auxiliary winding through R3 and D7. This design is to accommodate the required wide voltage range to support various protocols (including USB PD Programmable Power Supply PPS), from 5V to 20V.

Based on feedback of secondary side (Pin CATH of AP43770T16 Decoder) to primary side (FB pin of AP3108L) by through Opto-coupler U4, the AP3108L will switch ON and Off Q1 to regulate the desired voltage and current on the secondary side.

3.4.3 APR346 Synchronous Rectification (SR) MOSFET Driver

The APR346 operates in CCM/DCM mode in this design and drives the Q2 MOSFET. As the power loss with the APR346-controlled MOSFET Q2 is less than Schottky Diodes, the total efficiency can be improved.

3.4.4 AP43770T16 PD3.0+ Decoder & Protection on /off P MOSFET and Interface to Power Devices

The few sets of important pins provide critical protocol decoding and regulation functions in AP43770T16:

1) **CC1 & CC2 (Pin 7, 8)**: CC1 & CC2 (Configuration Channel 1 & 2) are defined by the USB PD spec to provide the channel communication link between power source and sink devices.

2) **Constant Voltage (CV)**: The CV is implemented by sensing VCC (pin 13) via resistor divider and comparing with internal reference voltage to generate a CV compensation signal on the CATH pin (pin 16). There is a loop compensation circuit C13 & R31 between Pin3 & Pin16, the fast voltage response can be obtained by adjusting their value. The output voltages can be adjusted by firmware programming.

3) **Over current protection (OCP)**: The OCP is implemented by sensing via current sense resistor (R33, 10mΩ) and current sense amplifier, then comparing with internal programmable reference voltage to generate a signal on CATH pin (pin 16).

4) **CATH (Pin 16)**: It is the key interface that links secondary decoder (AP43770T16) to primary PWM regulation controller (AP3108L), through the Cath pin to Opto-coupler U4A link that will feed all information based on all sensed CC1 & CC2 voltage status signals back to primary PWM controller for getting desired Vbus voltage & current.

5) **GATE Driver (Pin 12) to PMOSFET Gate**: The pin is used to turn on/off Vbus load switch (Q4) to enable/disable voltage output to the Vbus. An extra PMOSFET (Q4) is required to prevent reverse current from the attached battery source.

Chapter 4. The Evaluation Board (EVB) Connections

4.1 EVB PCB Layout

The thickness for both sides of PCB board trace copper is 2 oz.

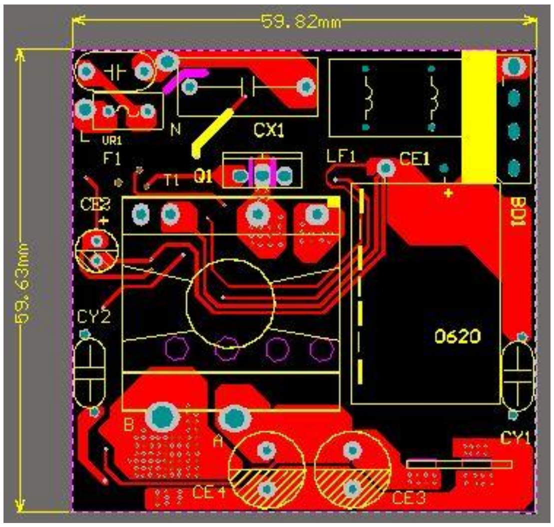


Figure 4: PCB Board Layout Top View

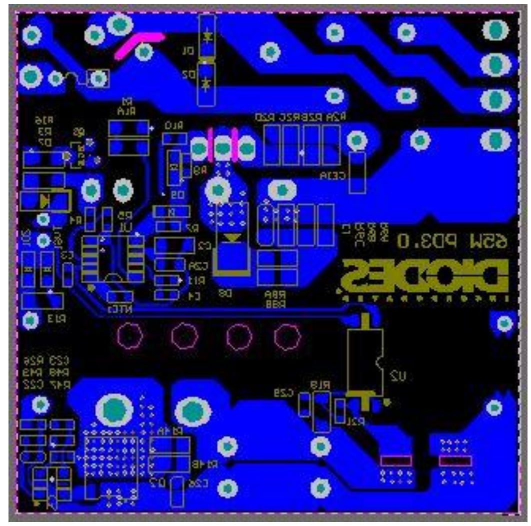


Figure 5: PCB Board Layout Bottom View

4.2 Quick Start Guide before Connection

1) Before starting the 65W EVB test, the end user needs to prepare the following tool, software and manuals.

   For details, please consult USBCEE sales through below link for further information.

   USBCEE PD3.0 Test Kit: USBCEE Power Adapter Tester. https://www.usbcee.com/product-details/4

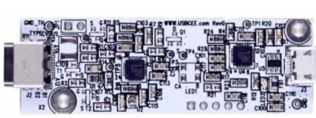
USBCEE PAT Tester	GUI Display	USB-A to Micro-B Cable	Type-C Cable
			

Figure 6: Items: Test Kit / Test Cables

2) Prepare a certified three-foot Type-C cable and a Standard-A to Micro-B Cable.
3) Connect the input AC L & N wires to AC power supply output “L and N“ wires.
4) Ensure that the AC source is switched OFF or disconnected before the connection steps.
5) A Type-C cable for the connection between EVB’s and Cypress’s Type-C receptacles.
6) Use 2 banana jack cables, one port of the cables are connected to E-load + & - terminals while the other port of the cables are connected to EVB’s VBUS & GND pads.

7) A Standard-A to Micro-B cable to be connected to the Cypress test kit's Micro-B receptacle & PC Standard-A receptacle respectively.

4.3 System Setup

4.3.1 Connection with E-Load

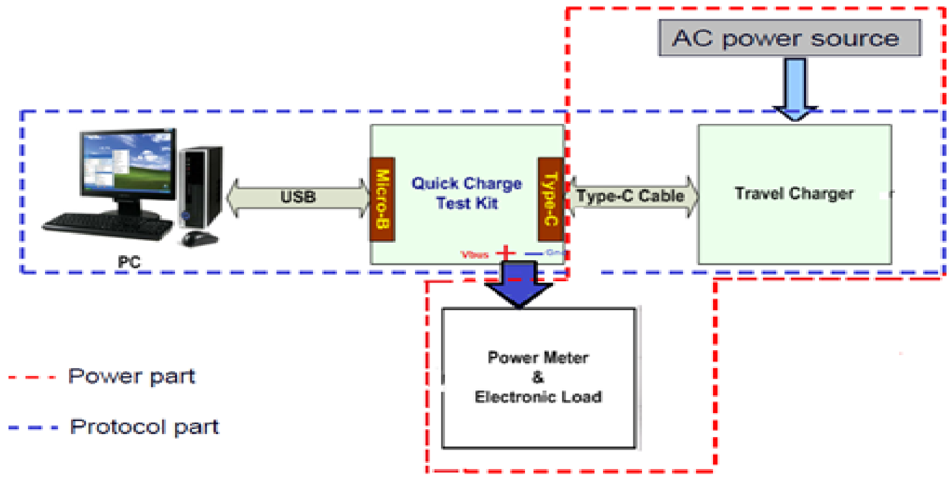


Figure 6: Diagram of Connections in the Sample Board

4.3.2 USBCEE PAT Tester

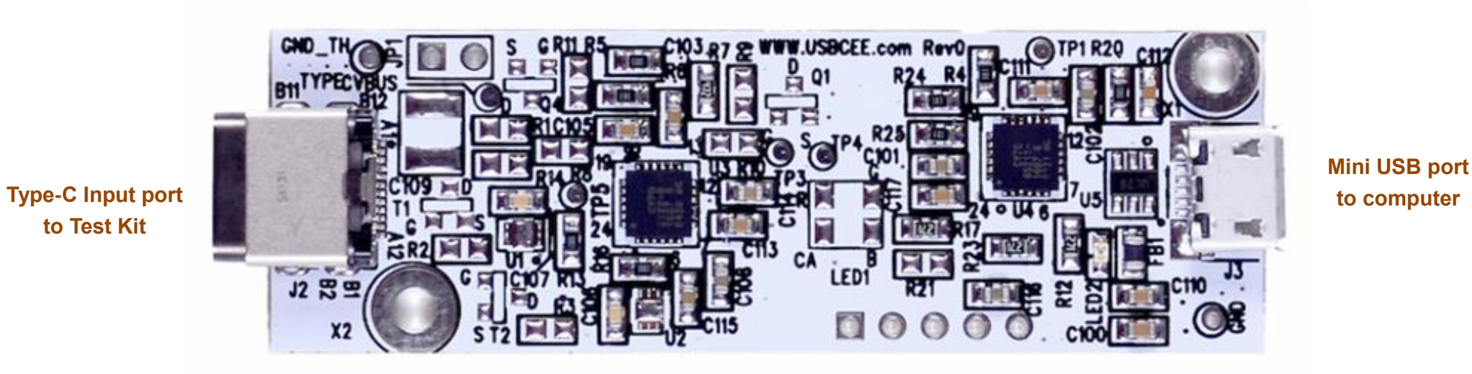


Figure 7: The Test Kit Input & Output and E-load Connections

4.3.3 Input & Output Wires Connection

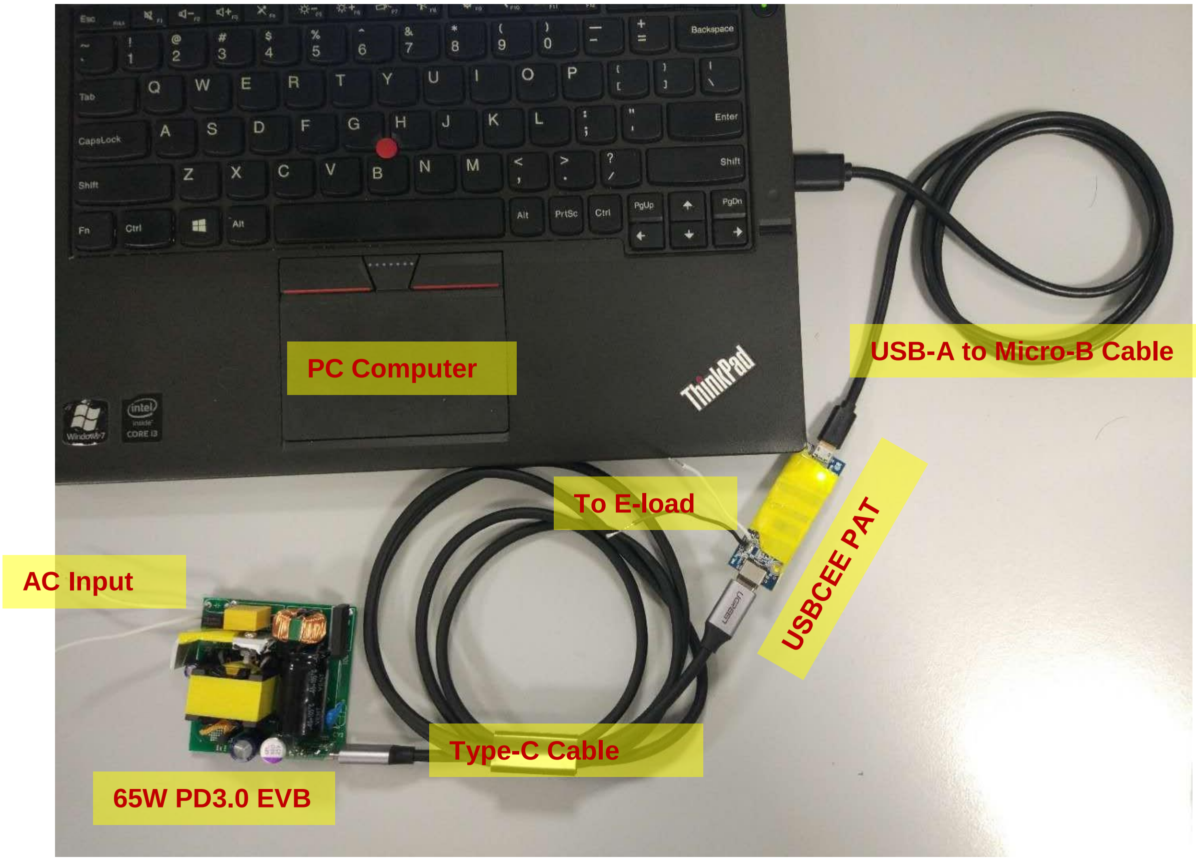


Figure 8: Wire Connection of 65W PD3.0 EVB to Test Kit and PC Computer

Chapter 5. Testing the Evaluation Board

5.1 Input & Output Characteristics

5.1.1 Input Standby Power

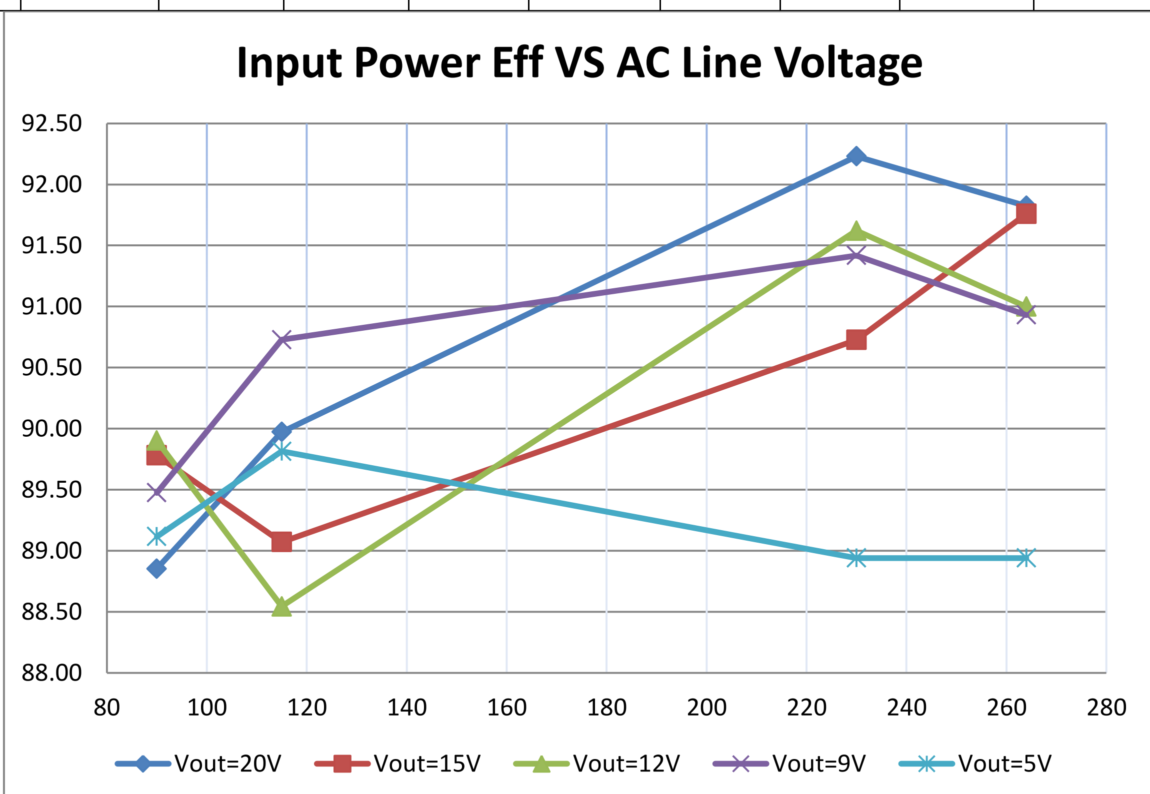
Output Voltage	Input Voltage	Standby Power (mW)
5V @ No Load	115Vac 60HZ	19
	230Vac 50HZ	27

Note:

Standard Power test condition: The output terminal of power board don't connected any load

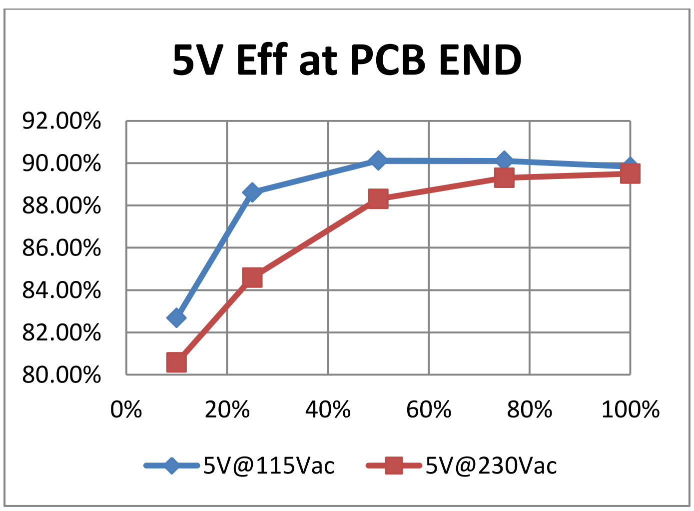
5.1.2 Input Power Efficiency at Different AC Line Input Voltage and its chart curve

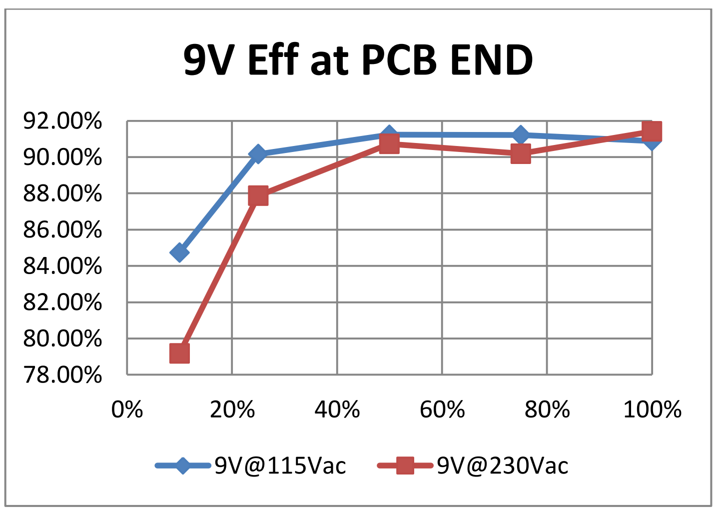
Vin （Vac）	Freq （HZ)	Vin （V）	Iin （A）	PF	Pin （W）	Vout （V）	Iout （A)	Pout （W）	Pd （W）	Eff （%)
90	47	89.99	1.42	0.59	75.03	20.5	3.252	66.67	8.364	88.85
115	60	115.1	1.26	0.51	74.1	20.501	3.252	66.67	7.431	89.97
230	50	230.34	0.75	0.40	72.3	20.505	3.252	66.68	5.618	92.23
264	63	264.22	0.68	0.39	72.63	20.508	3.252	66.69	5.938	91.82
90	47	89.99	1.03	0.55	51.86	15.479	3.008	46.56	5.299	89.78
115	60	115.1	0.954	0.50	52.27	15.478	3.008	46.56	5.712	89.07
230	50	230.35	0.543	0.39	51.31	15.476	3.008	46.55	4.758	90.73
264	63	264.33	0.396	0.39	50.73	15.475	3.008	46.55	4.181	91.76
90	47	90.02	0.859	0.53	41.74	12.475	3.008	37.52	4.215	89.90
115	60	115.12	0.784	0.47	42.38	12.475	3.008	37.52	4.855	88.54
230	50	230.35	0.441	0.40	40.96	12.476	3.008	37.53	3.432	91.62
264	63	264.32	0.399	0.38	41.24	12.476	3.008	37.53	3.712	91.00
90	47	90.04	0.7	0.52	31.84	9.471	3.008	28.49	3.351	89.47
115	60	115.14	0.604	0.46	31.4	9.471	3.008	28.49	2.911	90.73
230	50	230.37	0.34	0.37	31.16	9.47	3.008	28.49	2.674	91.42
264	63	264.33	0.31	0.38	31.33	9.471	3.008	28.49	2.841	90.93
90	47	90.08	0.452	0.50	18.47	5.472	3.008	16.46	2.010	89.12
115	60	115.17	0.359	0.43	18.33	5.473	3.008	16.46	1.867	89.81
230	50	230.4	0.211	0.36	18.51	5.473	3.008	16.46	2.047	88.94
264	63	264.33	0.192	0.36	18.51	5.473	3.008	16.46	2.047	88.94

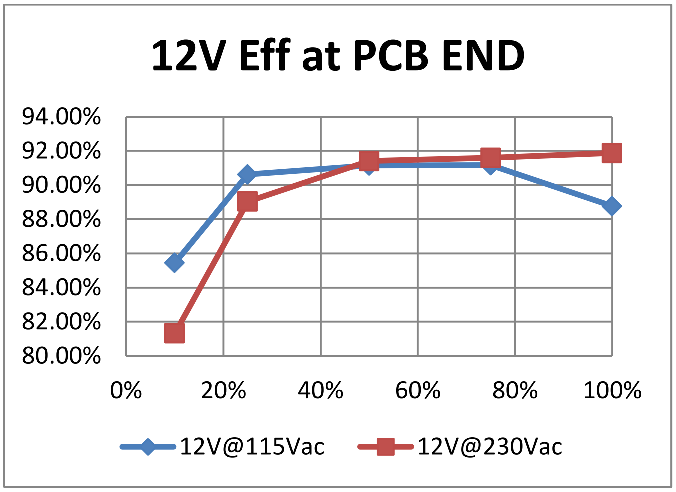


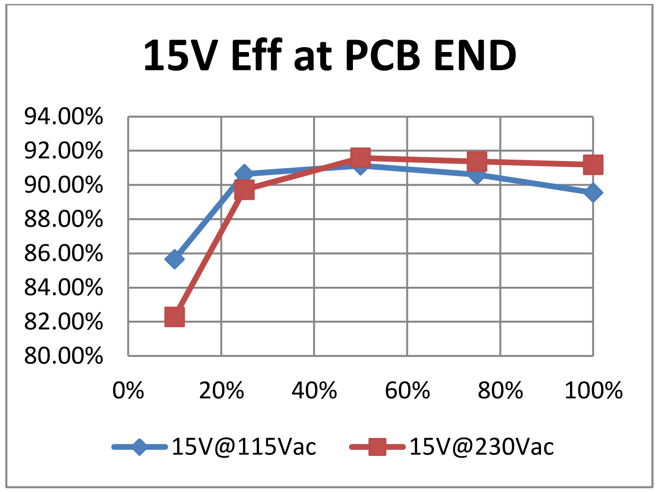
5.1.3 Average Efficiency at Different Loading (@ PCB end) and its chart curve

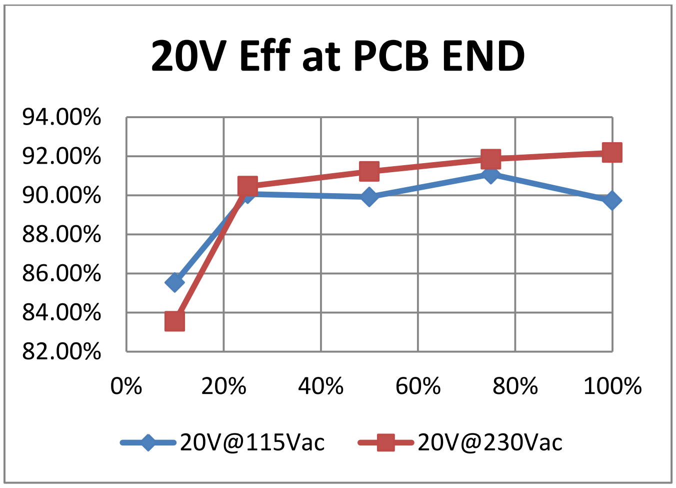
Vin	Vo	25% Load	50% Load	75% Load	100% Load	**Average Efficiency**	Energy Star Level VI	COC_Tier2	10% Load Efficiency
115V/60Hz	5V-3A	88.62%	90.12%	90.11%	89.83%	**89.67%**	>81.39%	>81.84%	82.69%
	9V -3A	90.16%	91.23%	91.21%	90.89%	**90.87%**	>86.62%	>87.30%	84.74%
	12V3A	90.62%	91.14%	91.16%	88.76%	**90.42%**	>87.40%	>88.30%	85.44%
	15V-3A	90.64%	91.13%	90.60%	89.55%	**90.48%**	>87.73%	>88.85%	85.65%
	20V-3.25A	90.06%	89.91%	91.07%	89.72%	**90.19%**	>87.73%	>88.85%	85.53%
230V/50Hz	5V-3A	84.60%	88.31%	89.31%	89.50%	**87.93%**	>81.39%	>81.84%	80.58%
	9V -3A	87.87%	90.73%	90.19%	91.42%	**90.05%**	>86.62%	>87.30%	79.17%
	12V3A	89.03%	91.40%	91.59%	91.87%	**90.97%**	>87.40%	>88.30%	81.32%
	15V-3A	89.72%	91.58%	91.37%	91.18%	**90.96%**	>87.73%	>88.85%	82.28%
	20V-3.25A	90.46%	91.21%	91.84%	92.18%	**91.42%**	>87.73%	>88.85%	83.54%











5.2 Key Performance Waveforms

5.2.1 65W PD3.0 System Start-up Time

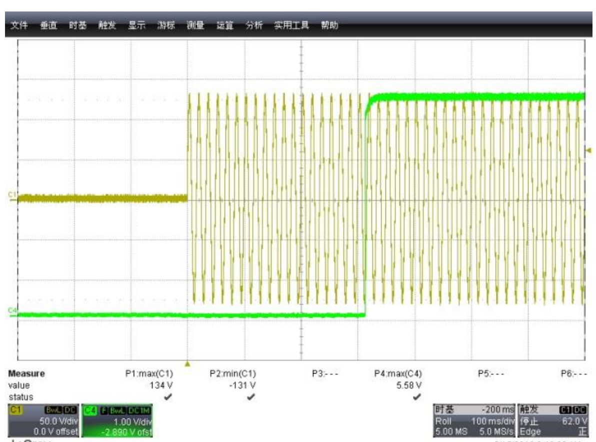


Figure 9: 65W PD 3.0 turn on time 0.32s 5V/3A at 90Vac

5.2.2 Q1 /Q2 Main Switching Voltage MOSFET Stress on at 20V/ 3.25A Loading @264Vac

Primary side MOSFET - Q1

Figure 10:   Q1 Vds Voltage stress

Secondary side SR MOSFET- Q2

Figure11: Q2 of Vds Voltage stress

Vout	Vds	Vds_Max_Spec	Ratio of voltage stress		Vout	Vds	Vds_Max_Spec	Ration of voltage stress
20V	598V	650V	92%		20V	87.1V	100V	87.1%

5.2.3 System Output Ripple & Noise with @ PCB End

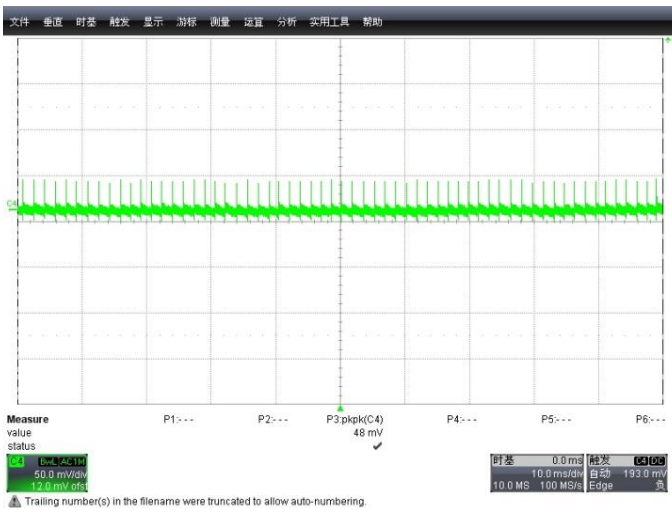


Figure 12: The Ripple at 90Vac/60Hz ΔV=48mV 5V/0A

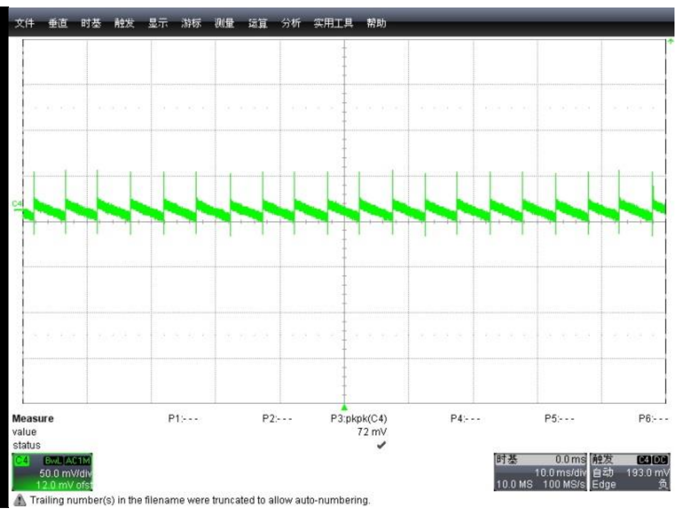


Figure 13: The Ripple at 264Vac/50Hz ΔV=72mv 5V/0A

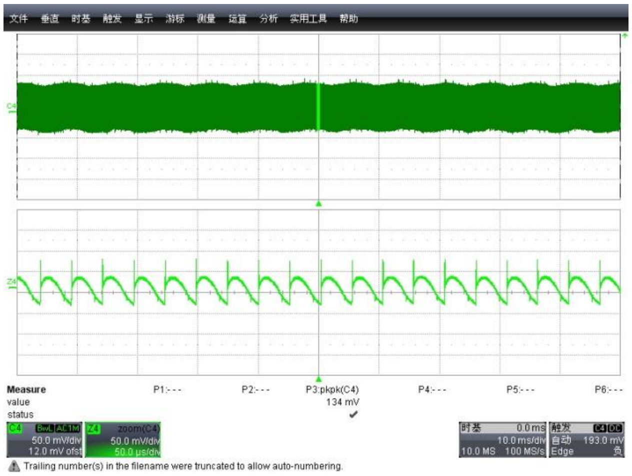


Figure 14:   90Vac/60Hz   5V/3A ΔV=132mV

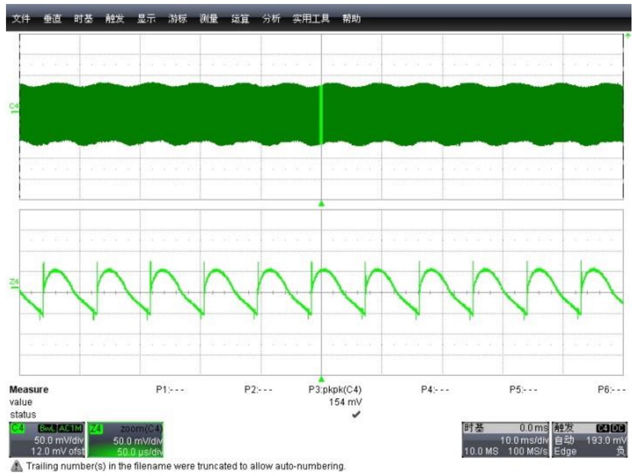


Figure 15:   264Vac/50Hz 5V/3A ΔV=154mv

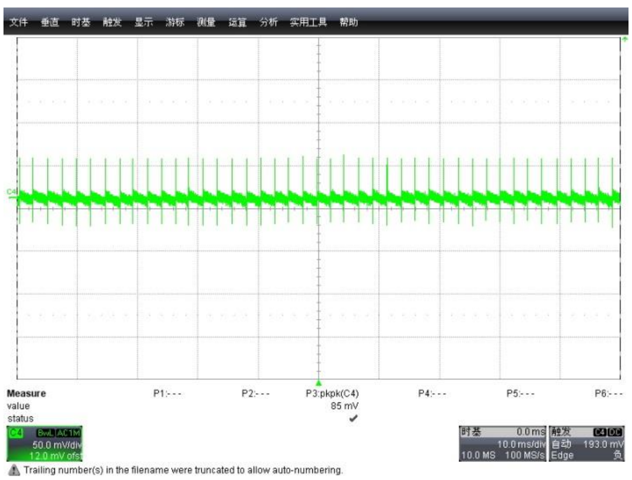


Figure 16: 90Vac/60Hz 9V/0A ΔV=85mV

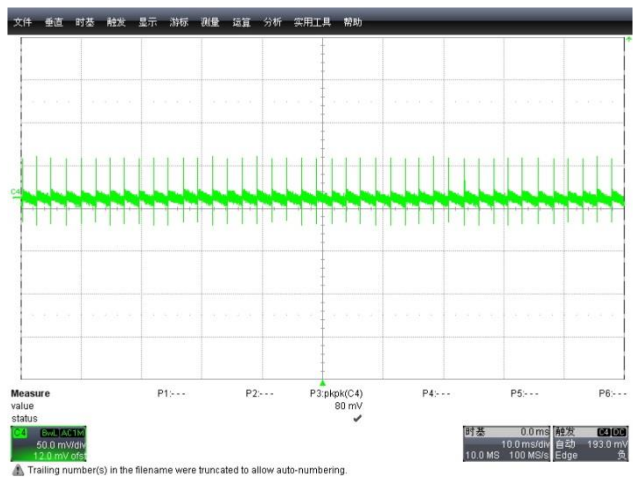


Figure 17: 264Vac/50Hz 9V/0A   ΔV=80mv

Figure 18: 90Vac/60Hz 9V/3A ΔV=150mV

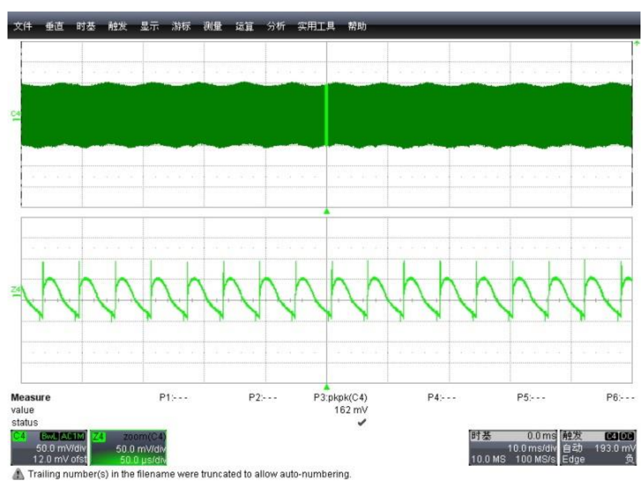


Figure 19: 264Vac / 60Hz 9V/3A ΔV=162mV

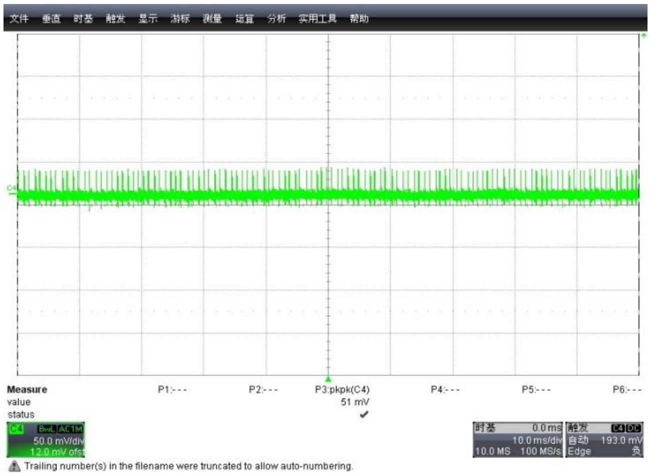


Figure 20: 90Vac/60Hz 12V/0A ΔV=51mV

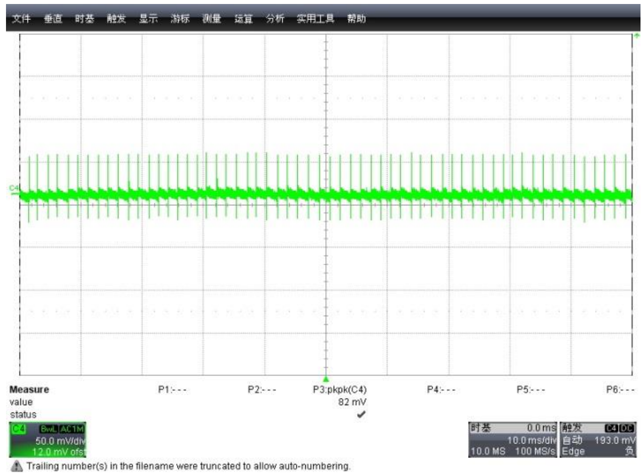


Figure 21: 264Vac / 60Hz 12V/0A ΔV=82mV

Figure 22: 90Vac/60Hz 12V/3A ΔV=157mV

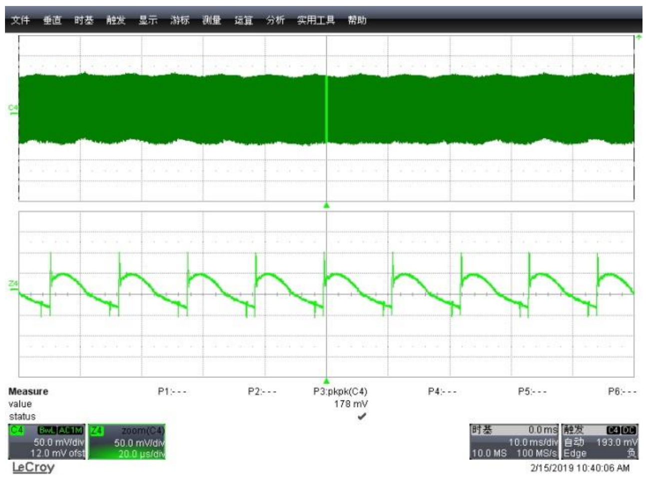


Figure 23: 264Vac / 60Hz 12V/3A ΔV=178mV

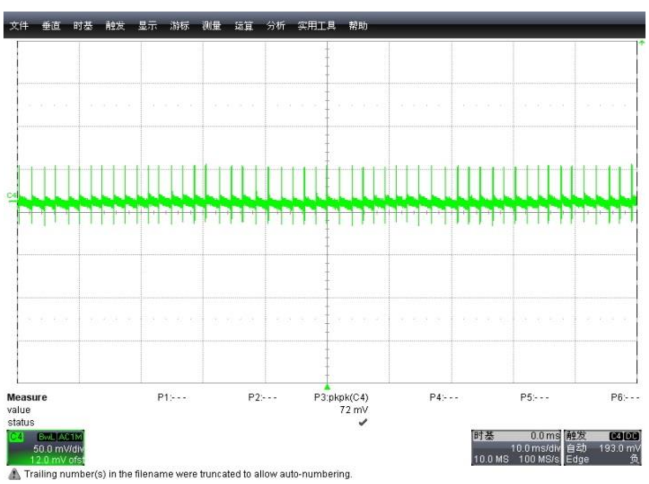


Figure 24: 90Vac/60Hz 15V/0A ΔV=72mV

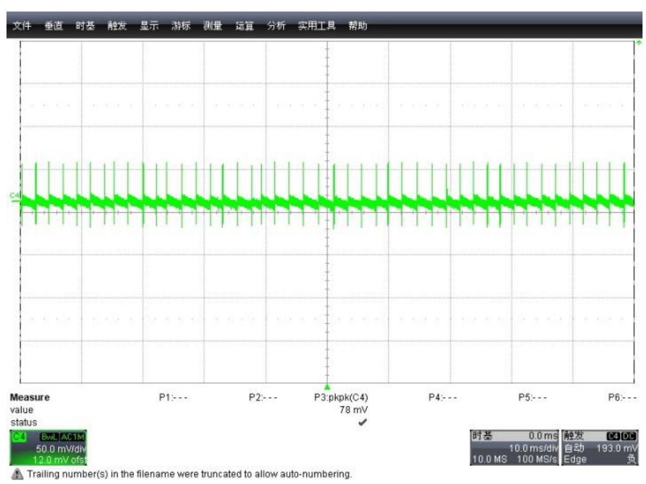


Figure 25: 264Vac / 60Hz 15V/0A ΔV=78mV

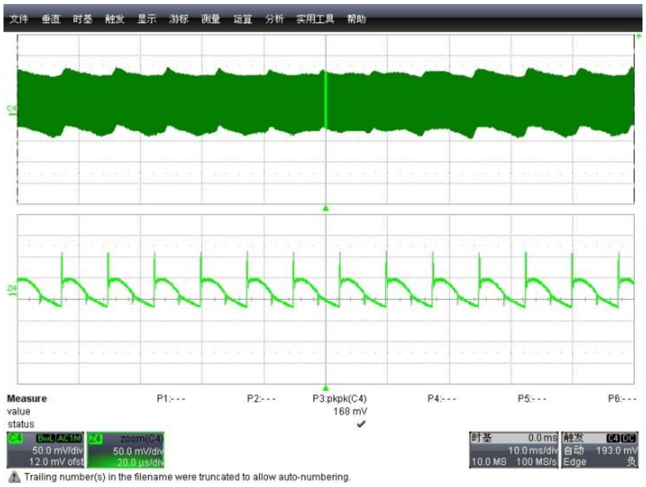


Figure 26: 90Vac/60Hz 15V/3A ΔV=168mV

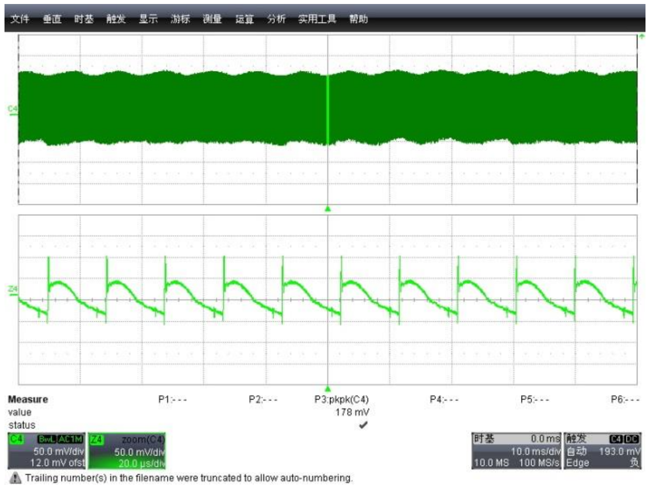


Figure 27: 264Vac / 60Hz 15V/3A ΔV=178mV

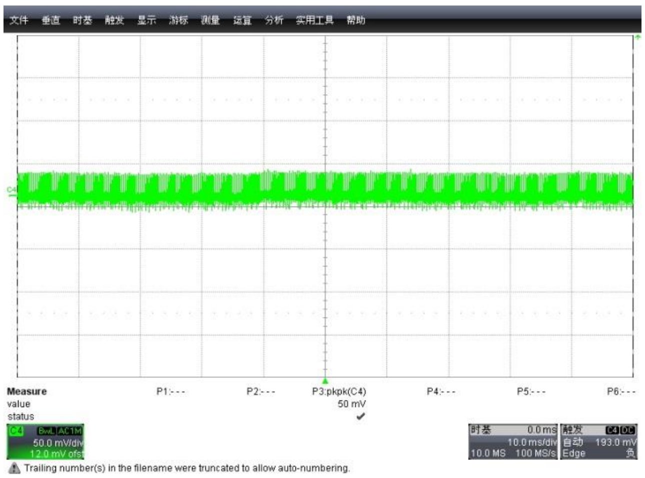


Figure 28: 90Vac/60Hz 20V/0A ΔV=50mV

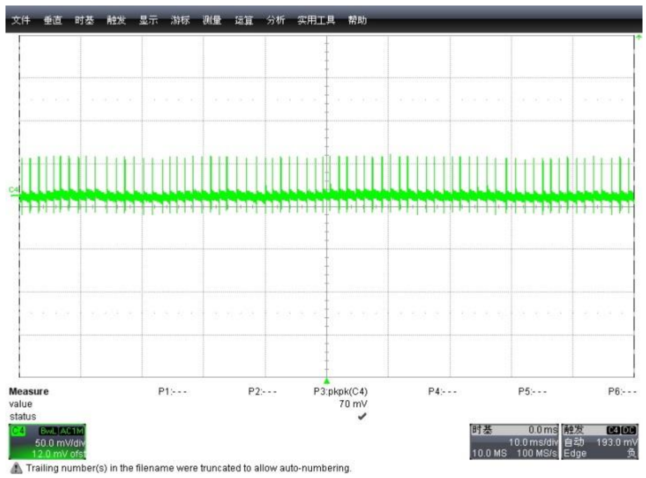


Figure 29: 264Vac / 60Hz 20V/0A ΔV=70mV

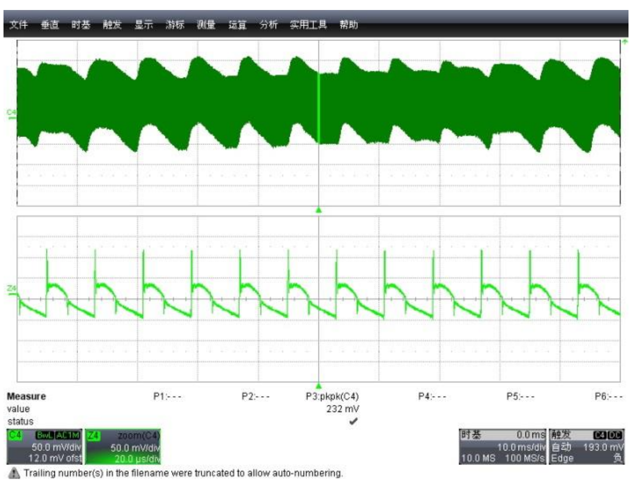


Figure 30: 90Vac/60Hz 20V/3.25A ΔV=232mV

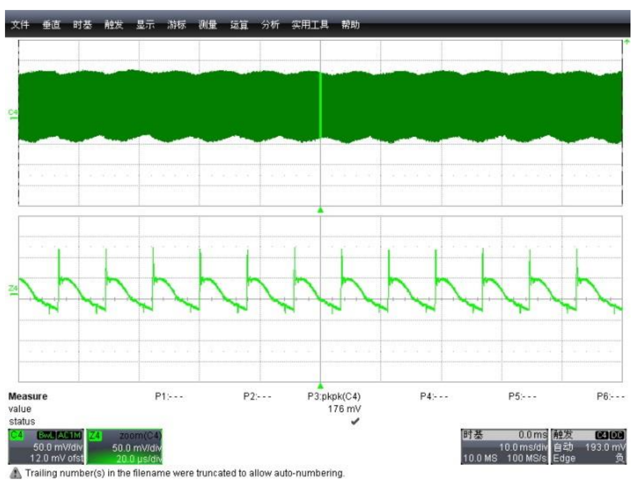


Figure 31: 264Vac / 60Hz 20V/3.25A ΔV=176mV

5.2.4 Dynamic load ----0.3A-3A, Tr=10mS , 100mA/uS(PCB End)

Figure 32: 5V 0.3 ~ 3A

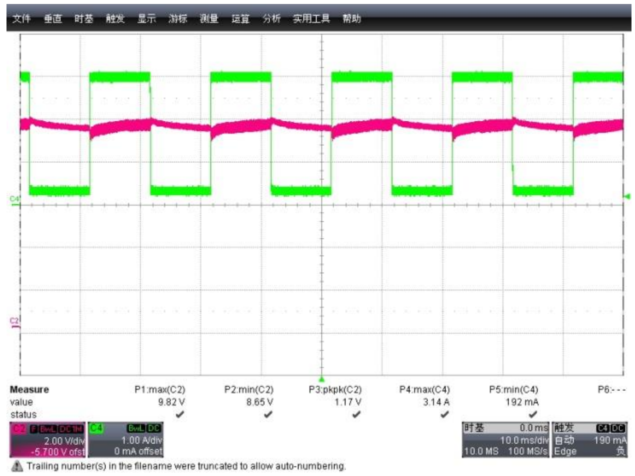


Figure 33: 9V 0.3 ~ 3A

Vin=90V	Vo_Undershoot(V)	Vo_Overshoot(V)
5V	4.72	5.76
9V	8.65	9.82

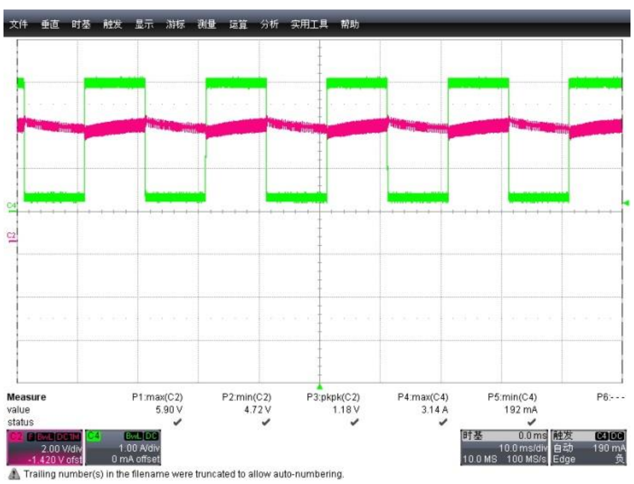


Figure 34: 5V 0.3 ~ 3A

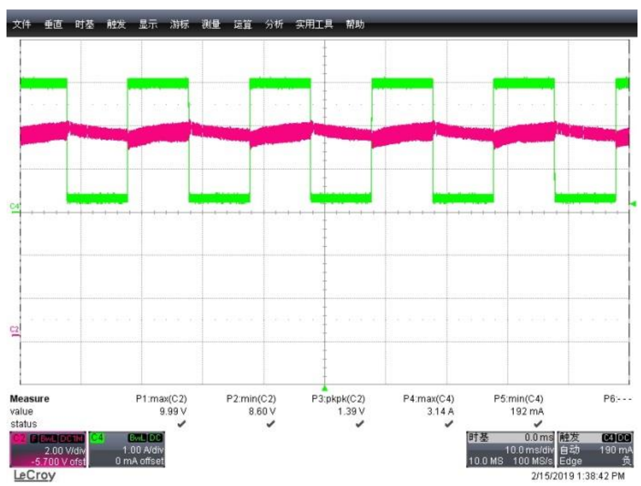


Figure 35: 9V 0.3 ~ 3A

Vin=264V	Vo_Undershoot(V)	Vo_Overshoot(V)
5V	4.72	5.9
9V	8.6	9.99

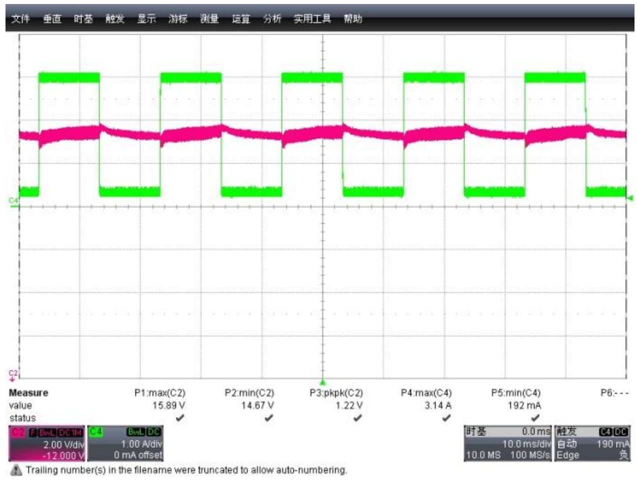


Figure 36: 12V 0.3 ~ 3A

Figure 37: 15V 0.3 ~ 3A

Vin=90V	Vo_ Undershoot(V)	Vo_ Overshoot(V)
12V	11.65	12.87
15V	14.67	15.89

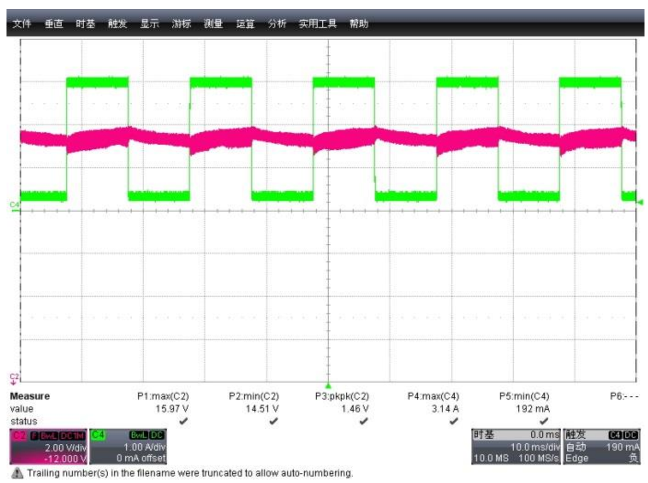


Figure 38: 12V 0.3 ~ 3A

Figure 39: 15V 0.3 ~ 3A

Vin=264V	Vo_ Undershoot(V)	Vo_ Overshoot(V)
12V	11.60	12.95
15V	14.51	15.97

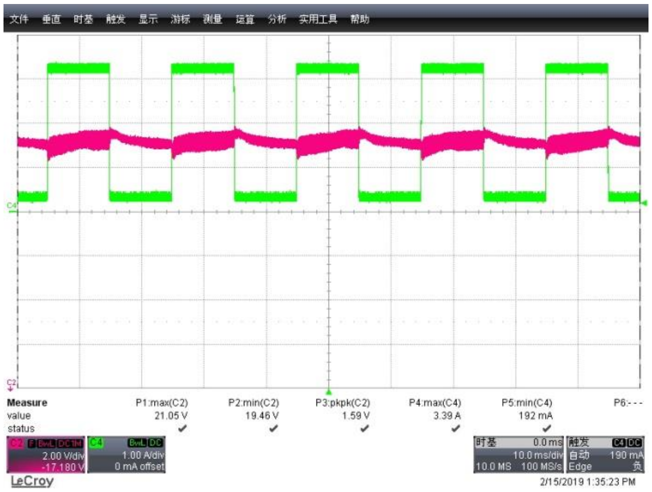


Figure 40: 20V 0 ~ 3A @ 90Vac

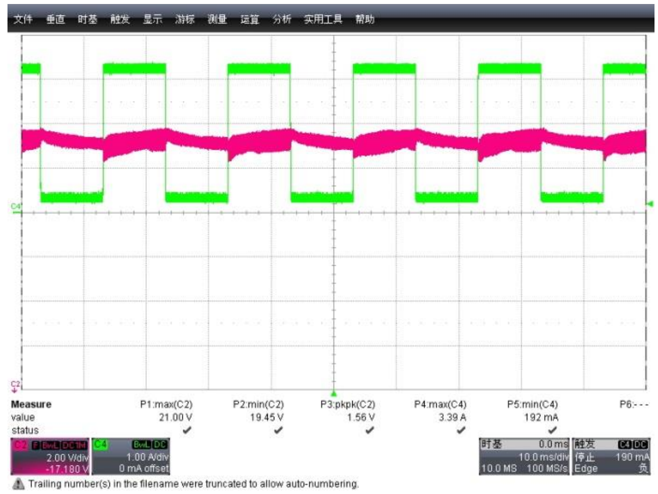


Figure 41: 20V 0 ~ 3A @264Vac

Vin	Vout	Vo_ Undershoot(V)	Vo_ Overshoot(V)
90Vac	20V	19.46	20.05
264Vac	20V	19.45	21.00

5.2.5 Output Voltage Transition Time

From Step up & Step down

Figure 42: 5V-9V-12V-15V-20V Transition Step Up Time

Figure 43: 5V-9V-12-15V-20V Transition Steo down Time

Transition time from Low to high

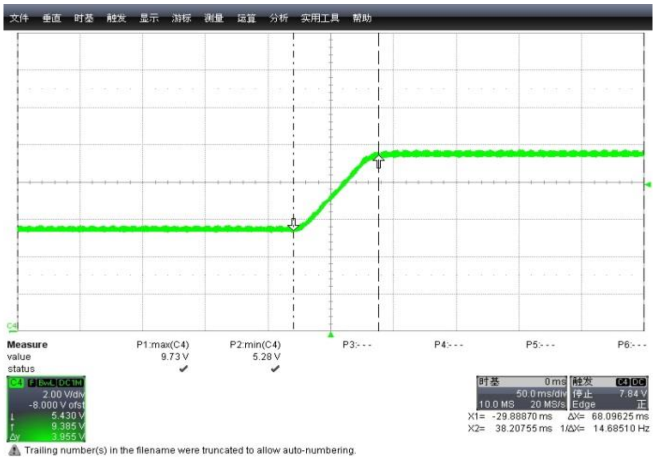


Figure 44: 5V→9V Transition upl Time: 68ms

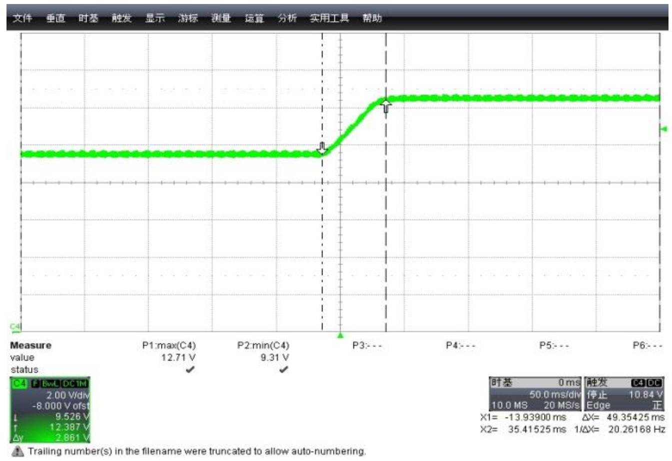


Figure 45: 9V→12V Fall Time: 49ms

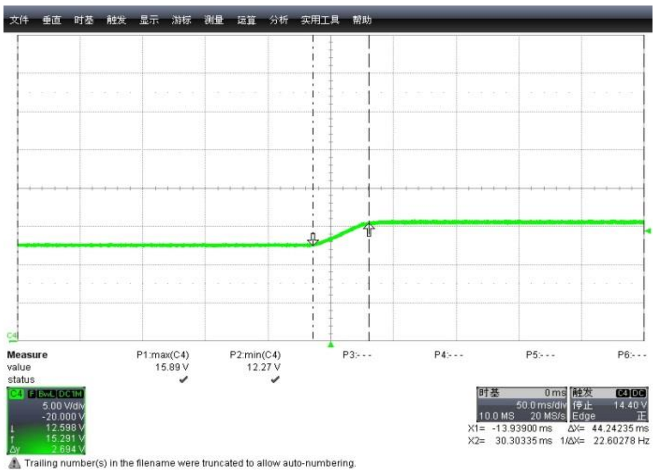


Figure 46: 12V→15V Fall Time: 44ms

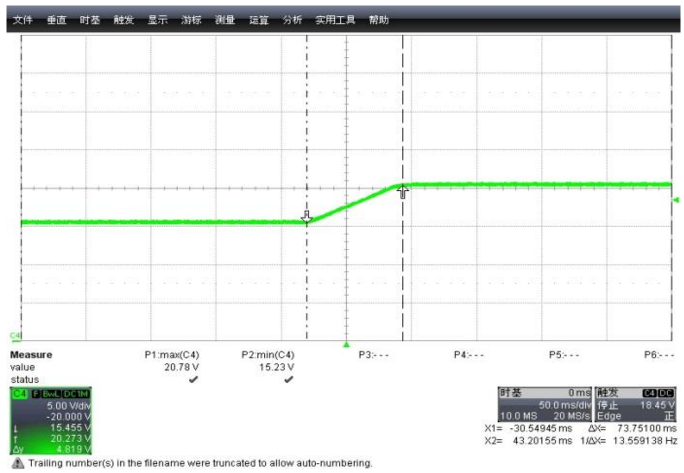


Figure 47: 15V→20V Fall Time: 74ms

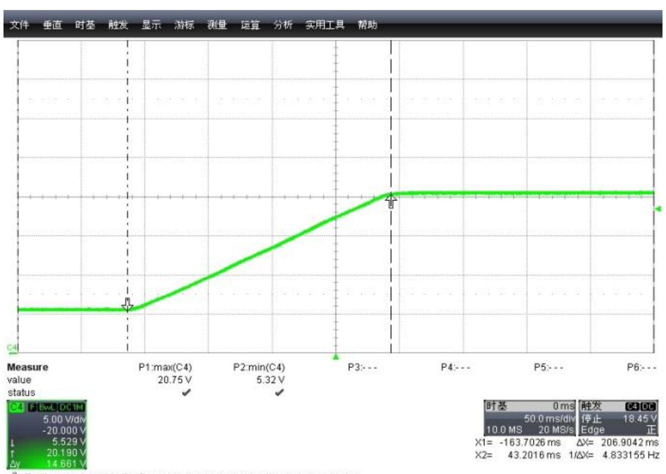
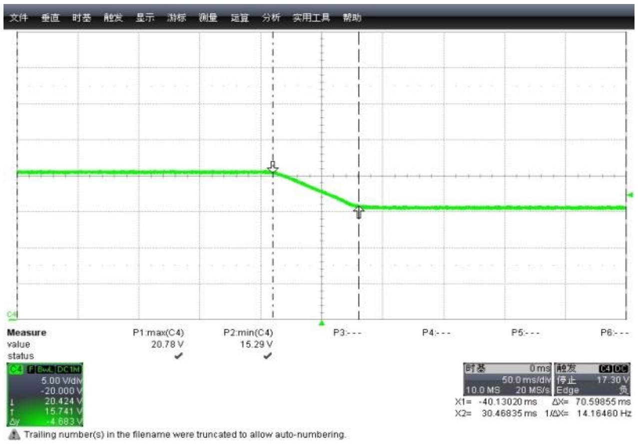


Figure 48: 5V→20V Fall Time: 206ms

5.2.6 Output Voltage Transition Time from High to Low



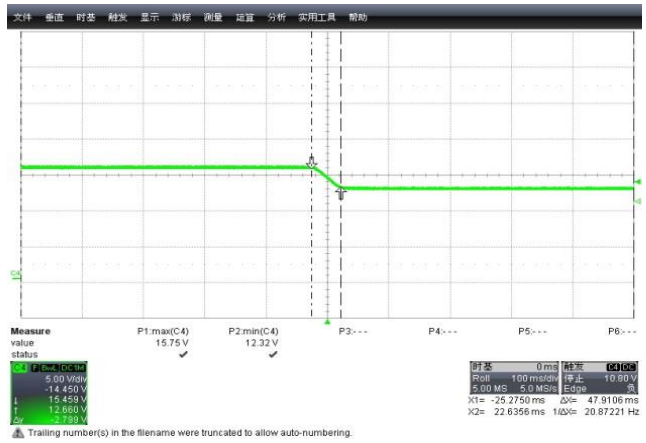


Figure 49: 20V→15V Fall Time: 71ms

Figure 50: 15V→12V Fall Time: 48ms

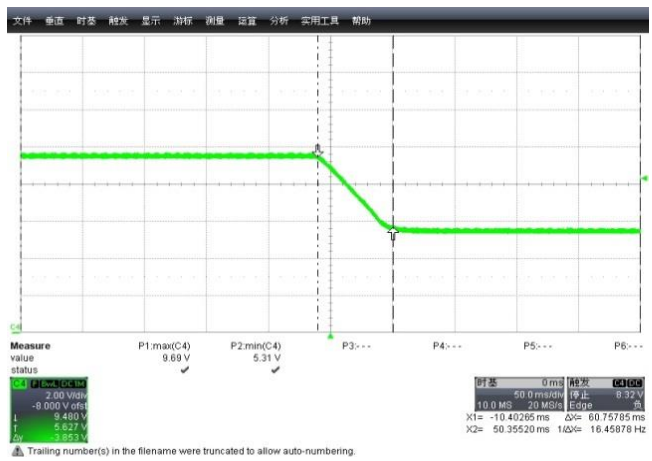


Figure 51: 12V→9.0V Fall Time: 56ms

Figure 52: 9V→5V Fall Time: 61ms

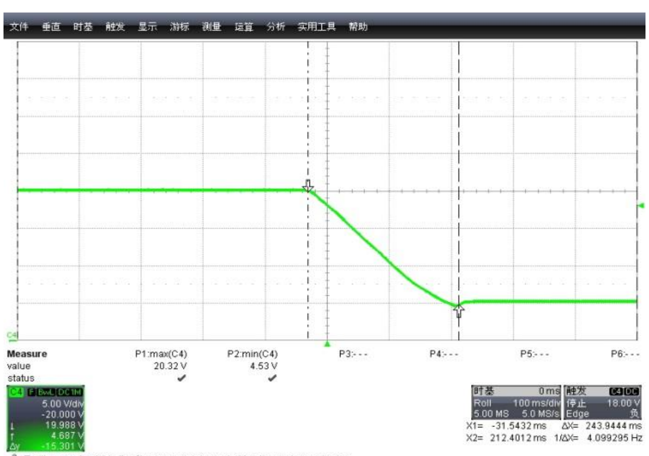


Figure 53: 20V→5.0V Fall Time: 244ms

5.2.7 Thermal Testing

Test Condition : AC input=90Vac, Load 20V-3.25A ,Open Frame

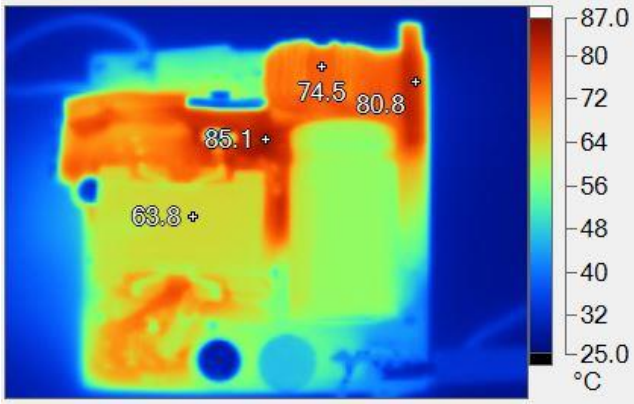


Figure 54: Components Side

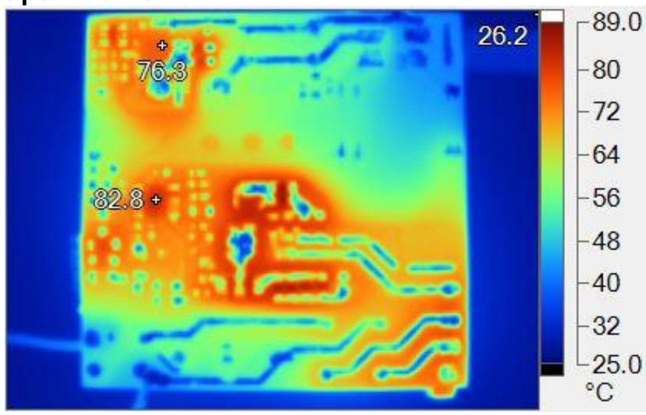


Figure 55: surface mount side

Test Items	Temperature	Unit
Ambient Temp	26.2	℃
AP3108L	82.8	℃
Q1	85.1	℃
T1	68.8	℃
Q2	76.3	℃
BD1	80.8	℃

Test Condition: Vin=264Vac Vo=20V Io=3.25A Open Frame

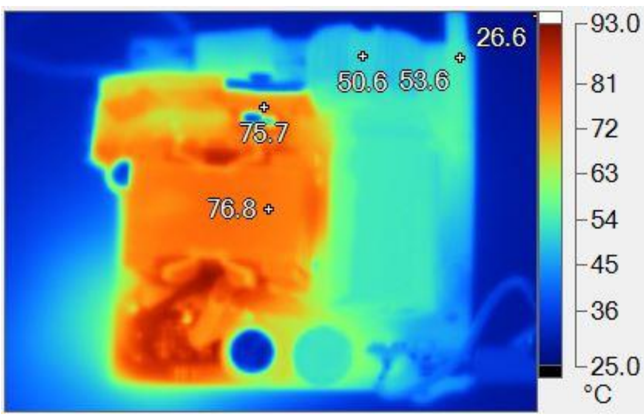


Figure 56: Components Side

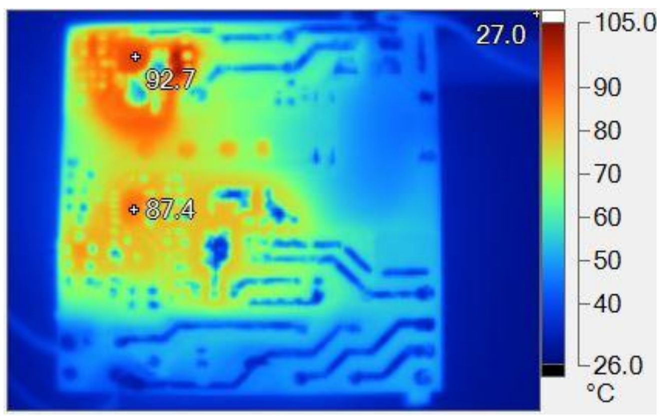
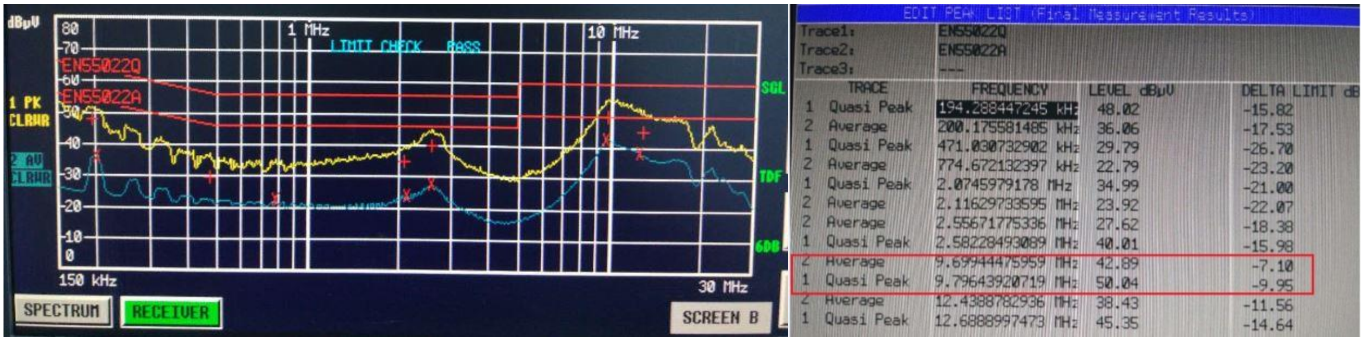


Figure 57: Surface mount side

Test Items	Temperature	Unit
Ambient Temp	26.6	℃
AP3108L	87.4	℃
Q1	75.7	℃
T1	76.8	℃
Q2	92.7	℃
BD1	53.6	℃

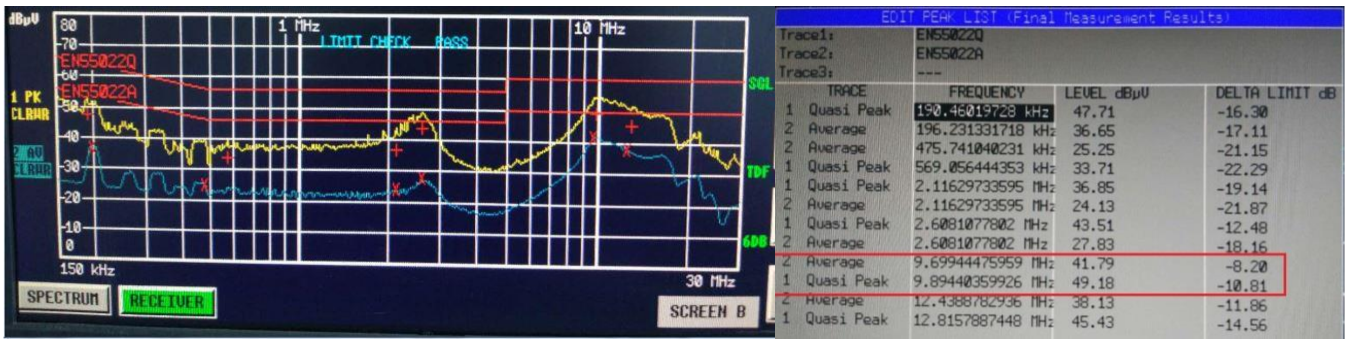
5.3. EMI (CE) testing results

5.3.1 EMI (CE) Testing results—115Vac @ 20V/3.25A- (L) & (N)



TRACE		FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
1	Quasi Peak	194.288447245 kHz	48.02	-15.82
2	Average	200.175581485 kHz	36.06	-17.53
1	Quasi Peak	471.030732902 kHz	29.79	-26.70
2	Average	774.672132397 kHz	22.79	-23.20
1	Quasi Peak	2.0745979178 MHz	34.99	-21.00
2	Average	2.11629733595 MHz	23.92	-22.07
2	Average	2.55671775336 MHz	27.62	-18.38
1	Quasi Peak	2.58228493089 MHz	40.01	-15.98
2	Average	9.69944475959 MHz	42.89	-7.10
1	Quasi Peak	9.79643920719 MHz	50.04	-9.95
2	Average	12.4388782936 MHz	38.43	-11.56
1	Quasi Peak	12.6888997473 MHz	45.35	-14.64

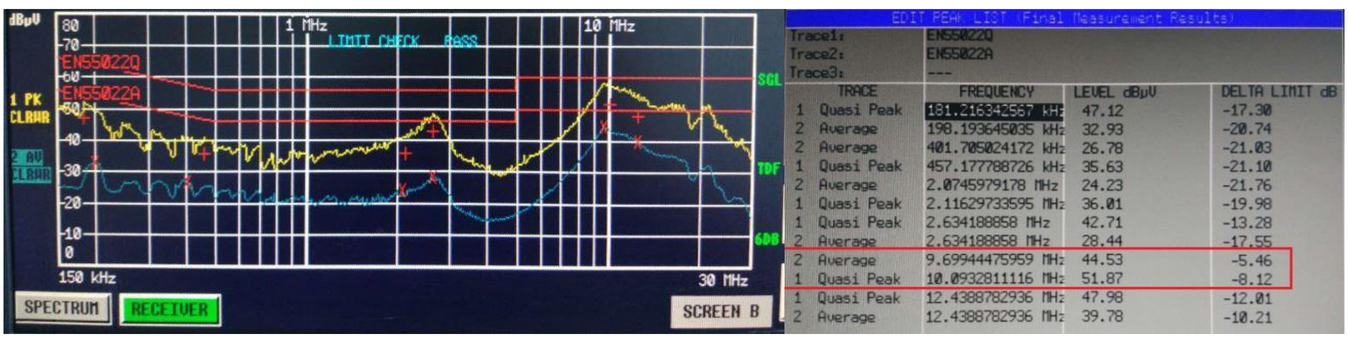
Figure 58: 115Vac/60Hz 20V/3.25A (L)



TRACE		FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
1	Quasi Peak	190.46019728 kHz	47.71	-16.30
2	Average	196.231331718 kHz	36.65	-17.11
2	Average	475.741040231 kHz	25.25	-21.15
1	Quasi Peak	569.056444353 kHz	33.71	-22.29
1	Quasi Peak	2.11629733595 MHz	36.85	-19.14
2	Average	2.11629733595 MHz	24.13	-21.87
1	Quasi Peak	2.6081077802 MHz	43.51	-12.48
2	Average	2.6081077802 MHz	27.83	-18.16
2	Average	9.69944475959 MHz	41.79	-8.20
1	Quasi Peak	9.89440359926 MHz	49.18	-10.81
2	Average	12.4388782936 MHz	38.13	-11.86
1	Quasi Peak	12.8157887448 MHz	45.43	-14.56

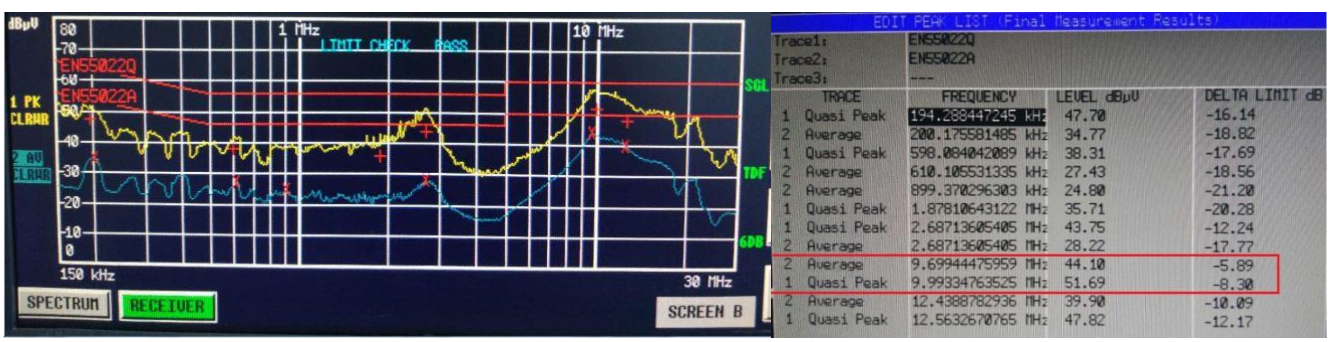
Figure 59: 115Vac/60Hz 20V/3.25A (N)

5.3.2 EMI (CE) Testing results—230Vac @ 20V/3.25A- (L) & (N)



TRACE		FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
1	Quasi Peak	181.216342567 kHz	47.12	-17.30
2	Average	198.193645035 kHz	32.93	-20.74
2	Average	401.705024172 kHz	26.78	-21.03
1	Quasi Peak	457.177788726 kHz	35.63	-21.10
2	Average	2.0745979178 MHz	24.23	-21.76
1	Quasi Peak	2.11629733595 MHz	36.01	-19.98
1	Quasi Peak	2.634188858 MHz	42.71	-13.28
2	Average	2.634188858 MHz	28.44	-17.55
2	Average	9.69944475959 MHz	44.53	-5.46
1	Quasi Peak	10.0932811116 MHz	51.87	-8.12
1	Quasi Peak	12.4388782936 MHz	47.98	-12.01
2	Average	12.4388782936 MHz	39.78	-10.21

Figure 60: 230Vac/50Hz 20V/3.25A (L)



TRACE		FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
1	Quasi Peak	194.288447245 kHz	47.70	-16.14
2	Average	200.175581485 kHz	34.77	-18.82
1	Quasi Peak	598.084042089 kHz	38.31	-17.69
2	Average	610.105531335 kHz	27.43	-18.56
2	Average	899.370296303 kHz	24.80	-21.20
1	Quasi Peak	1.87810643122 MHz	35.71	-20.28
1	Quasi Peak	2.68713605405 MHz	43.75	-12.24
2	Average	2.68713605405 MHz	28.22	-17.77
2	Average	9.69944475959 MHz	44.10	-5.89
1	Quasi Peak	9.99334763525 MHz	51.69	-8.30
2	Average	12.4388782936 MHz	39.90	-10.09
1	Quasi Peak	12.5632670765 MHz	47.82	-12.17

Figure 61: 230Vac/50Hz 20V/3.25A (N)

Chapter 6. Revision Control

6.1 Revision table

Revision	Items Changed & added	The changing reason
1.0	Release	
1.1	From Rev 1.0 to Rev 1.1	Cleared Page 1 wrong words near bottom line