# Not Recommended for New Design - Use PI3WVR648



Diodes Incorporated



**PI3WVR628** 

#### 2:1 MIPI 2-Data Lane Switch

### Description

The DIODES PI3WVR628 is a two-data-lane MIPI switch. This 6 channel single-pole, double-throw (SPDT) switch is optimized for switching between two high-speed (HS) or low-power (LP) MIPI signal. The PI3WVR628 is designed for the MIPI specification and allows connection to CSI/DSI, C-PHY/D-PHY module.

### Application(s)

- Cellular Phones, Smart Phones
- Tablets
- Laptops
- Displays

#### **Features**

- 3-lane, 2:1 switches that support D-PHY and C-PHY
- Data rate support: up to 3.5Gsps C-PHY, up to 4.5Gb/s D-PHY. •
- Bandwidth: 6.0 GHz Typical •
- Low Crosstalk: -30 dB@2.25 GHz •
- Input Signals 0 to 1.3V
- R<sub>ON</sub>: 5.0Ω Typical LP & HS MIPI •
- $\Delta R_{ON}$ : 0.1 $\Omega$  Typical LP & HS MIPI •
- $R_{ON\_FLAT}\!\!:\!0.3\Omega$  Typical LP & HS MIPI
- I<sub>CCZ</sub>: 1µA Maximum
- I<sub>CC</sub>: 15µA Typical
- Skew of Opposite Transitions of the Same Output: 2ps Typical
- V<sub>DD</sub> Operating Range: 1.5V to 3.6V
- ESD Tolerance: 2kV HBM
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/
- Packaging (Pb-free & Green):
  - <sup>o</sup> 24-Pin, X1-LGA2417-24 (1.7mm x 2.4mm) (XB)

#### Notes:

PI3WVR628 Document Number DS42007 Rev 6-3

<sup>1.</sup> No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.

<sup>2.</sup> See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free. 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.



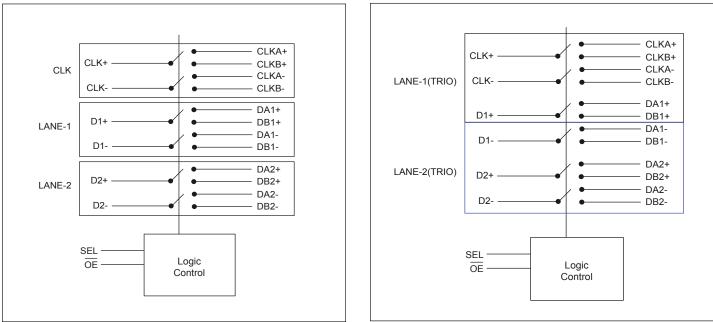
PI3WVR628 C-PHY



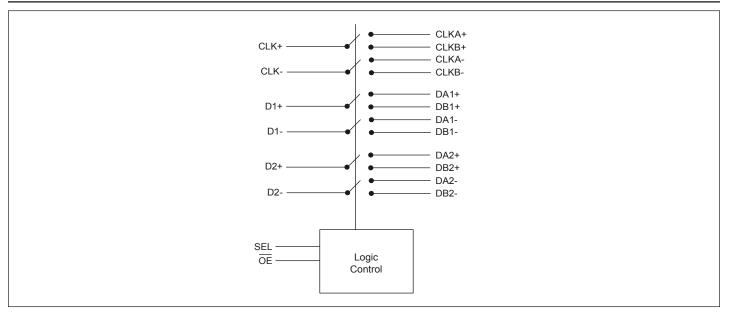
**PI3WVR628** 

## **Application Diagram**

## PI3WVR628 D-PHY



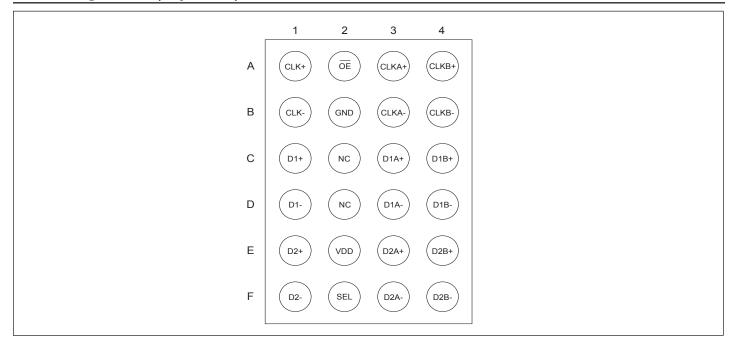
## **Block Diagram**







## Pin Configuration(Top View)



#### **Truth Table**

SEL	ŌĒ	Function
LOW	LOW	CLK+ = CLKA+, CLK- = CLKA-, Dn(+/-) = DAn(+/-)
HIGH	LOW	CLK+ = CLKB+, CLK- = CLKB-, Dn(+/-) = DBn(+/-)
Х	HIGH	Clock and Data Ports High Impedance





## **Pin Description**

Pin#	Pin Name	Signal Type	Description
E2	V <sub>DD</sub>	Power	1.5V to 3.3V power supply
B2	GND	Ground	Ground
A2	OE	Ι	Output enable. if OE is low, IC is enabled. if OE is high, IC is power down and all I/Os are Hi-Z
F2	SEL	Ι	Switch logic control
C2, D2	NC	-	Not Connect
F4	D2B-	I/O	Negative differential signal 2 for port B
E4	D2B+	I/O	Positive differential signal 2 for port B
F3	D2A-	I/O	Negative differential signal 2 for port A
E3	D2A+	I/O	Positive differential signal 2 for port A
F1	D2-	I/O	Negative differential signal 2 for COM port
E1	D2+	I/O	Positive differential signal 2 for COM port
D4	D1B-	I/O	Negative differential signal 1 for port B
C4	D1B+	I/O	Positive differential signal 1 for port B
D3	D1A-	I/O	Negative differential signal 1 for port A
C3	D1A+	I/O	Positive differential signal 1 for port A
D1	D1-	I/O	Negative differential signal 1 for COM port
C1	D1+	I/O	Positive differential signal 1 for COM port
B4	CLKB-	I/O	Clock negative differential signal for port B
A4	CLKB+	I/O	Clock positive differential signal for port B
B3	CLKA-	I/O	Clock negative differential signal for port A
A3	CLKA+	I/O	Clock positive differential signal for port A
B1	CLK-	I/O	Clock negative differential signal for COM port
A1	CLK+	I/O	Clock positive differential signal for COM port





## **Absolute Maximum Ratings**

(Above which useful life may be impaired. For user guidelines, not test	ed.)
(Above which useful life may be impaired. For user guidelines, not tester $V_{CC}$ , Supply Voltage,	ed.) Note: Stresse INGS I stress I these c operat: Expose tended
ESD: Human Body Model, JEDEC: JESD22-A114, All Pins 2.0kV Charged Device Model, JEDEC: JESD22-C101 1.0kV	

resses greater than those listed under MAXIMUM RAT-NGS may cause permanent damage to the device. This is a tress rating only and functional operation of the device at nese or any other conditions above those indicated in the perational sections of this specification is not implied. xposure to absolute maximum rating conditions for exnded periods may affect reliability.

#### Note:

1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

2. V<sub>SW</sub> refers to analog data switch paths.

## **Recommended Operating Conditions**

The Recommended operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications.

Symbol	Description	Test Conditions	Min.	Max.	Units
V <sub>CC</sub>	Supply Voltage		1.5	3.6	V
V <sub>CNTRL</sub>	Control Input Voltage (SEL, $\overline{OE}$ ) <sup>(1)</sup>		0	V <sub>CC</sub>	V
	Contractive Deciver Deciver DA DR	HS Mode	0	0.5	V
V <sub>SW</sub>	Switch I/O Voltage (CLK-, D-, CLKA-, CLKB-, DA-, DB-)	LP Mode	0	1.3	V
T <sub>A</sub>	Operating Temperature		-40	+85	°C

Note:

1. The control inputs must be held HIGH or LOW; they must not float.

## **DC and Transient Characteristics**

All typical values are at  $T_{\Delta} = 25^{\circ}$ C unless otherwise specified.

Cll.			$V_{CC}(V)$ -	$T_A = -4$	TT		
Symbol	Description	Test Conditions		Min.	Тур.	Max.	Units
V <sub>IK</sub>	Clamp Diode Voltage (OE, SEL)	$I_{IN} = -18mA$	1.5	-1.2		-0.6	V
V <sub>IH</sub>	Input Voltage High	SEL, $\overline{OE}$	1.5 to 3.3	1.0			V
V <sub>IL</sub>	Input Voltage Low	SEL, $\overline{OE}$	1.5 to 3.3			0.5	V
I <sub>IN</sub>	Control Input Leakage (OE, SEL)	$V_{CNTRL} = 0$ to $V_{CC}$	3.3	-0.5		0.5	μΑ
I <sub>NO(OFF)</sub> I <sub>NC(OFF)</sub>	Off Leakage Current of Port CLKA-, DA-, CLKB- and DB-	$V_{SW} = 0.0 \le DATA \le 1.3V$	3.3	-0.5		0.5	μΑ





0 1 1	Description			$T_{\rm A} = -40^{\rm o} {\rm C} \text{ to } +85^{\rm o} {\rm C}$			<b>T</b> T •4
Symbol	Description	Test Conditions	$V_{CC}(V)$	Min.	Тур.	Max.	Units
I <sub>A(ON)</sub>	On Leakage Current of Common Ports (CLK-, D-)	$V_{SW} = 0.0 \le DATA \le 1.3V$	3.3	-0.5		0.5	μA
I <sub>OFF</sub>	Power-Off Leakage Current (All I/O Ports)	V <sub>SW</sub> = 0.0 or 1.3V	0	-0.5		0.5	μA
I <sub>OZ</sub>	Off-State Leakage	$\frac{V_{SW} = 0.0 \le DATA \le 1.3V,}{OE = High}$	3.3	-0.5		0.5	μΑ
		$I_{ON} = -8mA, \overline{OE} = 0V,$	1.5				
R <sub>ON_MIPI_HS</sub>	Switch On Resistance for HS MIPI	$SEL = V_{CC}$ or 0V, CLKA,	2.5		5		Ω
		CLKB, DB- or DA- $= 0.2V$	3.3				
		$I_{ON} = -8mA$ , $\overline{OE} = 0V$ ,	1.5				
R <sub>ON_MIPI_LP</sub>	Switch On Resistance for LP MIPI	SEL = $V_{CC}$ or 0V, CLKA, CLKB, DB- or DA- = 1.2V	2.5		5		Ω
			3.3				
4.D	R <sub>ON_MIPI_HS</sub> On Resistance Matching Between HS MIPI Channels <sup>(1)</sup>	$I_{ON} = -8mA, \overline{OE} = 0V,$ SEL = V <sub>CC</sub> or 0V, CLKA, CLKB, DB- or DA- = 0.2V	1.5		0.1		
$\Delta R_{ON}_{MIPI}_{HS}$			2.5		0.1		Ω
			3.3 1.5				
$\Delta R_{ON_MIPI_LP}$	On Resistance Matching Between	$I_{ON} = -8mA$ , $OE = 0V$ , SEL = $V_{CC}$ or $0V$ , CLKA,	2.5		0.1		Ω
ARON_MIPI_LP	LP MIPI Channels <sup>(1)</sup>	CLKB, DB- or DA- = $1.2V$	3.3		0.1		22
		$I_{ON} = -8mA, \overline{OE} = 0V,$	1.5				
R <sub>ON_FLAT_</sub>	On Resistance Flatness for HS MIPI	$SEL = V_{CC}$ or 0V, CLKA,	2.5		0.3		Ω
MIPI_HS		CLKB, DB- or DA- = 0 to $0.5V$	3.3		0.0		
		$I_{ON} = -8mA, \overline{OE} = 0V,$	1.5				
R <sub>ON_FLAT_</sub>	On Resistance Flatness for LP MIPI	$SEL = V_{CC}$ or 0V, CLKA,	2.5		0.3		Ω
MIPI_LP	On Resistance Flatness for EF with F	CLKB, DB- or DA- = 0 to 1.3V	3.3		0.5		
I <sub>CC</sub>	Quiescent Supply Current	$\frac{V_{SEL} = 0 \text{ or } V_{CC}, I_{OUT} = 0,}{OE = 0V}$	3.6		11	20	μΑ
I <sub>CCZ</sub>	Quiescent Supply Current (High Impedance)	$\frac{V_{SEL} = 0 \text{ or } V_{CC}, I_{OUT} = 0,}{OE = 0V}$	3.6			1	μΑ
I <sub>CCT</sub>	Increase in $I_{\rm CC}$ Current Per Control Voltage and $V_{\rm CC}$	$V_{SEL} = 0 \text{ or } V_{CC}, \overline{OE} = 1.5V$	3.6		1		μΑ





## **AC Electrical Characteristics**

0 1 1			V <sub>CC</sub> (V)	$T_{\rm A} = -40^{\rm o}{\rm C}$ to $+85^{\rm o}{\rm C}$			
Symbol	Description	Test Conditions		Min.	Тур.	Max.	Units
t <sub>INIT</sub>	Initialization Time V <sub>CC</sub> to Output <sup>(1)</sup>	$R_{L} = 50\Omega, C_{L} = 0pF, V_{SW}$ $= 0.6V$	1.5 to 3.6		60		μs
t <sub>EN</sub>	Enable Time $\overline{OE}$ to Output	$R_{L} = 50\Omega, C_{L} = 0pF, V_{SW}$ $= 0.6V$	1.5 to 3.6		60	150	μs
t <sub>DIS</sub>	Disable Time $\overline{OE}$ to Output	$\begin{aligned} R_{\rm L} &= 50\Omega,  C_{\rm L} = 0 \text{pF},  V_{\rm SW} \\ &= 0.6 \text{V} \end{aligned}$	1.5 to 3.6		35	250	ns
t <sub>ON</sub>	Turn-On Time SEL to Output	$R_{\rm L} = 50\Omega, C_{\rm L} = 0 \text{pF}, V_{\rm SW}$ $= 0.6 \text{V}$	1.5 to 3.6		350	1100	ns
t <sub>OFF</sub>	Turn-Off Time SEL to Output	$\begin{aligned} R_L &= 50\Omega, \ C_L = 0 p F, \ V_{SW} \\ &= 0.6V \end{aligned}$	1.5 to 3.6		125	800	ns
t <sub>BBM</sub>	Break-Before-Make Time	$\begin{aligned} R_L &= 50\Omega, \ C_L = 0 p F, \ V_{SW} \\ &= 0.6V \end{aligned}$	1.5 to 3.6			450	ns
t <sub>PD</sub>	Propagation Delay <sup>(1)</sup>	$C_{\rm L} = 0 {\rm pF}, R_{\rm L} = 50 \Omega$	1.5 to 3.6			0.25	ns
O <sub>IRR</sub>	Differential Off Isolation for MIPI <sup>(1)</sup>	$\frac{R_L}{OE} = 50\Omega, f = 1250MHz,$ $\overline{OE} = HIGH, V_{SW} = 0.5V$	1.5 to 3.6		-26		dB
V	Differential Crosstells for MIDI(1)	$\label{eq:RL} \begin{split} R_L &= 50\Omega,  f = 1250 MHz, \\ SEL &= HIGH,  V_{SW} = 0.5 V \end{split}$	15 to 26			-35	10
X <sub>TALK</sub>	Differential Crosstalk for MIPI <sup>(1)</sup>	$\label{eq:RL} \begin{split} R_L &= 50\Omega,  f = 2250 MHz, \\ SEL &= LOW,  V_{SW} = 0.5 V \end{split}$	- 1.5 to 3.6			-30	dB
T		$\begin{split} R_{L} &= 50\Omega, \ C_{L} = 0 p F, \\ f &= 2250 M Hz, \ V_{SW} = 0.5 V \end{split}$	1.5 to 3.6		-1.1		ar
I <sub>LOSS</sub> I	Differential Insertion Loss <sup>(1)</sup>	$R_L = 50\Omega, C_L = 0pF,$ f = 1250MHz, V <sub>SW</sub> = 0.5V	1.5 to 3.6		-0.8		dB
BW	Differential -3db Bandwidth <sup>(1)</sup>	$\begin{aligned} R_{L} &= 50\Omega, \ C_{L} &= 0 p F, \ V_{SW} \\ &= 0.5 V \end{aligned}$	1.5 to 3.6	5	6		GHz

Note:

1. Guaranteed by characterization.





## **High-Speed-Related AC Electrical Characteristics**

Crown b a l	Description	Test Can litiana	$V_{CC}(V)$	$T_{\rm A} = -40^{\rm o}{\rm C}$ to $+85^{\rm o}{\rm C}$			
Symbol		Test Conditions		Min.	Тур.	Max.	Units
	D-PHY HS Mode Skew of Opposite Transitions of the Same Output <sup>(1)</sup>	$\begin{array}{l} R_L=50\Omega,\ C_L=0pF,\ V_{SW}=\\ 0.3V \end{array}$	1.5 to 3.6		4		
t <sub>SK(P)</sub>	C-PHY HS Mode Skew of 3 channels in same lane	$\begin{array}{l} R_L=50\Omega,C_L=0pF,V_{SW}=\\ 0.5V \end{array}$	1.5 to 3.6		4		ps
	D-PHY HS Mode Skew of all group A or group B channels <sup>(1)</sup>	$\begin{array}{l} R_L=50\Omega,\ C_L=0pF,\ V_{SW}=\\ 0.3V \end{array}$	1.5 to 3.6		8		

Note:

1. Guaranteed by characterization.

## Capacitance

			$T_{\rm A} = -40^{\rm o}{\rm C} \text{ to } +85^{\rm o}{\rm C}$			
Symbol	Description	Test Conditions	Min.	Тур.	Max.	Units
C <sub>IN</sub>	Control Pin Input Capacitance <sup>(1)</sup>	$V_{CC} = 0V, f = 1MHz$		2.1		pF
C <sub>ON</sub>	On Capacitance <sup>(1)</sup>	$V_{CC} = 3.3V, \overline{OE} = 0V, f = 1250MHz$ (In HS common value)		1.3		pF
C <sub>OFF</sub>	Off Capacitance <sup>(1)</sup>	$V_{CC}$ or $\overline{OE}$ = 3.3V, f = 1250MHz (Both sides in HS common value)		0.8		pF

Note:

1. Guaranteed by characterization.





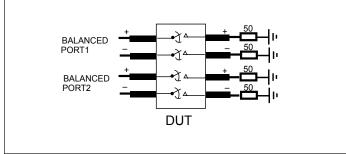
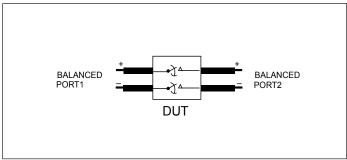
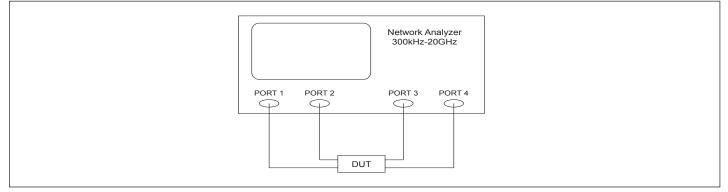


Figure 1. Crosstalk Setup



**Figure 3. Differential Insertion Loss** 

## **Test Circuit for Dynamic Electrical Characteristics**



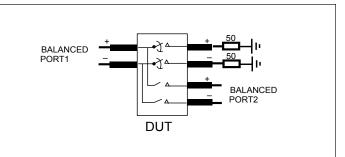
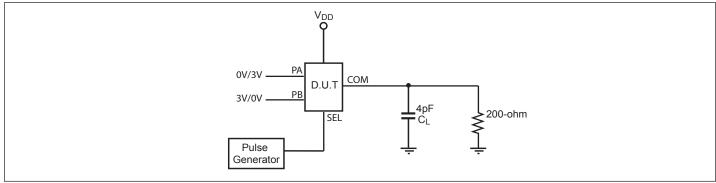


Figure 2. Off-Isolation Setup





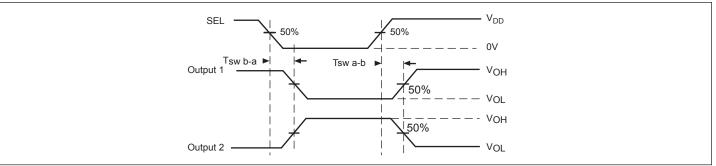
## Test Circuit for Electrical Characteristics(1-4)



Notes:

- 1. C<sub>L</sub> = Load capacitance: includes jig and probe capacitance.
- 2.  $R_{\rm T}$  = Termination resistance: should be equal to  $Z_{\rm OUT}$  of the Pulse Generator
- 3. All input impulses are supplied by generators having the following characteristics: PRR  $\leq$  MHz, Z<sub>O</sub> = 50 $\Omega$ , t<sub>R</sub>  $\leq$  2.5ns, t<sub>F</sub>  $\leq$  2.5ns.
- 4. The outputs are measured one at a time with one transition per measurement.

## **Switching Waveforms**

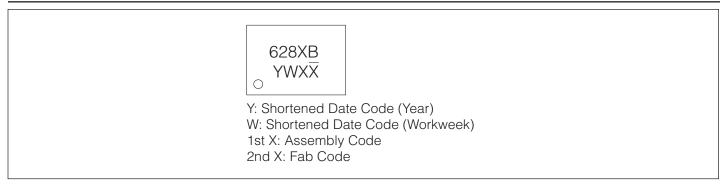


**Voltage Waveforms for Select Timing** 

### **Test Condition**

Output 1 Test Condition	<b>Output 2 Test Condition</b>
PA = Low	PA = High
PB = High	PB = Low

## **Part Marking**

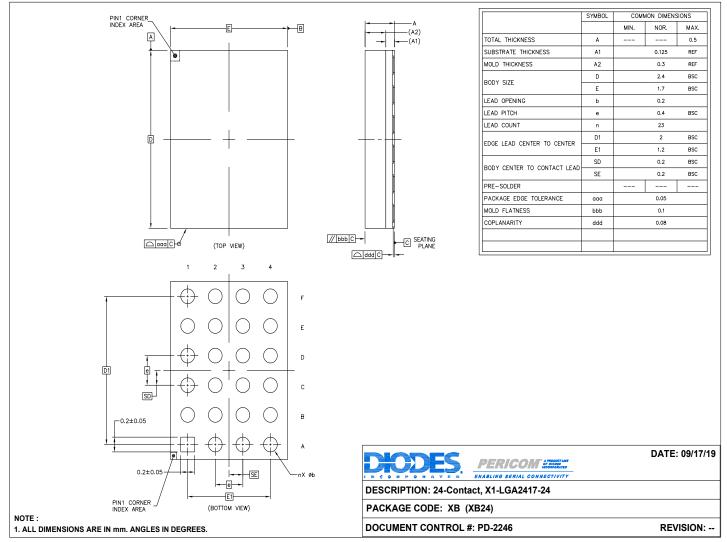






## **Packaging Mechanical**

### 24-X1-LGA2417-24 (XB)



#### For latest package info.

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## **Ordering Information**

Ordering Code	Package Code	Package Description
PI3WVR628XBEX	XB	24-contact, X1-LGA2417-24

Notes:

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.

2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free. 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm

antimony compounds.

4. E = Pb-free and Green

5. X suffix = Tape/Reel





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