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Output short-circuit protection on a synchronous rectified flyback converter with the ZXGD3101 controller

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Introduction

Offline synchronous rectified flyback converters must declare safe operation without any damage or performance degradation in the event of a sustained output short-circuit when the ZXGD3101 synchronous MOSFET controller loses its supply voltage and therefore the output current flow is completely via the internal body diode. At a first glance, this diode conduction loss should be greater when compared to the conventional schottky or ultrafast rectifier because of its higher forward voltage drop. Fortunately, most modern PWM controllers accommodate a low frequency pulse skipping mode to effectively limit the average power dissipating in both primary and synchronous MOSFETs. In order to make sure a power supply using the ZXGD3101 controller is operated safely during a short-circuit, this application note describes how to verify experimentally whether the pulse skipping pattern is sufficient to ensure the synchronous MOSFET will not be overheated, and also derives the current runaway constraint in relation to the magnetic saturation.

Short-circuit mechanism overview in a flyback converter

An output short-circuit will be seen by the primary side PWM controller as a sudden loss of feedback information from the output of the opto-coupler. In fact, during the start-up sequence, the system also runs open loop since no regulation has yet occurred. Some inexpensive controllers do not include short-circuit protection. Instead, they rely on the collapse of the auxiliary winding when the output is short-circuited to enter the burst mode operation. Unfortunately, the inevitable leakage inductance degrades the magnetic coupling between the power winding and the auxiliary winding. As a result, the auxiliary supply will not completely collapse to trigger the Under-Voltage Lock-Out (UVLO) function as expected: the controller will keep driving the primary MOSFET, and the uncontrollably huge output current will probably destroy the output rectifier after a few minutes. Thus, the technique of continuously monitoring the feedback loop and making a decision regardless of the auxiliary conditions is recognized to offer the best fault detection performance.

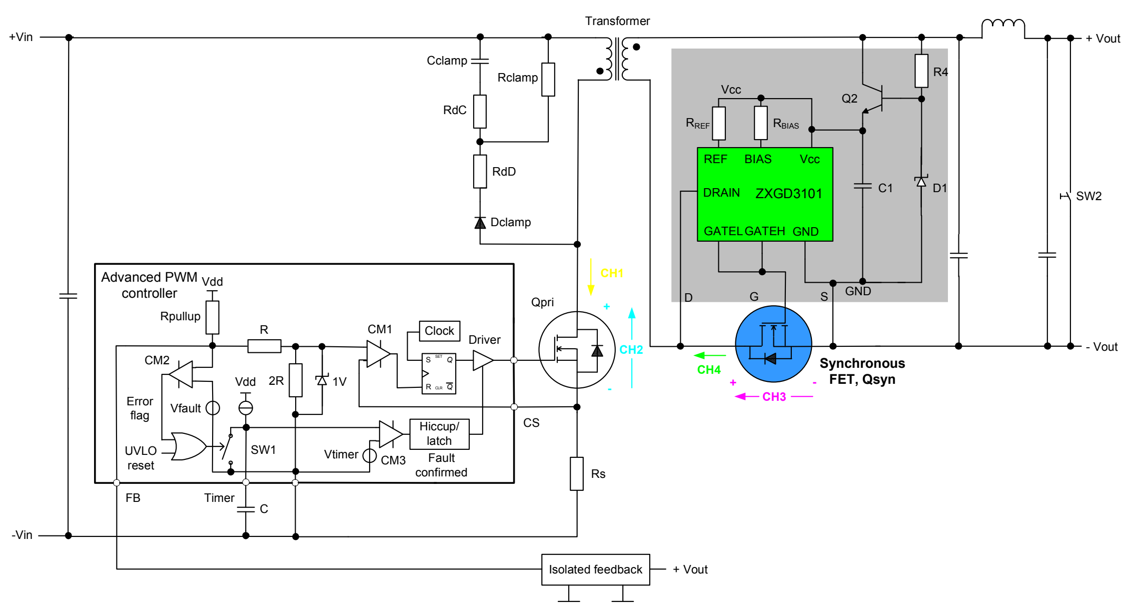

Figure 1 – PWM control with short-circuit protection for the ZXGD3101 synchronous rectification controller

The converter is protected by the primary side PWM controller in Figure 1 during the short-circuit condition. The primary side controller permanently observes the feedback signal, knowing that it should be within a certain range for regulation. If the signal goes outside this range, there must be a problem. Then an error flag is asserted, and a timer is started to delay the reaction to a fault. This is because a start-up sequence is also seen as a fault since no feedback signal appears prior to regulation. The timer is there to give a sufficient time for starting up. Typical values are in the range of 50 to 100ms.

To deliver the maximum peak current (1V over the sense resistor), the feedback pin must be in the vicinity of 3V. If it is above, close to the internal V_{dd} level, the PWM chip no longer has control over the converter. When this situation is detected by comparator CMP2, the switch SW1 opens and the external capacitor C can charge. If the fault lasts long enough, the timer capacitor voltage will reach the V_{timer} reference level, confirming the presence of a fault. The controller can then either go into auto-recovery, hiccup mode or simply totally latch off the circuit. If the fault lasts too short a time, the capacitor is reset and waits for another event.

System design considerations

In addition to employing an efficient primary PWM controller, there exists a mandatory system design criteria to fulfill a safe short-circuit as follows: Similar to the normal operation, in the indefinite period of short-circuit, a steady-state operation requires the volt-second balance across the storage element of magnetic energy, which is the power transformer in a flyback converter. Otherwise, current runaway will occur in such a way that energy rise inside the magnetics during primary MOSFET's on-time exceeds energy decay during its off-time. Thus the primary current rise abruptly saturates the magnetics, eventually leading to converter destruction.

Prior to the derivation below, all relevant defined symbols are listed in Table 1.

Table 1 – Symbol list

Symbol	Description
V_{in}	DC input voltage
V_o	Output voltage
T_{ON}	Power switch on-time
T_{ONmin}	Minimum switch on-time manageable by the PWM controller IC
T_{LEB}	Leading edge blanking duration
T_{DEL}	Propagation delay from current detection to gate off state
V_R	Secondary voltage reflected back to the primary during secondary rectifier conduction
T_{sw}	Switching period, equal to the reciprocal of the switching frequency of the converter
n	Primary-to-secondary turn ratio of the power transformer
V_F	Forward drop across the secondary rectifier

Under short-circuit condition the converter is working in the Continuous Conduction Mode (CCM). So the balance condition has to be,

$$V_{in} \times T_{ON} = V_R \times (T_{sw} - T_{ON}) \qquad \text{Equation (1)}$$

Solving equation (1) for T_{ON} yields the switch on-time,

$$T_{ON} = \frac{V_R}{V_{in} + V_R} \times T_{sw} \qquad \text{Equation (2)}$$

Note that the reflected voltage V_R is given by,

$$V_R = n \times (V_o + V_F) \qquad \text{Equation (3)}$$

Whereas in normal operation V_o is regulated and therefore V_R is constant. In case of a short-circuit, V_o drops as does V_R. Their values will be dependent on the total resistance of the secondary circuit, including diode, secondary winding wire, PCB tracks, and the short-circuit resistance. The more severe the short-circuit, the lower the total resistance, and the lower V_o.

Equation (2) shows that, in a short-circuit, T_{ON} gets shorter. If the time resulting from equation (2) is lower than T_{ONmin}, the shortest switch on-time that the controller can guarantee, which comprises the leading edge blanking duration T_{LEB} and the propagation delay from current detection to gate off state

T_{DEL}, then the controller will not be able to maintain the volt-second balance and the current will begin to rise with no control.

Combining equations (2) and (3), the runaway condition is,

$$\frac{n\times(V_o+V_F)}{V_{in}+n\times(V_o+V_F)}\times T_{sw}\le T_{ONmin} \qquad \text{Equation (4)}$$

It is possible to estimate the left side of equation (4) assuming V_o=0 (ideal short-circuit). In real-world condition V_o will be greater than zero thus T_{ON} will be in this way underestimated. Ideally, equation (4) becomes,

$$\frac{n\times V_F}{V_{in}+n\times V_F}\times T_{sw}\le T_{ONmin} \qquad \text{Equation (5)}$$

The inspection of equation (5) indicates that the conditions that favor current runaway are a high input voltage V_{in}, a high switching frequency (i.e. a shorter T_{sw}) and a high regulated output voltage: In fact, being V_R fixed by MOSFET breakdown issues, the higher V_o, the lower n.

Test results and data analysis

A synchronous rectified flyback converter with the ZXGD3101 controller in Figure 1 was tested by applying a dead short across the output terminals by closing the switch SW2 at two extremes of 90Vac and 264Vac to validate the concepts discussed above in general universal input applications. Figures 2(a) to (d) show the experimental switching waveforms for both primary and synchronous MOSFETs upon an output short-circuit at those two input voltages.

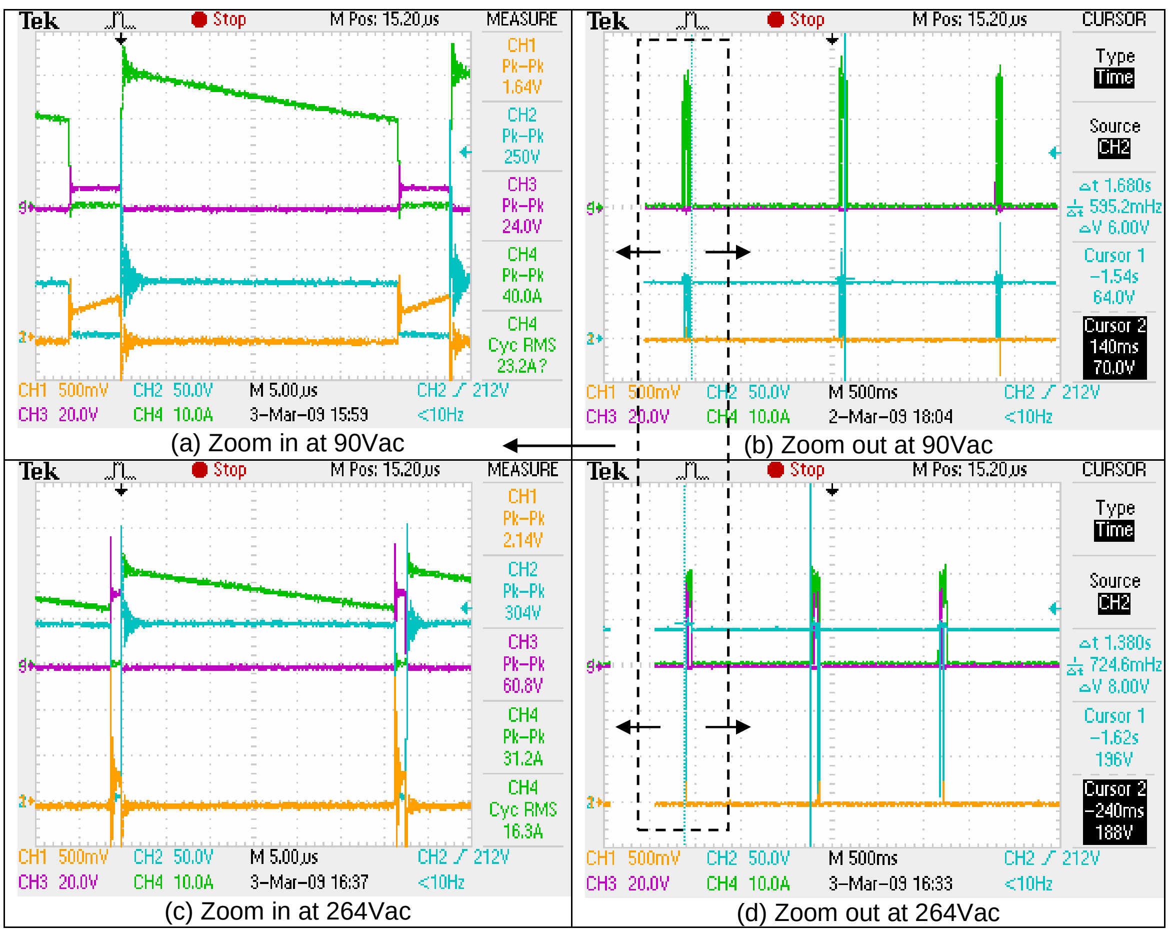

Figure 2 – Short-circuit waveforms (Orange: primary MOSFET drain current; Blue: primary MOSFET drain-source voltage; Purple: syncMOSFET drain-source voltage; Green: syncMOSFET drain current flowing through the body diode)

From Figure 2, the essential data are captured in Table 2 for the following component stress analysis while the worst case parameters are highlighted in blue for the selection guide of reliable MOSFETs.

Table 2 – Critical test results

	V_{in}=90Vac	V_{in}=264Vac
V_{DS} of primary MOSFET (peak)	500V	608V
I_D of primary MOSFET (peak)	3.9A	8.3A
V_{DS} of synchronous MOSFET (peak)	20V	56V
I_D of synchronous MOSFET (peak)	38A	25A
T_{ON}	6µs	1.25µs
T_{sw}	37.5µs	32.5µs

First of all, Figure 2 shows that the synchronous MOSFET is much more dissipative than the primary one due to the very low duty cycle. Secondly, Table 2 shows that the worst case current stress on the synchronous MOSFET occurs at the low line input voltage of 90Vac. With reference to Figure 2(a), the average drain current flowing through the MOSFET is calculated as,

$$I_{SYN(avg)} = \frac{1}{T_{sw}} \int_0^{T_{sw}-T_{ON}} \left(-\frac{I_{SYN(pk)} - I_{SYN(valley)}}{T_{sw} - T_{ON}} t + I_{SYN(pk)} \right) dt = \frac{1}{38\,\mu s} \int_0^{32\mu s} \left(-5.625 \times 10^5 t + 38 \right) dt = 24.42A$$

Originally, the resultant continuous power loss for the MOSFET with an intrinsic body diode drop of 1.25V can be as high as,

$$24.42A \times 1.25V = 30.53W$$

However, as can be seen from Figure 2(b), the PWM controller enters skip cycle mode with an on time of 0.1s over a repetitive period of 1.7s. So the effective dissipation is significantly reduced as,

$$30.53W \times \frac{0.1s}{1.7s} = 1.796W$$

In free air at the elevated temperature limit of 75°C, we must consider the typical junction-to-ambient thermal resistance $R_{THJ\text{-}A}$ of 62.5°C/W for the standard SMD D^2PAK style MOSFET. For the minimum recommended footprint (120mm^2) on a FR4, 2oz copper board, the $R_{THJ\text{-}PCB}$ value is 42°C/W and the maximum allowable power dissipation turns out to be (based on 20% design margin for the operating junction temperature),

$$P_D = \frac{\Delta T}{R_{THJ-PCB}} = \frac{T_{JMAX} \times 80\% - T_A}{R_{THJ-PCB}} = \frac{175°C \times 0.8 - 75°C}{42°C/W} = 1.548W \qquad \text{where } T_{JMAX} = 175°C$$

Thus the drain pad area has to be extended up to 1in^2 (600mm^2) to give,

$$R_{THJ-PCB} = 34°C/W \Rightarrow P_D = \frac{\Delta T}{R_{THJ-PCB}} = \frac{175°C \times 0.8 - 75°C}{34°C/W} = 1.912W > 1.796W$$

The current runaway condition should be assessed here. Recap from equation (5), it is reasonable to set V_F=1.25V for the intrinsic body diode of the synchronous MOSFET since the ZXGD3101 controller has lost its supply voltage which is directly fed from the power supply output.

Table 3 – Essential system parameters

V_{in} at 264Vac	373.4V	Customer specified
T_{sw}	32.5µs	Design variable
n	34:3	Design variable
T_{LEB}	350ns	Obtained from datasheet
T_{DEL}	120ns	Obtained from datasheet
$T_{ONmin}=T_{LEB}+T_{DEL}$	470ns	Calculated

Substituting the above numerical data into equation (5), we get,

$$T_{ON} = \frac{\frac{34}{3} \times 1.25V}{373.4V + \frac{34}{3} \times 1.25V} \times 32.5\,\mu s = 1.188\,\mu s > T_{ONmin} = 470ns$$

It is found that the current runaway can be avoided. Otherwise, there are two suggested options as a result of altering the primary inductance of the power transformer in this quasi-resonant converter as below:

1. Decrease the switching frequency
2. Increase the primary-to-secondary turn ratio

Conclusion

The instantaneous voltage, current and thermal stresses of switching MOSFETs should be taken into account at the output short-circuit instant. This application note describes a systematic approach to check if pulse skipping methods of output short-circuit protection in synchronous rectified flyback converters are suitable and adequate when used with the ZXGD3101 controller. It requires an appropriate selection of the primary PWM controller in conjunction with a thorough consideration of the current runaway condition as well as the power loss in the synchronous MOSFET. The mathematical analysis removes the need to have an experimental trial-and-error method which may be destructive if the under-rated MOSFETs have been used during the development stage.

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