



### 40V P-CHANNEL ENHANCEMENT MODE MOSFET PowerDI3333-8

### **Product Summary**

BV <sub>DSS</sub>	R <sub>DS(ON)</sub> Max	I <sub>D</sub> Max T <sub>A</sub> = +25°C		
-40V	$13m\Omega$ @ V <sub>GS</sub> = -10V	-10.3A		
-40V	$18m\Omega$ @ V <sub>GS</sub> = -4.5V	-8.8A		

## **Description and Applications**

This MOSFET is designed to meet the stringent requirements of automotive applications. It is qualified to AEC-Q101, supported by a PPAP and is ideal for use in:

- · Reverse-polarity protections
- Power-management functions
- DC-DC converters

### **Features and Benefits**

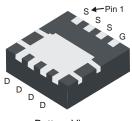
- Low R<sub>DS(ON)</sub> Ensures On-State Losses are Minimized
- Small Form Factor Thermally Efficient Package Enables Higher Density End Products
- Occupies 33% of the Board Area Occupied by SO-8, Enabling Smaller End Product
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- The DMP4013LFGQ is suitable for automotive applications requiring specific change control; this part is AEC-Q101 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.

https://www.diodes.com/quality/product-definitions/

### **Mechanical Data**

- Package: PowerDI<sup>®</sup>3333-8
- Package Material: Molded Plastic, "Green" Molding Compound.
   UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Diagram
- Terminals: Finish Matte Tin Annealed over Copper Leadframe.
   Solderable per MIL-STD-202, Method 208 (3)
- Weight: 0.034 grams (Approximate)

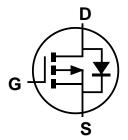
#### PowerDI3333-8



Bottom View



Top View



**Equivalent Circuit** 

### Ordering Information (Note 4)

Part Number	Package	Packing		
Part Number	Fackaye	Qty.	Carrier	
DMP4013LFGQ-7	PowerDI3333-8	2000	Tape & Reel	
DMP4013LFGQ-13	PowerDI3333-8	3000	Tape & Reel	

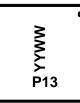
Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.



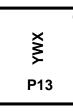
## **Marking Information**

Site 1



P13 = Product Type Marking Code YYWW = Date Code Marking YY = Last Two Digits of Year (ex: 23 = 2023) WW = Week Code (01 to 53)

Site2



P13 = Product Type Marking Code YWX = Date Code Marking Y = Year (ex: 3 = 2023) W = Week (ex: a = Week 27; z Represents Week 52 and 53) X = Internal Code (ex: U = Monday)

## **Maximum Ratings** (@ $T_A = +25$ °C, unless otherwise specified.)

Characteristic	Symbol	Value	Units		
Drain-Source Voltage			VDSS	-40	V
Gate-Source Voltage			Vgss	±20	V
Continuous Preis Correct (Note CV)	Steady State	$T_A = +25$ °C $T_A = +70$ °C	lD	-10.3 -8.3	А
Continuous Drain Current (Note 6) V <sub>GS</sub> = -10V	t < 10s	$T_A = +25$ °C $T_A = +70$ °C	lD	-13.7 -11	А
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%	I <sub>DM</sub>	-80	Α		
Maximum Continuous Body Diode Forward Current	Is	-10.3	Α		
Avalanche Current, L = 0.1mH			IAS	-34	Α
Avalanche Energy, L = 0.1mH	E <sub>AS</sub>	58	mJ		

## Thermal Characteristics (@TA = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units		
Total Power Dissipation (Note 5)		PD	1	W	
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	ReJA	123	°C/W	
Thermal Resistance, Junction to Ambient (Note 5)	t < 10s	КөЈА	69	C/VV	
Total Power Dissipation (Note 6)		PD	2.1	W	
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	Reja	60		
t < 10s		Көја	34	°C/W	
Thermal Resistance, Junction to Case (Note 6)		$R_{ heta JC}$	3.3		
Operating and Storage Temperature Range		TJ, TSTG	-55 to +150	°C	

Notes: 5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.

<sup>6.</sup> Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.



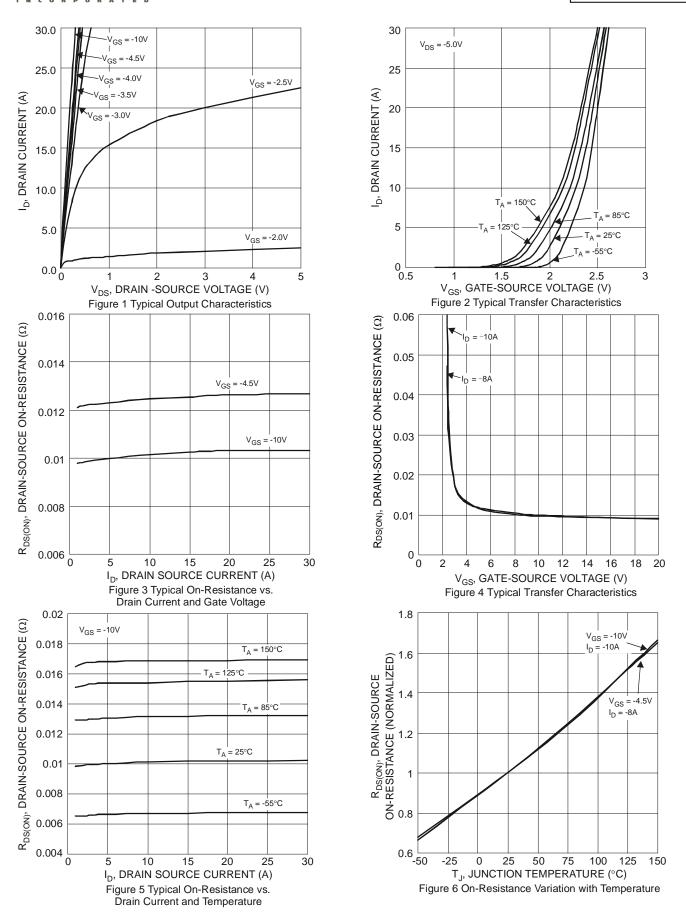
# Electrical Characteristics (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 7)							
Drain-Source Breakdown Voltage		-40	_	_	V	$V_{GS} = 0V, I_{D} = -250\mu A$	
Zero Gate Voltage Drain Current TJ = +25°C	IDSS	_	_	-1	μA	V <sub>DS</sub> = -40V, V <sub>GS</sub> = 0V	
Gate-Source Leakage	I <sub>GSS</sub>	_	_	±100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 7)							
Gate Threshold Voltage	Vgs(TH)	-1	_	-3	V	$V_{DS} = V_{GS}$ , $I_D = -250\mu A$	
Static Drain-Source On-Resistance	Present	_	9.4	13	mΩ	$V_{GS} = -10V, I_{D} = -10A$	
Static Dialii-Source Off-Resistance	R <sub>DS(ON)</sub>	_	12.3	18	m77	$V_{GS} = -4.5V, I_{D} = -8A$	
Diode Forward Voltage	VsD	_	-0.7	-1.2	V	V <sub>G</sub> S = 0V, I <sub>S</sub> = -1A	
DYNAMIC CHARACTERISTICS (Note 8)							
Input Capacitance	Ciss	_	3426	_	pF	\/ 20\/ \/ 0\/	
Output Capacitance	Coss	_	283	_	pF	V <sub>DS</sub> = -20V, V <sub>GS</sub> = 0V, f = 1MHz	
Reverse Transfer Capacitance	Crss	_	235	_	pF	1 – 11011 12	
Gate Resistance	$R_g$	_	4.7	_	Ω	$V_{DS} = 0V$ , $V_{GS} = 0V$ , $f = 1MHz$	
Total Gate Charge (V <sub>GS</sub> = -4.5V)	$Q_g$	_	32.5	_	nC		
Total Gate Charge (V <sub>GS</sub> = -10V)	Qg	_	68.6	_	nC	\/ 20\/ I- 40A	
Gate-Source Charge	Qgs	_	8.2	_	nC	$V_{DS} = -20V, I_{D} = -10A$	
Gate-Drain Charge	$Q_{gd}$	_	9.9	_	nC		
Turn-On Delay Time	t <sub>D(ON)</sub>	_	5.3	_	ns		
Turn-On Rise Time	tR	_	20	_	ns	V <sub>DD</sub> = -20V, V <sub>GEN</sub> = -10V,	
Turn-Off Delay Time	tD(OFF)	_	126	_	ns	$R_G = 3\Omega$ , $I_D = -10A$	
Turn-Off Fall Time	tF	_	83	_	ns	]	
Body Diode Reverse-Recovery Time	t <sub>RR</sub>	_	19.5	_	ns		
Body Diode Reverse-Recovery Charge	Qrr	_	9.8	_	nC		

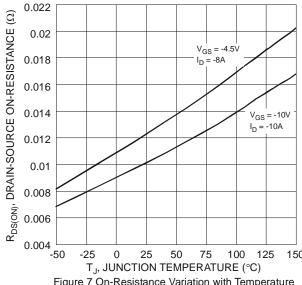
Notes:

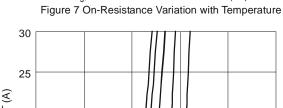
<sup>7.</sup> Short duration pulse test used to minimize self-heating effect. 8. Guaranteed by design. Not subject to product testing.

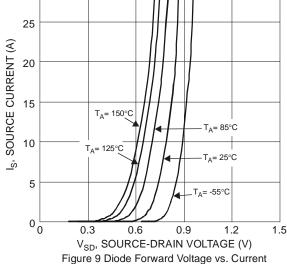


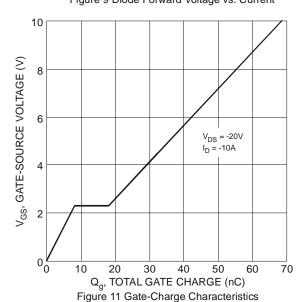












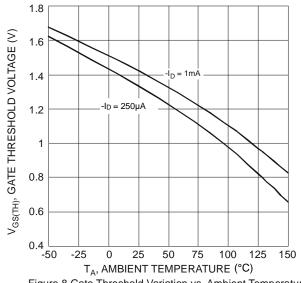
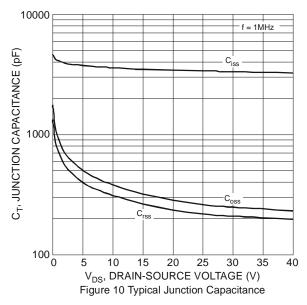
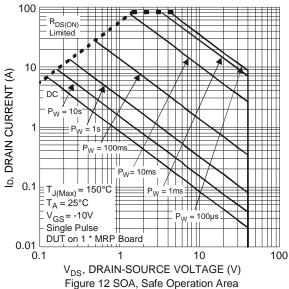
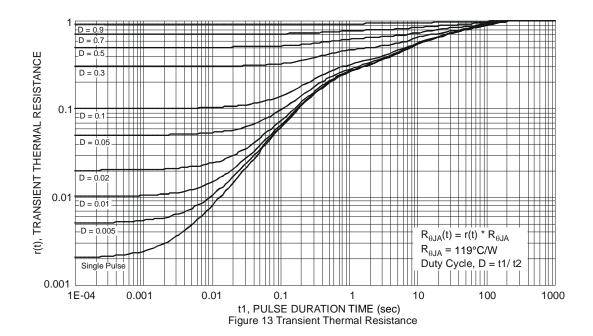


Figure 8 Gate Threshold Variation vs. Ambient Temperature







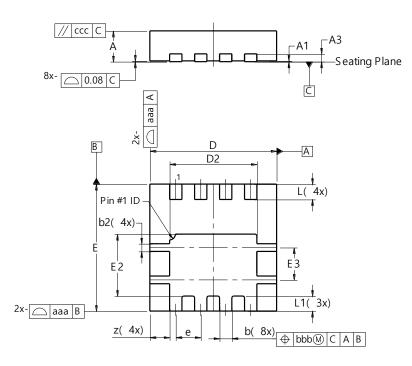




## **Package Outline Dimensions**

Please see http://www.diodes.com/package-outlines.html for the latest version.

### PowerDI3333-8

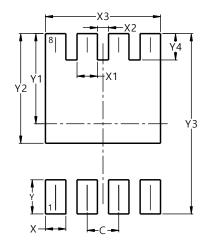


PowerDI3333-8					
Dim	Min	Max	Тур		
Α	0.75	0.85	0.80		
A1	0.00	0.05	0.02		
A3	_	_	0.203		
b	0.27	0.37	0.32		
b2	-	_	0.20		
D	3.25	3.35	3.30		
D2	2.22	2.32	2.27		
Е	3.25	3.35	3.30		
E2	1.56	1.66	1.61		
E3	0.79	0.89	0.84		
е	-	_	0.65		
L	0.35	0.45	0.40		
L1	_	_	0.39		
Z	0.515				
aaa	0.25				
bbb	0.10				
CCC	0.10				
All Dimensions in mm					

## **Suggested Pad Layout**

Please see http://www.diodes.com/package-outlines.html for the latest version.

### PowerDI3333-8



Dimensions	Value (in mm)		
С	0.650		
X	0.420		
X1	0.420		
X2	0.230		
Х3	2.370		
Y	0.700		
Y1	1.850		
Y2	2.250		
Y3	3.700		
Y4	0.540		



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