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Chapter 1 Summary

1.1 General Description

The 140W ACF PD3.1 EPR (28V) Evaluation Board is composed of three main controllers, AP3306, APR3401 and AP43771H. The AP3306 is a highly integrated Active Clamp Flyback (ACF) controller that is optimally designed for offline power supply to meet ultra-low standby power, high power density, and comprehensive protection requirements. The APR3401 is a secondary side Synchronous Rectification (SR) Controller. The AP43771H, a protocol decoder in charge of matching the associated charger capacity and request by an attached USB Type-C® equipped device under charged (DUC), regulates the feedback network of the charger to fulfill voltage and current requirements from DUC. In addition, Gallium Nitride (GaN) FET is employed to further improve the efficiency and thermal performance.

1.2 Key Features

1.2.1 System Key Features

- Diodes Incorporated (Diodes) Patented ACF Topology Implementation for Critical Efficiency Improvement Approaches
- Cost-Effective Implementation for High Efficiency High Power Density Charger
- High-Voltage Startup and low standby power (<80mW)
- Meets DOE VI and COC Tier 2 Efficiency Requirements
- USB Type-C Port - Supports the Maximum Output of 140W PD3.1 Function and AVS 28V with 100mV/step
- SSR Topology Implementation with an Optocoupler for Accurate Step Voltage Controlling
- Low overall system BOM cost

1.2.2 AP3306 Key Features

- Active Clamp Flyback Topology with Recycled Leakage Energy and Zero Voltage Switching Functions
- High-Voltage Startup
- Embedded VCC LDO for VCCL pin to Guarantee Wide Range Output Voltage
- Constant, Low Output Current in Output Short Situation
- Non-Audible-Noise Quasi-Resonant Control
- Soft Start During Startup Process
- Frequency Foldback for High Average Efficiency
- Secondary Winding Short Protection with FOCP
- Frequency Dithering for Reducing EMI
- X-CAP Discharge Function
- Useful Pin fault protection:
  SENSE Pin Floating Protection/
  FB/Optocoupler Open/Short Protection
- Comprehensive System Protection Feature:
  VOVP/OLP/BNO/SOVP/SSCP

1.2.3 APR3401 Key Features

- Synchronous Rectification Works with DCM/QR/ACF operation modes
- Eliminate Resonant Ringing Interference
- Fewest External Components used

1.2.4 AP43771H Key Feature

- Support USB PD Rev 3.1
- MTP for System Configuration
- OTP for Main Firmware
- Operating Voltage Range: 3.3V to 28V
- Built-In Regulator for CV and CC Control
- Programmable OVP/UVP/OCP/OTP
- Support Power Saving Mode
- External N-MOSFET Control for VBUS Power Delivery
- Support e-Marker Cable Detection
- W-DFN3030-14 package

1.3 Applications

- Type-C USB PD3.1 (EPR) 28V chargers

1.4 Main Power Specifications

Parameter	Value
Input Voltage	$90V_{AC}$ to $264V_{AC}$
Input standby power	< 80mW
Main Output (Vo / Io)	PDO: 5V/3A, 9V/3A, 15V/3A, 20V/3A, 28V/5A
	AVS: 15V-28V/5A
Voltage Step	AVS 15V to 28V, 100mV/step
Efficiency	Comply with CoC version 5 tier-2
Total Output Power	140 W (at PDO 28V @ 5A)
Protections	OCP, OVP, UVP, OLP, OTP, SCP
Dimensions	PCB: 84 * 55 * 23 mm^3, (3.307” * 2.165” * 0.906” inch$^{3)}$ Case: 88 * 59 * 27 mm^3, 140.18CC, (3.465” * 2.323” * 1.063”, 8.556 CI, 16.36 W/C.I.)
Power Density Index	1.00 W/CC; 16.36 W/CI

1.5 Evaluation Board Picture

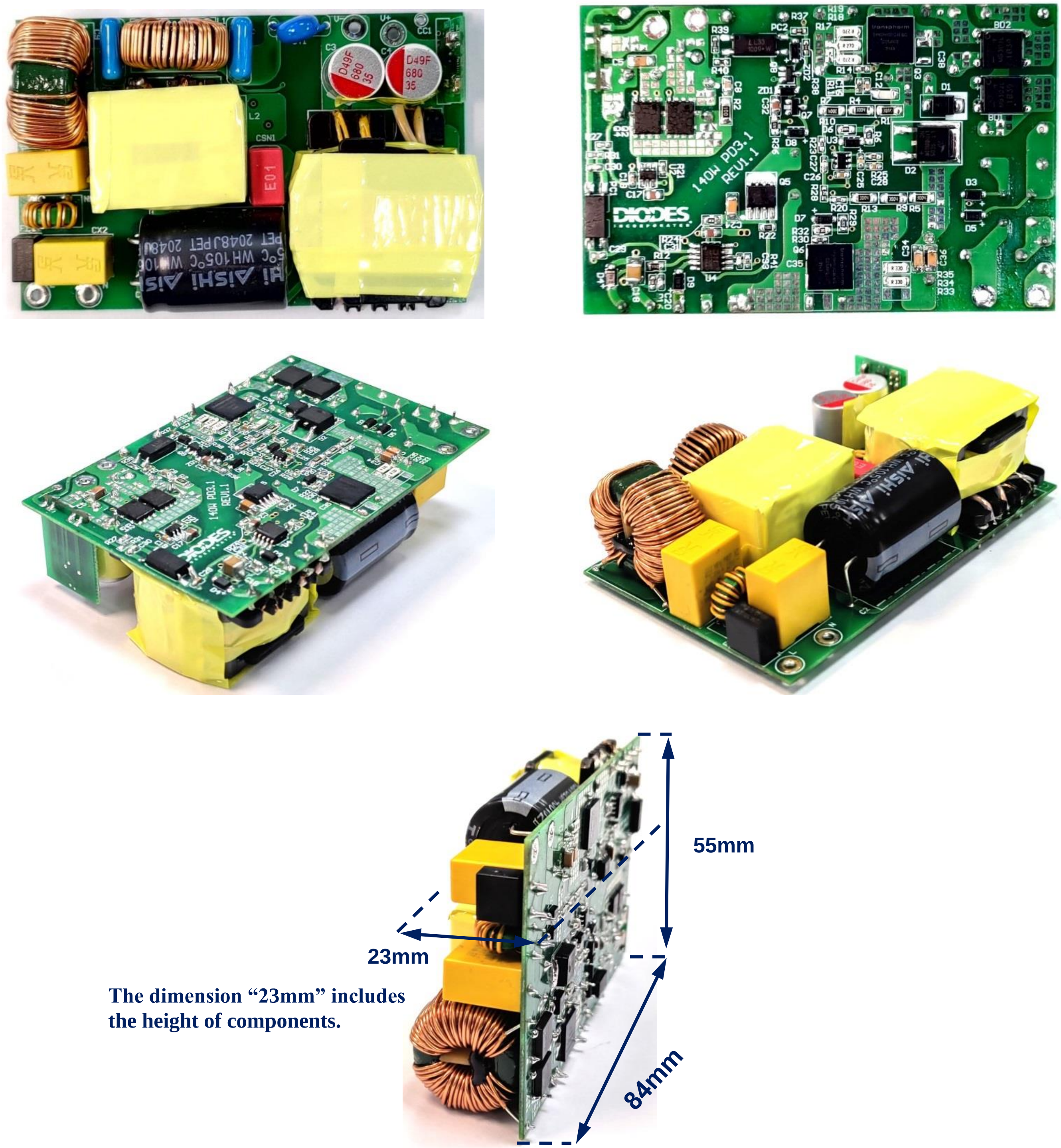


Figure 1. Photos of 140W ACF+GaN PD3.1 AVS Adapter EVB

Chapter 2 Power Supply Specification

2.1 Specification and Test Results

Parameter	Value	Test Summary
Input Voltage / Frequency	90V_{AC} to 264V_{AC} / 50Hz or 60Hz	Test Condition
Input Current	<2A_{RMS}	
Standby Power	< 80mW, load disconnected	**PASS,** 50.552mW@230VAC/50Hz
5V/3A Average Efficiency	CoC Version 5, Tier-2 Efficiency >81.84%	**PASS,** 89.01%@115VAC/60Hz 89.84%@230VAC/50Hz
5V/0.3A Efficiency (10% Load)	CoC Version 5, Tier2 Efficiency >72.48%	**PASS,** 86.02%@115VAC/60Hz 85.22%@230VAC/50Hz
9V/3A Average Efficiency	CoC Version 5,Tier2 Efficiency >87.30%	**PASS,** 92.39%@115VAC/60Hz 92.79%@230VAC/50Hz
9V/0.3A Efficiency (10% Load)	CoC Version 5,Tier2 Efficiency >77.30%	**PASS,** 89.21%@115VAC/60Hz 88.89%@230VAC/50Hz
15V/3A Average Efficiency	CoC Version 5,Tier2 Efficiency >88.85%	**PASS,** 93.64%@115VAC/60Hz 94.05%@230VAC/50Hz
15V/0.3A Efficiency (10% Load)	CoC Version 5,Tier2 Efficiency >78.85%	**PASS,** 89.66%@115VAC/60Hz 89.96%@230VAC/50Hz
20V/5A Average Efficiency	CoC Version 5,Tier2 Efficiency >89%	**PASS,** 93.63%@115VAC/60Hz 94.28%@230VAC/50Hz
20V/0.5A Efficiency (10% Load)	CoC Version 5,Tier2 Efficiency >79%	**PASS,** 91.64%@115VAC/60Hz 90.68%@230VAC/50Hz
28V/5A Average Efficiency	CoC Version 5,Tier2 Efficiency >89%	**PASS,** 93.59%@115VAC/60Hz 94.46%@230VAC/50Hz
28V/0.5A Efficiency (10% Load)	CoC Version 5,Tier2 Efficiency >79%	**PASS,** 90.87%@115VAC/60Hz 89.86%@230VAC/50Hz
Output Voltage Regulation Tolerance	+/- 5%	**PASS,**
5V→9V / 9V→15V / 15V→20V / 20V →28V	Rise time : 0~275ms (PD SPEC)	**PASS,**

2.2 Compliance

Parameter	Test Conditions	Low to High	High to Low	Standard	Test Summary
Output Voltage Transition time	5V/3A to 9V/3A, 90Vac/60Hz	70.24ms	78.59ms	<275ms	Pass
	5V/3A to 9V/3A, 264Vac/50Hz	75.67ms	79.4ms		Pass
	9V/3A to 15V/3A, 90Vac/60Hz	96.64ms	96.32ms		Pass
	9V/3A to 15V/3A, 2640Vac/50Hz	86.73ms	88.57ms		Pass
	15V/3A to 20V/3A, 90Vac/60Hz	93.31ms	87.65ms		Pass
	15V/3A to 20V/3A, 264Vac/50Hz	74.84ms	71.19ms		Pass
	20V/3A to 28V/3A, 90Vac/60Hz	94.47ms	94.22ms		Pass
	20V/3A to 28V/3A, 264Vac/50Hz	93.57ms	95.12ms		Pass
Output Connector	USB Type-C *1-				
Temperature	25℃				
Dimensions (W /D/ H)	84mm x55mm x 23mm				

Chapter 3 Schematic

3.1 Board Schematic

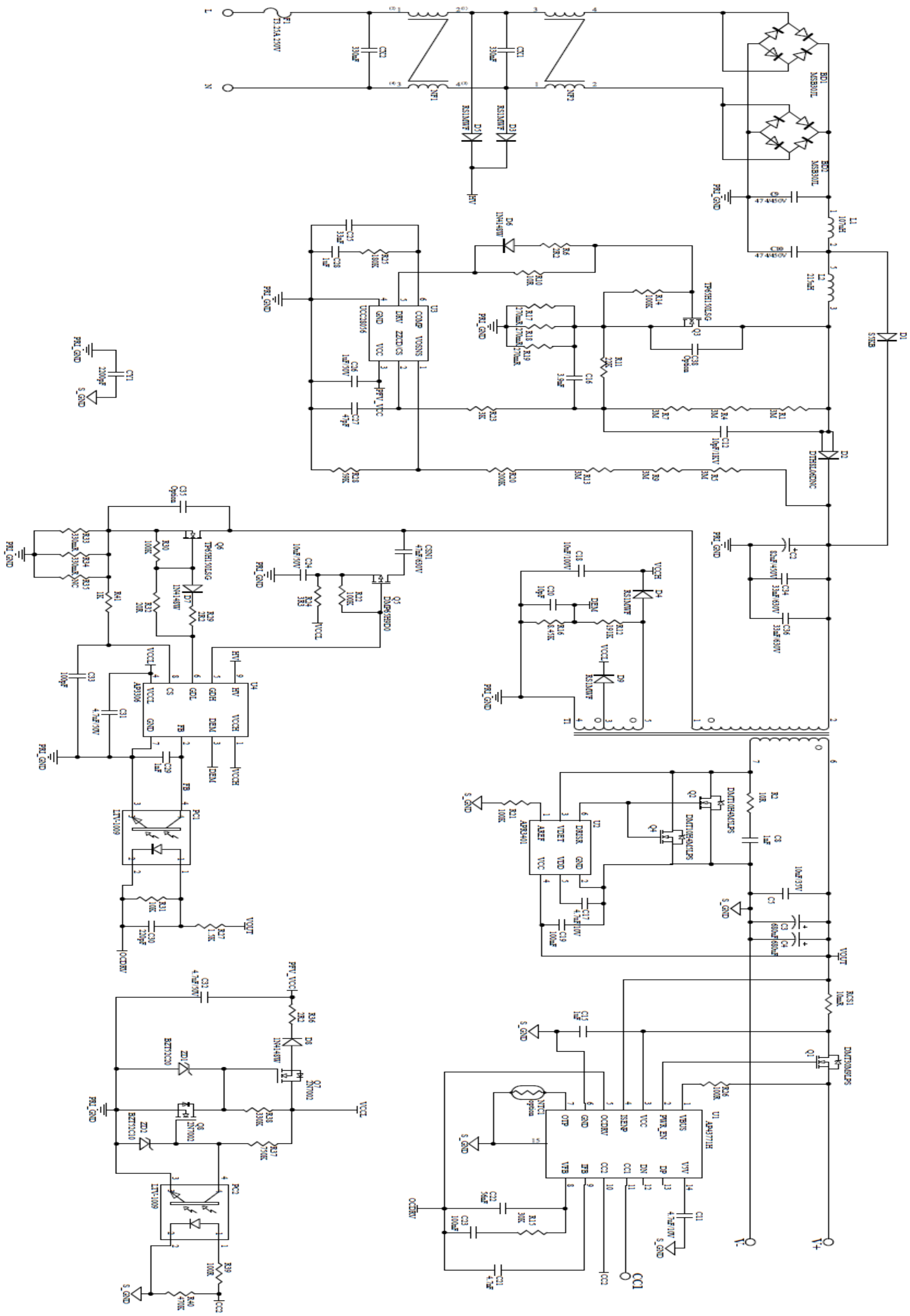


Figure 2. Schematic of 140W ACF+GaN PD3.1 AVS Adapter EVB

3.2 Bill of Material (BOM)

Item	Quantity	Reference	Description	Manufacturer Part Number	Manufacturer
1	**1**	**U1**	**AP43771H PD controller**	**AP43771H**	**Diodes Incorporated (Diodes)**
2	**1**	**U2**	**APR3401, SR Controller**	**APR3401**	**Diodes**
3	**1**	**U4**	**AP3306, Active Clamping Flyback Controller**	**AP3306S10-13**	**Diodes**
4	1	U3	UCC28056, CRM/DCM PFC Controller IC	UCC28056-6	Texas Instruments
5	**1**	**Q1**	**MOSFET, N-CH, 30V, DMT30M9LPS**	**DMT30M9LPS**	**Diodes**
6	**1**	**Q5**	**High-Side Switch MOSFET, P-CH, 650V, SO-8, DMP65H9D0HSS-13**	**DMP65H9D0 SOP-8**	**Diodes**
7	**2**	**Q7, Q8**	**MOSFET, N-CH, 60V, SOT-23, 2N7002-7-F**	**2N7002-7-F**	**Diodes**
8	**2**	**Q2, Q4**	**MOSFET, N-CH, 100V, DMT10H4M5LPS**	**DMT10H4M5LPS**	**Diodes**
9	2	Q3, Q6	Low-Side Switch GaN, 650V, PQFN 8X8, TP65H150G4LSG	TP65H150G4LSG	Transphorm*
10	**2**	**BD1, BD2**	**Bridge 3A 600V MSB30JL**	**MSB30JL**	**Diodes**
11	**1**	**D1**	**Surface Mount Glass Passivated Rectifier, 5A, 800V, SMB, S5KC**	**S5KC**	**Diodes**
12	**1**	**D2**	**Hyper-Fast Epitaxial Rectifier, 8A, 600V, TO252, DTH8L06DNC**	**DTH8L06DNC**	**Diodes**
13	**4**	**D3, D4, D5, D9**	**Fast Rectifier, 1A, 1000V, SOD-123, RS1MWF**	**RS1MWF-7**	**Diodes**
14	**3**	**D6, D7, D8**	**Switching Diode, SWD, 150mA, 75V, SOD123, 1N4148W**	**1N4148W-7-F**	**Diodes**
15	**1**	**ZD1**	**BZT52C20_Zener Diode_20V_SOD123**	**BZT52C20-7-F**	**Diodes**
16	**1**	**ZD2**	**BZT52C10_Zener Diode_10V_SOD123**	**BZT52C10-7-F**	**Diodes**
17	1	C2	EC 82µF 450V 18x25-P7.5	EWH2WM820M25OTE	AiShi
18	2	C3, C4	EC 680µF 35V 10x16 polymer	SPF1VM681G16O00raxxx	AiShi
19	1	C5	MLCC 10µF 35V 1206 X7R		
20	1	C8	MLCC 1nF 200V 0805 X7R		
21	2	C9, C10	Plastic Cap 474/450V, CM-12.5X4.5-P10	FPS22W474K4R	Nitsuko
22	2	C11, C17	MLCC 4.7µF 10V 0805 X7R		
23	1	C12	MLCC 10pF 1kV 1206 X7R		
24	1	C15	MLCC 1µF 50V 0805 X7R		
25	1	C16	MLCC 3.9nF 50V 0603 X7R		
26	1	C18	MLCC 10µF 100V 1210 X7R		
27	1	C19	MLCC 100nF 50V 0603 X7R		
28	1	C20	MLCC 10pF 50V 0603 X7R		

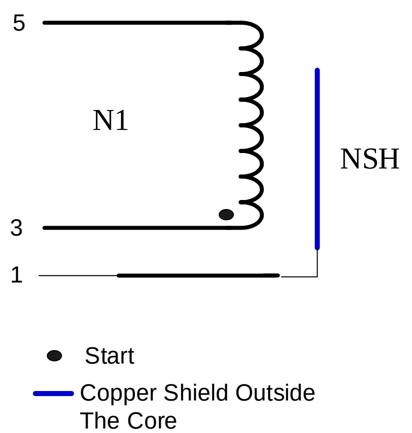
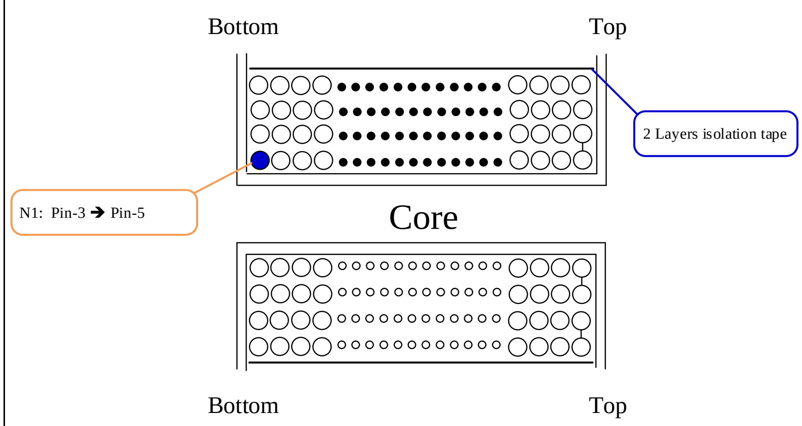
29	1	C21	MLCC 4.7nF 50V 0603 X7R		
30	1	C23	MLCC 100nF 50V 0603 X7R		
31	1	C22	MLCC 56nF 50V 0603 X7R		
32	1	C24	MLCC 10µF 50V 1206 X7R		
33	1	C25	MLCC 33nF 50V 0603 X7R		
34	2	C26, 28	MLCC 1µF 50V 0603 X7R		
35	1	C27	MLCC 47pF 50V 0603 X7R		
36	1	C29	MLCC 1nF 50V 0603 X7R		
37	1	C30	MLCC 220pF 50V 0603 X7R		
38	2	C31, C32	MLCC 4.7µF 50V 0805 X7R		
39	1	C33	MLCC 100pF 50V 0603 X7R		
40	2	C34, C36	MLCC 33nF 1KV 1206 X7R		
41	1	CSN1	Plastic Cap 47nF 630V, CM-11X6-P7.5mm		
42	2	CX1, CX2	X2 0.33µF AC275V 13 x 8mm-P7.5mm	MKP-34K0275AB110SH6	HJC
43	1	CY1	Y1 2200pF AC300V	YU0AH222M090DAMD0H	Walsin
44	1	F1	Fuse T3.15A 250V Time Lag		
45	1	T1	POT33, 450µH, 32:5:6:11		
46	1	L1	Inductor 107µH		
47	1	L2	Inductor 215µH		
48	1	NF1	CM Choke, 140µH, T9x5x3, φ0.5*6.5 turns.	TL-20042402T02TA	FTGI
49	1	NF2	CM Choke T20x10x10		
50	1	NTC1	NTC 100K 0603 (Option)	NTCG103JF103FT1S	TDK
51	2	PC1, PC2	Optocoupler	TLV-1009	LITE ON
52	6	R1, R4, R5, R7, R9, R13	RES 3M 1206 1%		RALEC, TA-I
53	1	R2	RES 10R 1206 5%		RALEC, TA-I
54	3	R6, R29, R36	RES 2R2 0805 1%		RALEC, TA-I
55	1	R10	RES 10R 0603 5%		RALEC, TA-I
56	1	R11	RES 22K 0603 5%		RALEC, TA-I
57	1	R12	RES 191K 0805 1%		RALEC, TA-I
58	4	R14, R21, R22, R30	RES 100K 0603 1%		RALEC, TA-I
59	1	R15	RES 30K 0603 1%		RALEC, TA-I
60	1	R16	RES 8.45K 0603 1%		RALEC, TA-I
61	3	R17, R18, R19	RES 270mR 1206 1% 1W	SMD12A1FR270T	Sart Tech
62	1	R20	RES 200K 0603 1%		RALEC, TA-I

63	1	R23	RES 3K 0603 1%		RALEC, TA-I
64	1	R24	RES 3R3 0805 1%		RALEC, TA-I
65	1	R25	RES 180K 0603 5%		RALEC, TA-I
66	1	R26	RES 100R 0805 1%		RALEC, TA-I
67	1	R27	RES 1.5K 0603 1%		RALEC, TA-I
68	1	R28	RES 59K 0603 1%		RALEC, TA-I
69	1	R31	RES 10K 0603 1%		RALEC, TA-I
70	1	R32	RES 20R 0805 1%		RALEC, TA-I
71	2	R33, R34	RES 330mR 1206 1% 1W	SMD12A1FR330T	Sart Tech
72	1	R37	RES 750K 0603 1%		RALEC, TA-I
73	1	R38	RES 330K 0603 1%		RALEC, TA-I
74	1	R39	RES 100R 0603 1%		RALEC, TA-I
75	1	R40	RES 470K 0603 1%		RALEC, TA-I
76	1	R41	RES 1K 0603 1%		RALEC, TA-I
77	1	RCS1	RES 10mR 1206 1% Low CTR type	SMF12M1FR010T	Sart Tech

SuperGaN® Power FETs is a trademark of Transphorm Incorporated.
Detailed product information can be found on https://www.transphormusa.com.

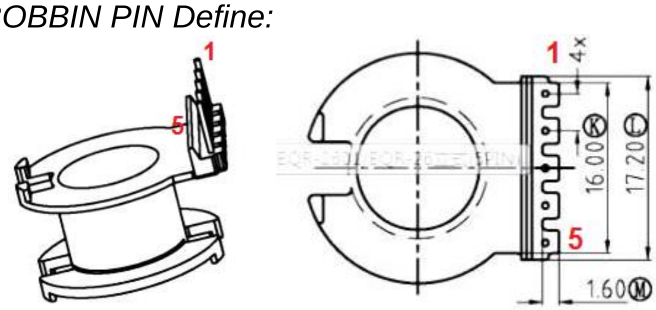
3.3 PFC Inductance, Transformer Design

3.3.1 PFC Inductance

Schematic	Structure
	

Definition	Pin define (Start >> End)	Wire (φ)	No. of Turns	Layers	Layers of Tape
N1	3 → 5	2UEW Litz Wire, 0.1mm x 50, 1P, Bot -> Top -> Bot-> Top	40	4	2 L
NSH	Core → 1	10mm width copper, 1P wrapped outside the core	1	1	1 L

BOBBIN PIN Define:

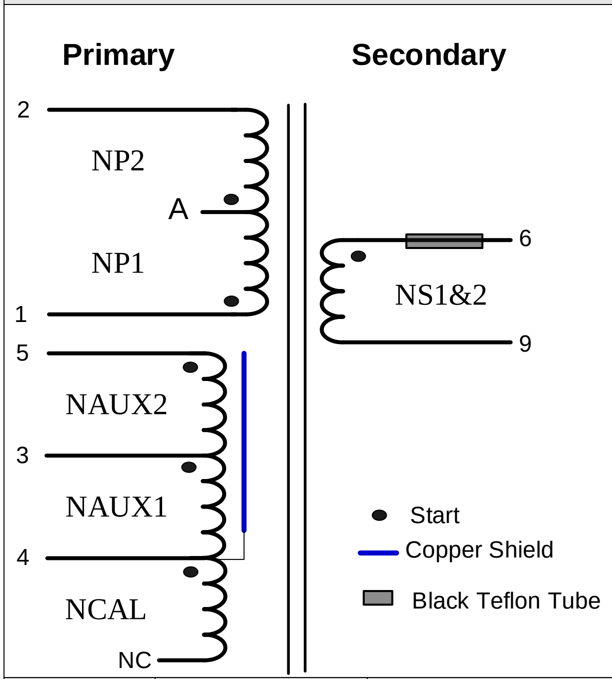


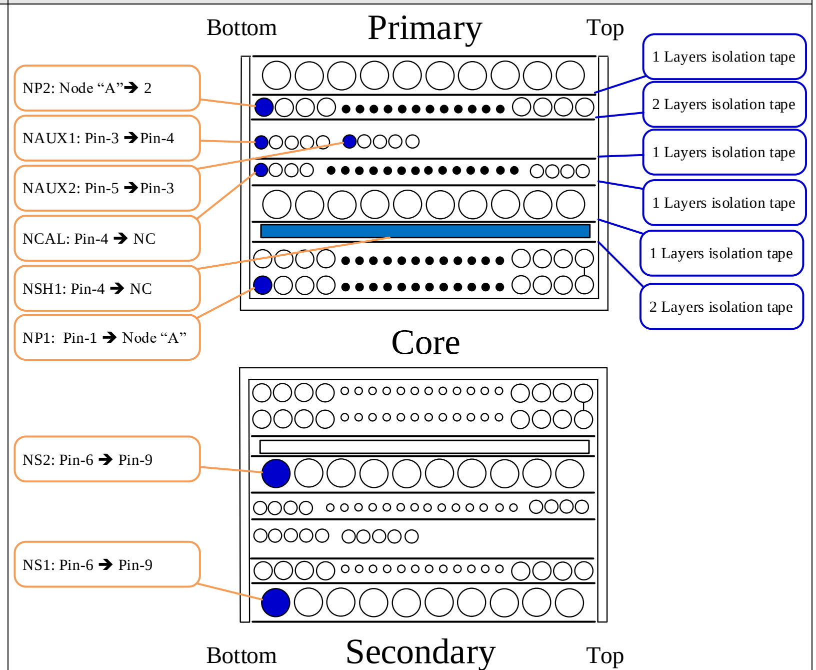
Inductance	Pin 3-5, measured at 100kHz / 1V	215µH+/- 5%
Note	Core：NH96 from LIANFENG MEGNET INDUSTRY	

3.3.2 Transformer Design

Schematic

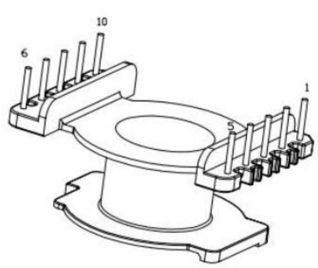
Structure





Definition	Pin define (Start >> End)	Wire (φ)	No. of Turns	Layers	Layers of Tape
NP1	1 → A	2UEW Litz Wire, 0.1mm x 30, 1P, Bot -> Top -> Bot	22	2	2 L
NSH1	4 → NC	10mm width copper, 1P	1	1	1 L
NS1	6→ 9	Triple Insulated Litz Wire, 0.25mm x 7P, 2P	5	1	1 L
NCAL	4 → NC	2UEW, 0.13mm , 1P	38	1	1 L
NAUX1	3 → 4	2UEW, 0.13mm , 1P	5	1	2 L
NAUX2	5 → 3	2UEW, 0.13mm , 1P	6		
NP2	A → 2	2UEW Litz Wire, 0.1mm x 30, 1P, Bot -> Top	10	1	1L
NS2	6 → 9	Triple Insulated Litz Wire, 0.25mm x 7P, 2P	5	1	1 L

BOBBIN PIN Define:



Primary Inductance	Pin 1-2,all other windings open, measured at 100kHz / 1V	450µH+/- 5%
Note	Core：NH96 from LIANFENG MEGNET INDUSTRY Or JPP-96 from A-CORE JIANGMEN ELECTRONICS	

3.4 Schematics Description

3.4.1 AC Input Circuit & EMI Filter

The Fuse F1 protects against overcurrent conditions which occur when some main components fails. The NF1 and NF2 are common mode chocks for the common mode noise suppression. The BD1 & BD2 are bridge rectifiers which convert alternating current and voltage into direct current and voltage. The CX1 & CX2, C9 & C10, L1 are proposed to filter the differential switching noise back to AC source.

3.4.2 UCC28056 PFC Controller

The UCC28056 device drives PFC boost stages based on an innovative mixed mode method that operates in transition mode (TM) at full load and transitions into seamlessly discontinuous conduction mode (DCM) at reduced load, automatically reducing switching frequency.

To further improve standby power consumption and low voltage output efficiency, UCC28056 VCC is disabled by AP43771H when the VBUS is below 15V.

3.4.3 AP3306 PWM Controller

AP3306, a highly integrated Active Clamp Flyback (ACF) controller, integrates high-voltage start-up function through HV pin and X-Cap discharging function. It also integrates a VCCL LDO circuit, which allows the LDO to regulate the wide range VCCL to an acceptable value. This makes AP3306 an ideal candidate for wide range output voltage applications such as USB-PD3.1 EPR. With embedded high-side and low-side switch control mechanism, AP3306 provides proper timing sequences to control Q5 (high-side Switch) and Q6 (low-side Switch) operations to implement two key efficiency improvement approaches, namely, ZVS (Zero Voltage Switching) and leakage energy recycling (stored in Csn) to achieve high-power density charger applications. At no load or light load, the AP3306 will enter the burst mode to minimize standby power consumption.

3.4.4 APR3401 Synchronous Rectification (SR) MOSFET Driver

As a high performance solution, APR3401 is a secondary side SR controller to effectively reduce the secondary side rectifier power dissipation which works in DCM operation.

3.4.5 AP43771H PD 3.1 Decoder & Protection on/off N MOSFET and Interface to Power Devices

Important pins provide critical protocol decoding and regulation functions in AP43771H:

1) **CC1 (Pin 11)**: CC1 (Configuration Channel 1) is defined by USB Type-C spec to provide the channel communication link between power source and sink device.
2) **CC2 (Pin 10)**: CC2 (Configuration Channel 2) is responsible for turning off the VCC of UCC28056 when the VBUS is below 15V to further improve standby power consumption and low voltage output efficiency.
3) **Constant Voltage (CV)**: The CV is implemented by sensing VFB (pin 8) and comparing with internal reference voltage to generate a CV compensation signal on the OCDRV pin (pin 5). The output voltage is controlled by firmware through CC1/CC2 channel communication with the sink device.
4) **Constant Current (CC)**: The CC is implemented by sensing the current sense resistor (RCS, 10mΩ, 1%, Low TCR) and compared with internal programmable reference voltage. The output current is controlled by firmware through CC1/CC2 channel communication with the sink device.
5) **Loop Compensation:**
R115 & C22 & C23 from the voltage loop compensation circuit, and C21 form the current loop compensation circuit.
6) **OCDRV (Pin5)**: It is the key interface link from secondary decoder (AP43771H) to primary regulation circuit (AP3306). It is connected to optocoupler PC1 Pin 2 (Cathode) for feedback information based on all sensed CC1 & CC2 signals for getting desired Vbus voltage and current.
7) **PWR_EN (Pin2) to N-MOSFET Gate**: The pin is used to turn on/off N-MOSFET (Q1) to enable/disable voltage output to the Vbus.

Chapter 4 The Evaluation Board (EVB) Connections

4.1 EVB PCB Layout

Main Board

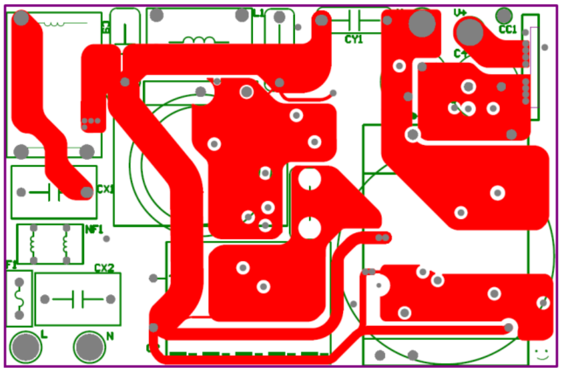


Figure 3. PCB Layout Top View

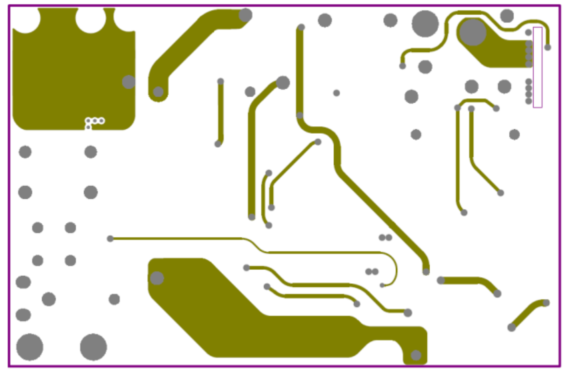


Figure 4. PCB Layout Inner Layer 1

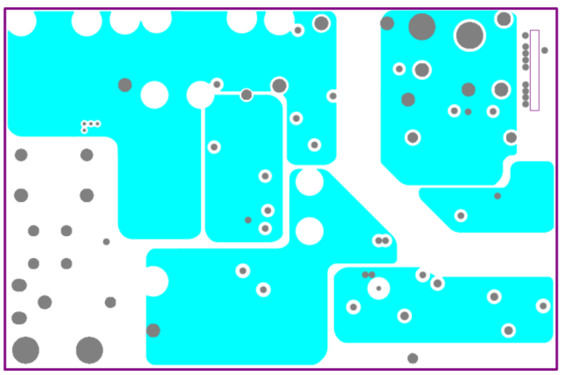


Figure 5. PCB Layout Inner Layer 2

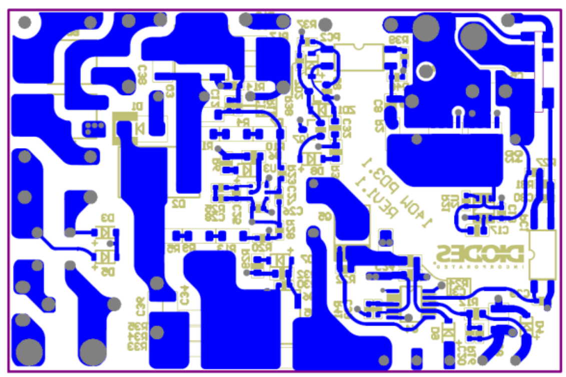


Figure 6. PCB Layout Bottom View

Daughter Board

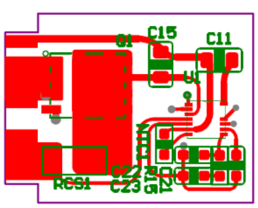


Figure 7. PCB Layout Top View

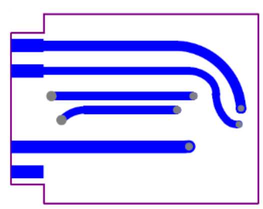


Figure 8. PCB Layout Bottom View

4.2 Quick Start Guide before Connection

1) Before starting the 140W EVB test, the following tools needs to be prepared.

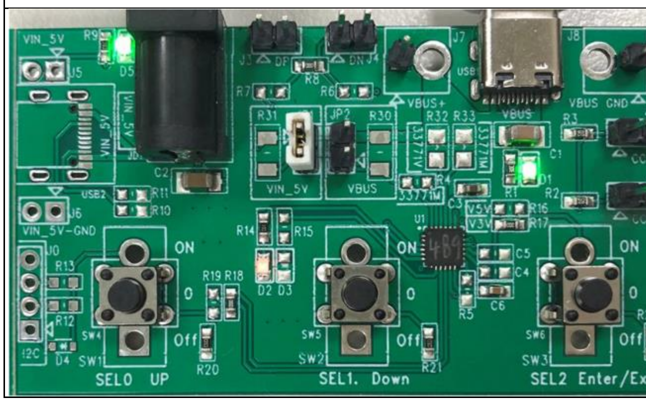
DIODES PD3.1 Tester	Certified USB Type-C Cable
	

Figure 9. DIODES PD3.1Tester / Certified USB Type-C Cable

2) Make sure the AC source is switched OFF before starting the connection steps.

3) Connect the EVB inputs “L” & “N” to the AC source output “L” & “N “.

4) Connect EVB and DIODES PD3.1 tester with a certified USB Type-C cable.

5) Connect the Diodes PD3.1 tester “VBUS+” & “VBUS GND” to E-load.

6) The Diodes PD3.1 tester can be powered by two options:

- Jumper on the left side (VBUS): VBUS-powered.
- Jumper on the right side (DC_IN): External DC 5V powered.

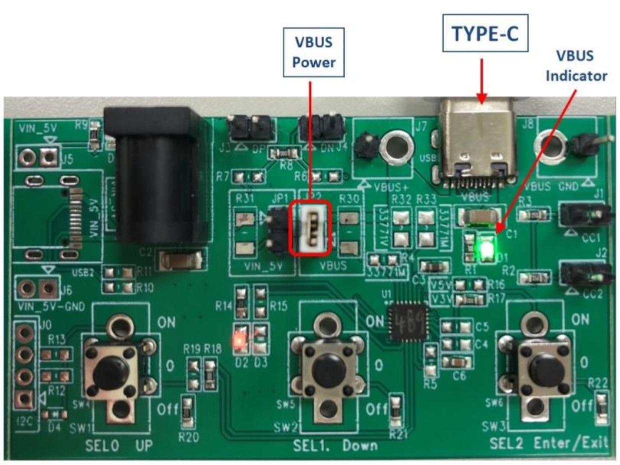


Figure 10. VBUS-powered

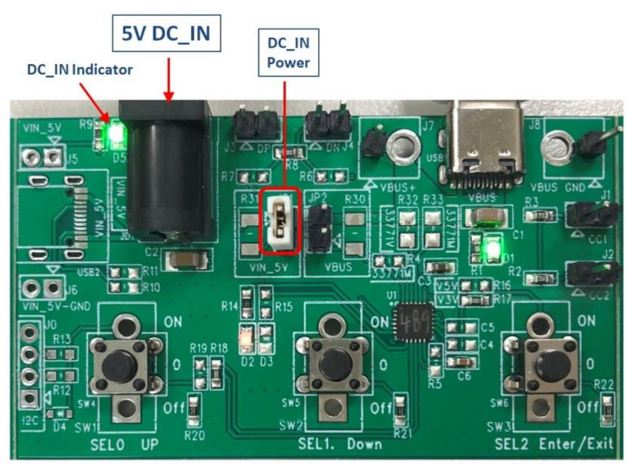


Figure 11. External DC 5V powered

4.3 Connection Diagram

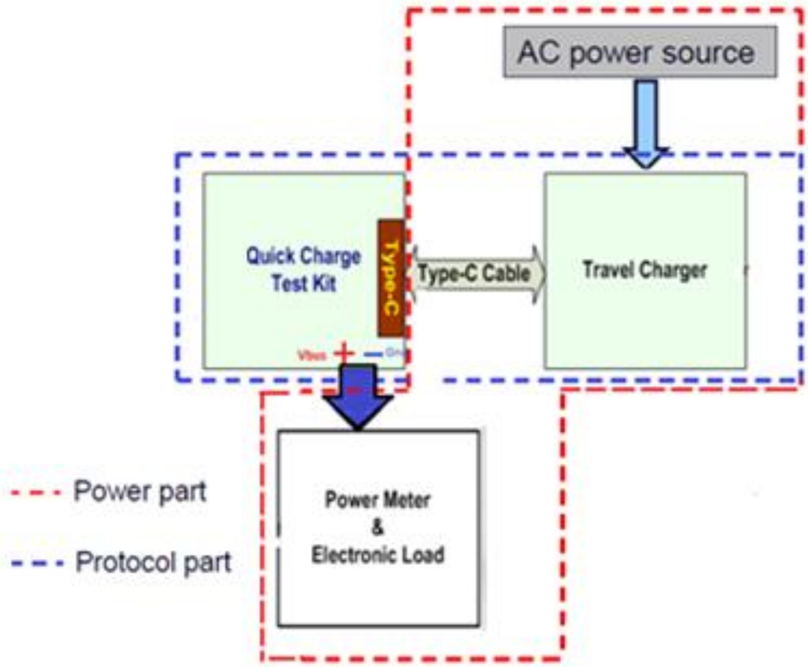


Figure 12. Connection diagram for each device

Chapter 5 Testing the Evaluation Board

5.1 Input & Output Characteristics

5.1.1 Input Standby Power

Vin(V_{AC})	F(Hz)	Pin(mW)
90	60	19.055
115	60	22.942
230	50	50.552
264	50	64.007

5.1.2 Multiple Output Efficiency at Different AC Line Input Voltage

PDO(V)	Iout(A)	Vin(Vac)	F(Hz)	Vout_Board (V)	Pin(W)	Pout(W)	Eff(%)
28	5.00	90	60	28.69	154.19	143.45	93.03%
		115	60	28.66	152.97	143.29	93.67%
		230	50	28.67	151.04	143.37	94.92%
		264	50	28.66	150.93	143.30	94.94%
20	5.00	90	60	20.96	112.43	104.81	93.22%
		115	60	20.95	111.49	104.75	93.95%
		230	50	20.95	110.28	104.74	94.98%
		264	50	20.98	110.4	104.91	95.03%
15	3.00	90	60	15.29	49.68	45.87	92.33%
		115	60	15.47	49.44	46.42	93.89%
		230	50	15.51	49.13	46.52	94.68%
		264	50	15.52	49.21	46.56	94.61%
9	3.00	90	60	9.41	30.57	28.23	92.35%
		115	60	9.41	30.45	28.22	92.68%
		230	50	9.41	30.18	28.22	93.50%
		264	50	9.41	30.19	28.22	93.47%
5	3.00	90	60	5.35	17.84	16.04	89.91%
		115	60	5.34	17.72	16.02	90.44%
		230	50	5.34	17.58	16.03	91.18%
		264	50	5.34	17.60	16.02	91.02%

5.1.3 Efficiency vs. AC Line Input Voltage

Figure 14 illustrates the efficiency vs. input voltage

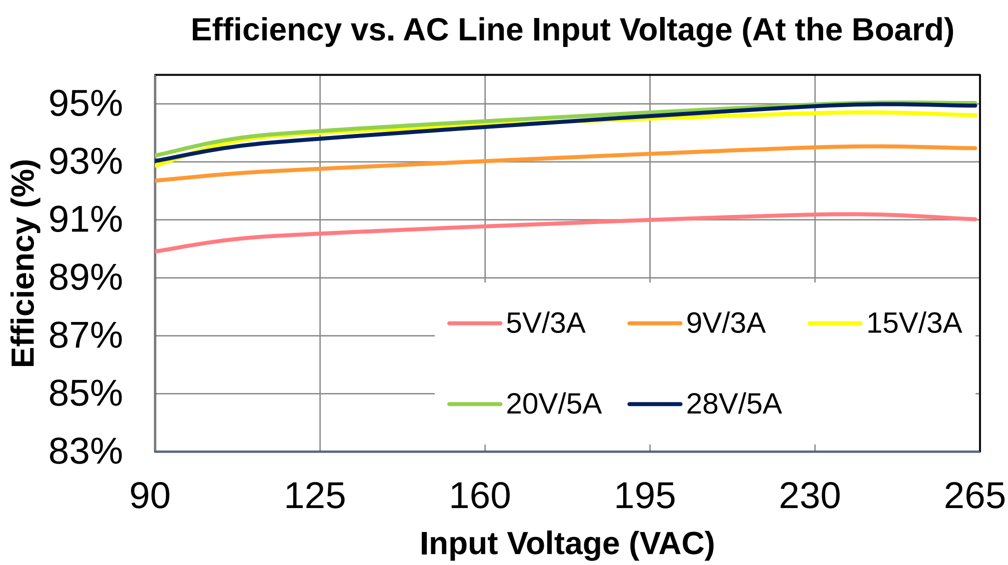


Figure 13. Efficiency vs. Input Voltage – PDO_5V/3A, 9V/3A, 15V/3A 20V/5A, 28V/5A

5.1.4 Total Harmonic Distortion (THD) and Power Factor Correction (PFC)

Figure 15 illustrates the THD vs. Output Power

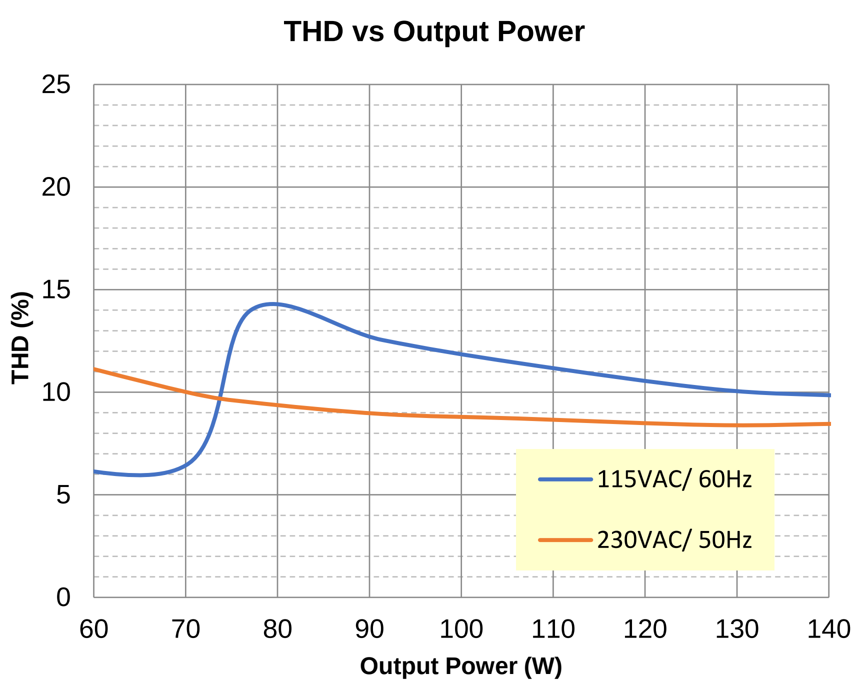


Figure 14. THD vs. Output Power – Full Load 140W PDO_28V/5A

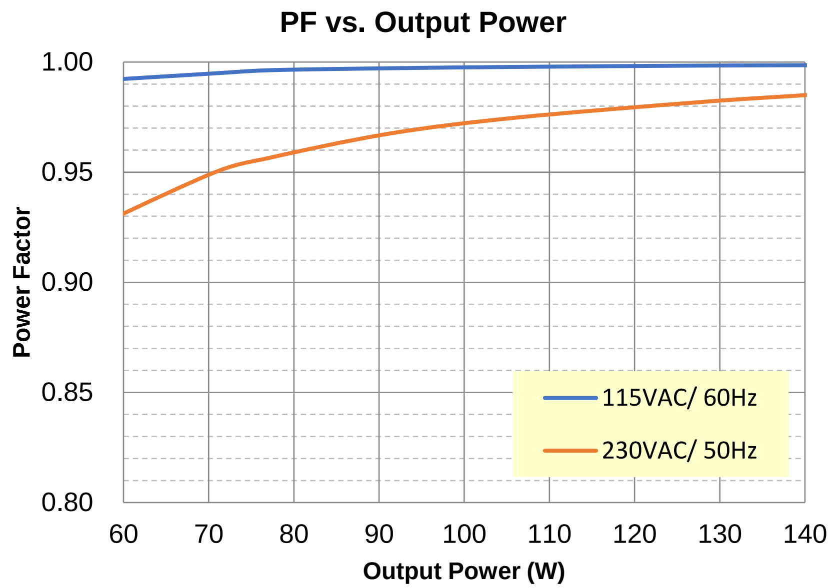


Figure 15. PF vs. Output Power – Full Load 140W PDO_28V/5A

5.1.5 Multiple Output Average Efficiency at Different Loading

Port-C PD3.1_PDO_28V / 20V Average Efficiency

PDO Mode	Vin (Vac)	F(Hz)	Remarks	Iout(A)	Vout(V)	Pin(W)	Pout(W)	Eff(%)	Average Efficiency
28V/5A	115	60	100%	5	28.66	152.97	143.29	93.67%	93.59%
			75%	3.75	28.58	113.65	107.17	94.30%	
			50%	2.5	28.28	75.33	70.70	93.85%	
			25%	1.25	28.12	37.98	35.15	92.55%	
			10%	0.5	27.99	15.40	14.00	90.87%	
	230	50	100%	5	28.67	151.04	143.37	94.92%	94.46%
			75%	3.75	28.55	112.40	107.06	95.25%	
			50%	2.5	28.29	74.63	70.73	94.77%	
			25%	1.25	28.11	37.82	35.14	92.91%	
			10%	0.5	27.99	15.58	14.00	89.86%	
20V/5A	115	60	100%	5	20.95	111.49	104.75	93.95%	93.63%
			75%	3.75	20.89	83.22	78.33	94.13%	
			50%	2.5	20.57	54.94	51.44	93.62%	
			25%	1.25	20.40	27.47	25.50	92.83%	
			10%	0.5	20.32	11.11	10.16	91.46%	
	230	50	100%	5	20.95	110.28	104.74	94.98%	94.28%
			75%	3.75	20.80	82.37	77.99	94.69%	
			50%	2.5	20.61	54.62	51.52	94.33%	
			25%	1.25	20.39	27.38	25.49	93.12%	
			10%	0.5	20.29	11.19	10.14	90.68%	

Port-C PD3.1_PDO_15V / 9V /5V Average Efficiency

PDO Mode	Vin (Vac)	F(Hz)	Remarks	Iout(A)	Vout(V)	Pin(W)	Pout(W)	Eff(%)	Average Efficiency
15V/3A	115	60	100%	3	15.47	49.44	46.42	93.89%	93.64%
			75%	2.25	15.42	36.97	34.68	93.81%	
			50%	1.5	15.30	24.51	22.96	93.65%	
			25%	0.75	15.18	12.22	11.39	93.20%	
			10%	0.3	15.15	5.07	4.54	89.66%	
	230	50	100%	3	15.51	49.13	46.52	94.68%	94.05%
			75%	2.25	15.42	36.70	34.69	94.51%	
			50%	1.5	15.29	24.39	22.94	94.06%	
			25%	0.75	15.20	12.27	11.40	92.94%	
			10%	0.3	15.14	5.05	4.54	89.96%	
9V/3A	115	60	100%	3	9.41	30.45	28.22	92.68%	92.39%
			75%	2.25	9.30	22.59	20.93	92.64%	
			50%	1.5	9.20	14.94	13.80	92.39%	
			25%	0.75	9.11	7.44	6.83	91.84%	
			10%	0.3	9.05	3.04	2.72	89.21%	
	230	50	100%	3	9.41	30.18	28.22	93.50%	92.79%
			75%	2.25	9.32	22.46	20.98	93.40%	
			50%	1.5	9.21	14.89	13.81	92.78%	
			25%	0.75	9.10	7.46	6.83	91.50%	
			10%	0.3	9.04	3.05	2.71	88.89%	
5V/3A	115	60	100%	3	5.34	17.71	16.02	90.44%	89.01%
			75%	2.25	5.25	13.11	11.82	90.15%	
			50%	1.5	5.16	8.72	7.74	88.74%	
			25%	0.75	5.05	4.37	3.79	86.70%	
			10%	0.3	4.99	1.74	1.50	86.02%	
	230	50	100%	3	5.34	17.58	16.03	91.18%	89.84%
			75%	2.25	5.25	13.02	11.82	90.81%	
			50%	1.5	5.16	8.62	7.74	89.78%	
			25%	0.75	5.07	4.33	3.80	87.59%	
			10%	0.3	4.99	1.76	1.50	85.22%	

Efficiency measurement guide

AC port:

AC Input

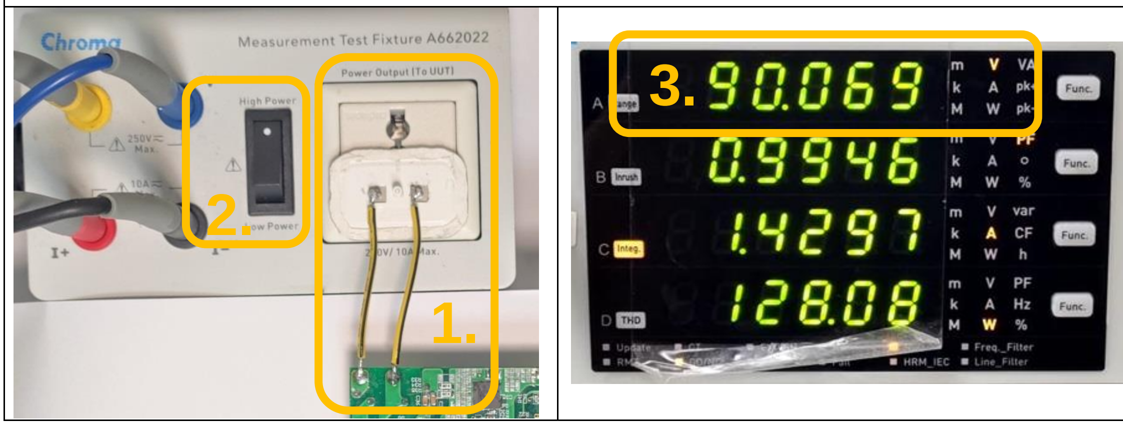


Figure 16. AC input with efficiency measurement

1) AC power core should be as short as possible. (Figure shows as a wall mount application.)
2) Power meter test fixture should switch to "High Power".
3) Make sure AC input level shown on power meter is correct.

DC port:

DC Output

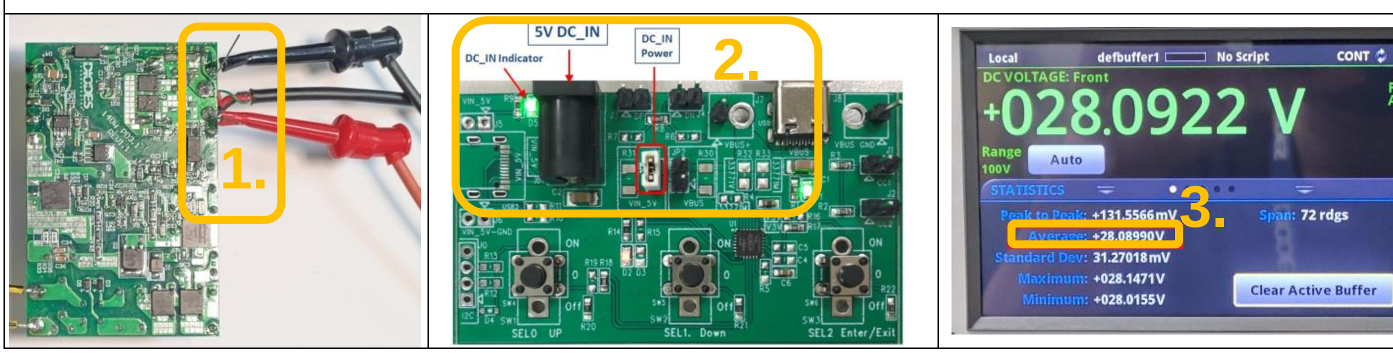


Figure 17. DC output with efficiency measurement

1) Output measured at PCB end.
2) PD tester should supplied by external 5V.
3) Suggest both input/output meter measure with average/integrate function.
4) PSU should at least burn in 20 minutes.

5.1.6 PD3.1 AVS Mode Test

AVS Mode voltage step up/down test with DIODES PD3.1 tester.

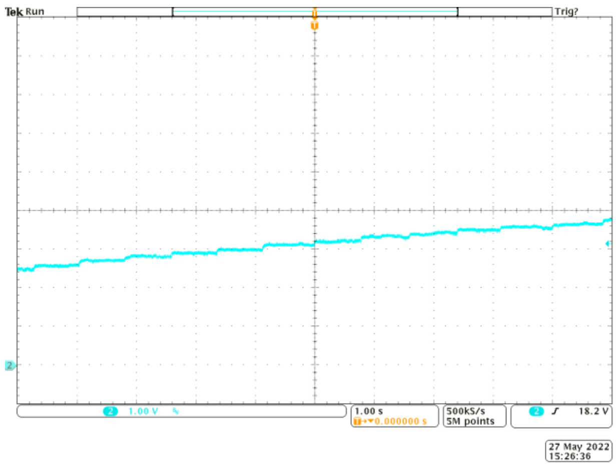


Figure 18. Vout steps up with AVS mode

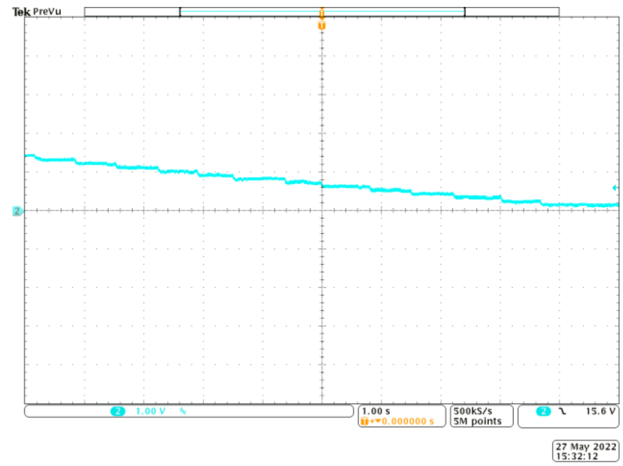


Figure 19. Vout steps down with AVS mode

5.2 Key Performance Waveforms

5.2.1 140W PD3.1 System Start-up Time

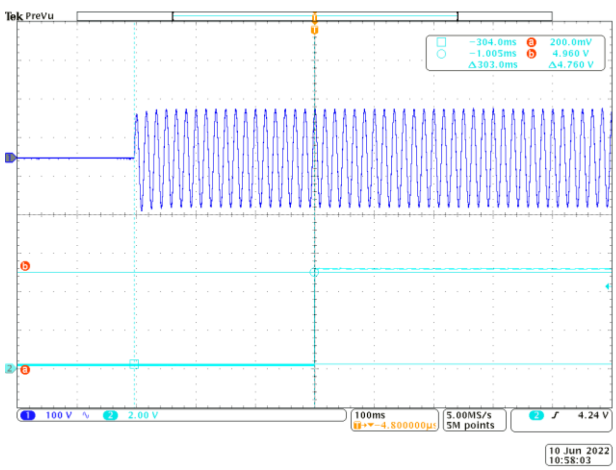


Figure 20. Turn on time is 303ms at Full Load@ 90Vac

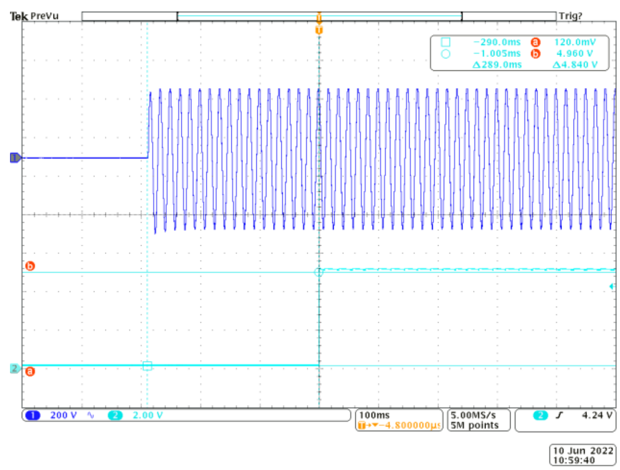
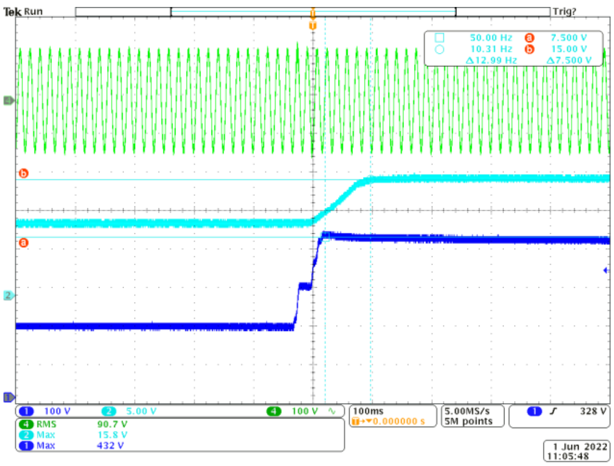


Figure 21. Turn on time is 289ms at Full Load@ 264Vac

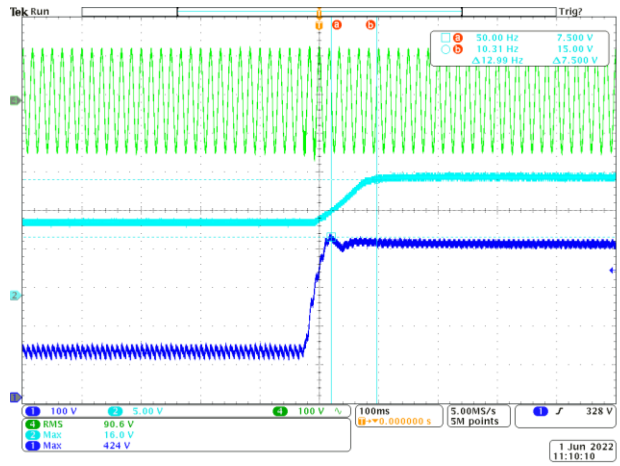
5.2.2 PFC Start-up

The following waveforms show the start-up of PFC when output voltage is set above 15V:



CH1:VBUS(PFC), CH2:Vout, CH4: AC Input

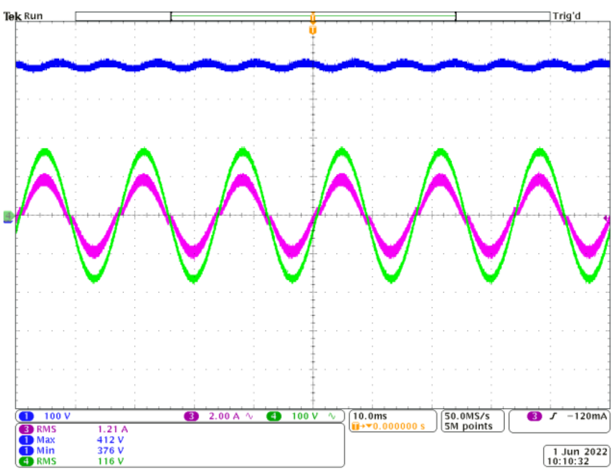
Figure 22. 9V to 15V @90V$_{AC}$/60Hz; Load=0A



CH1:VBUS(PFC), CH2:Vout, CH4: AC Input

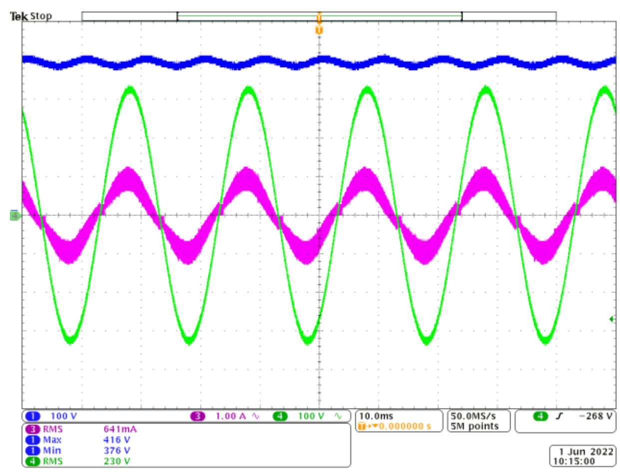
Figure 23. 9V to 15V @90V$_{AC}$/60Hz; Load=3A

5.2.3 Line Voltage and Line Current



CH1:VBUS(PFC), CH3: AC Input Current, CH4:AC Input Voltage

Figure 24. 28V/5A @115V$_{AC}$/60Hz



CH1:VBUS(PFC), CH3: AC Input Current, CH4:AC Input Voltage

Figure 25. 28V/5A @230V$_{AC}$/50Hz

5.2.4 Switching Transistor Voltage Stress

5.2.4.1 PFC Q3 GaN Vds Voltage stress

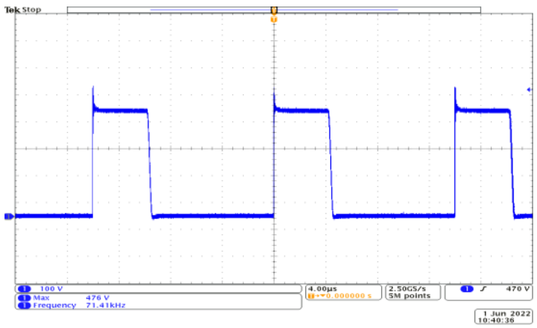


Figure 26. 28V/5A @90V$_{AC}$/60Hz

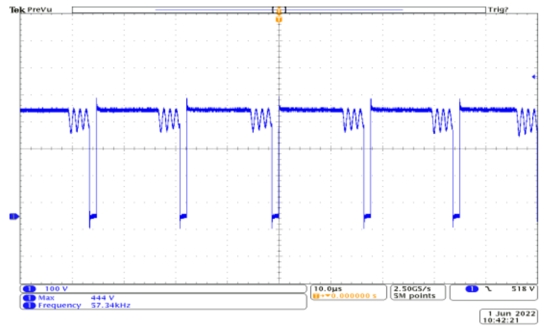


Figure 27. 28V/5A @264V$_{AC}$/50Hz

Component	Input Voltage	Output	Vds	Vds_Max_Spec	Ratio of voltage stress
Q3	90 V$_{AC}$ /60Hz	28V/5A	476V	650V	73.23%
	264 V$_{AC}$ /50Hz		444V		68.31%

5.2.4.2 ACF Primary side MOSFET Q6 & Q5 and Secondary side SR MOSFET Q2

Input: 264Vac/60Hz **Output: 28V/5A**

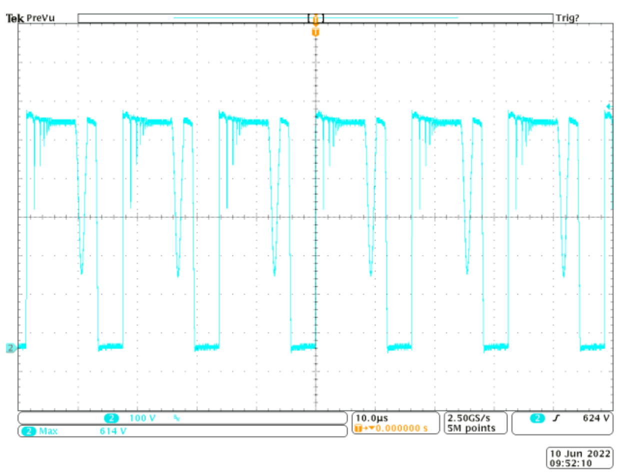


Figure 28. Q6 Vds Voltage stress

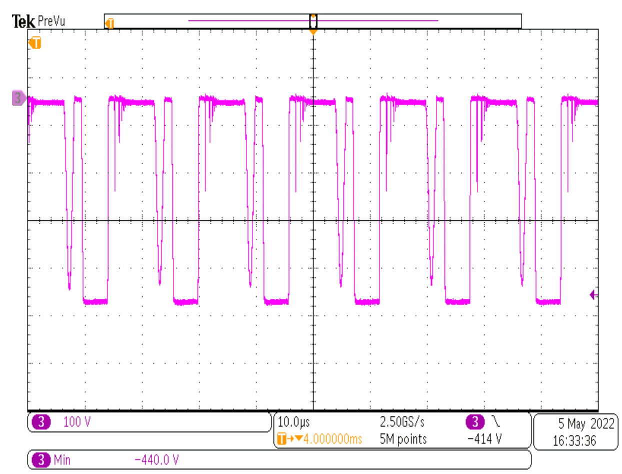


Figure 29. Q5 Vds Voltage stress

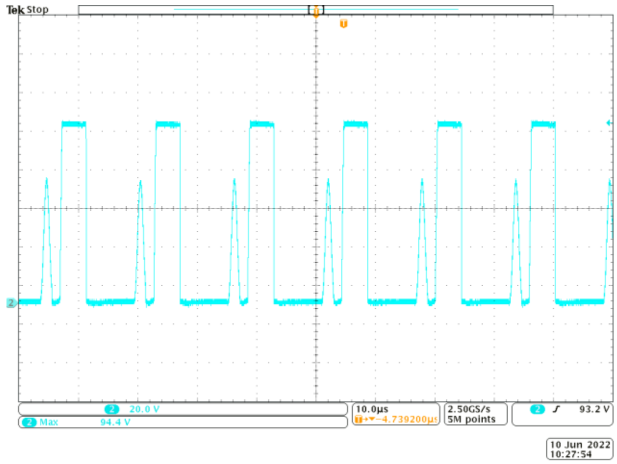


Figure 30. Q2 Vds Voltage stress

Component	Vout	Vds	Vds_Max_Spec	Ratio of voltage stress
Q6	28V	614V	650V	94.46%
Q5		-440.0V	- 650V	67.69%
Q2		94.4V	100V	94.40%

5.2.5 System Output Ripple & Noise with the Cable

Connect 10μF E-Cap and 0.1μF MLCC to the cable end in parallel

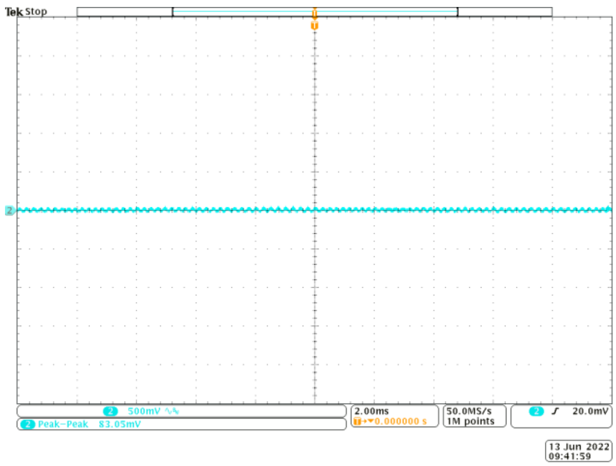


Figure 31. 90Vac/60Hz@ 5V/3A ΔV=83.05mV

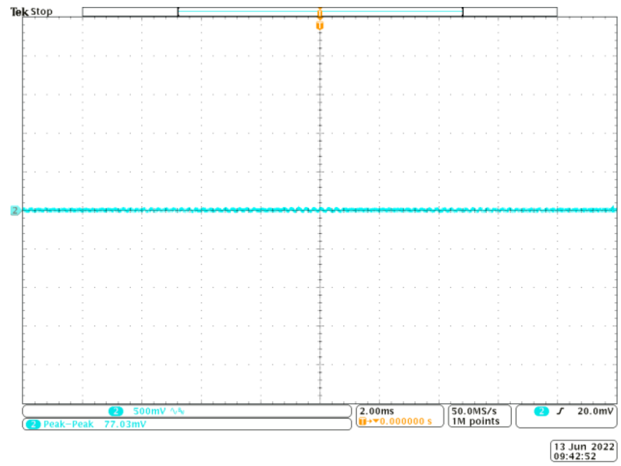


Figure 32. 264Vac/50Hz@5V/3A ΔV=77.03mV

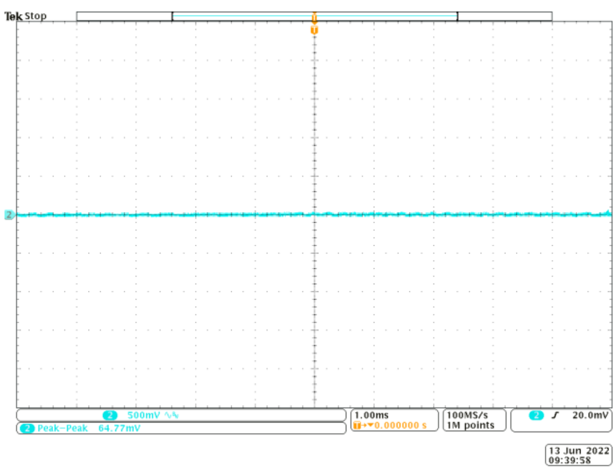


Figure 33. 90Vac/60Hz@9V/3A ΔV=64.77mV

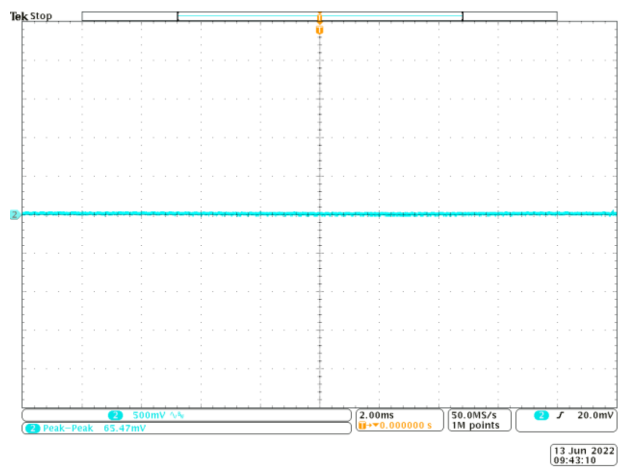


Figure 34. 264Vac/50Hz@9V/3A ΔV=65.47mV

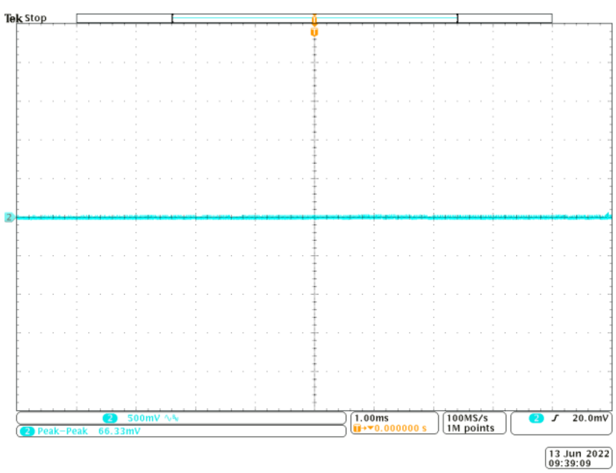


Figure 35. 90Vac/60Hz@15V/3A ΔV=66.33mV

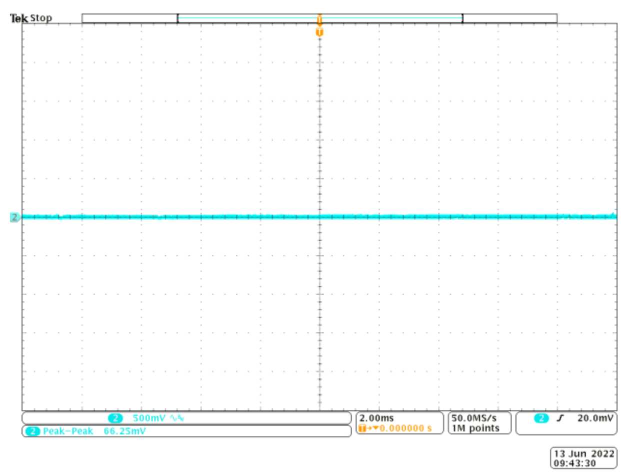


Figure 36. 264Vac/50Hz@15V/3A ΔV=66.25mV

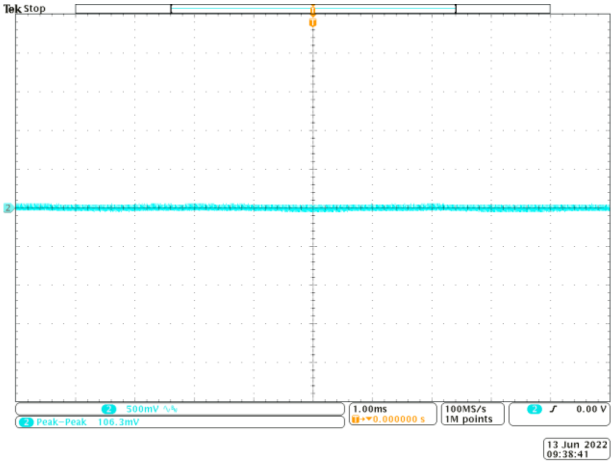


Figure 37. 90Vac/60Hz@20V/5A ΔV=106.3mV

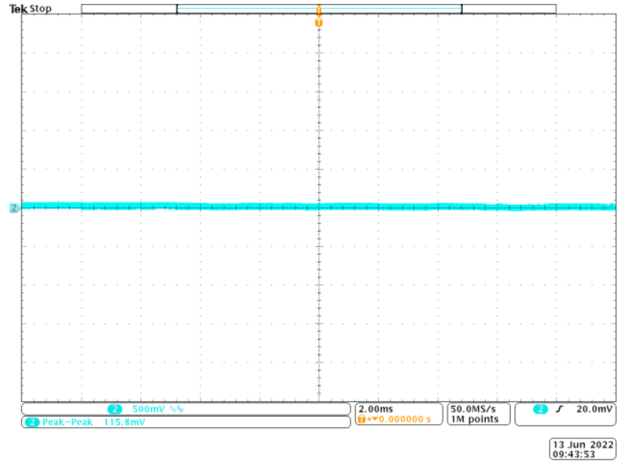


Figure 38. 264Vac/50Hz@20V/3.25A ΔV=115.8mV

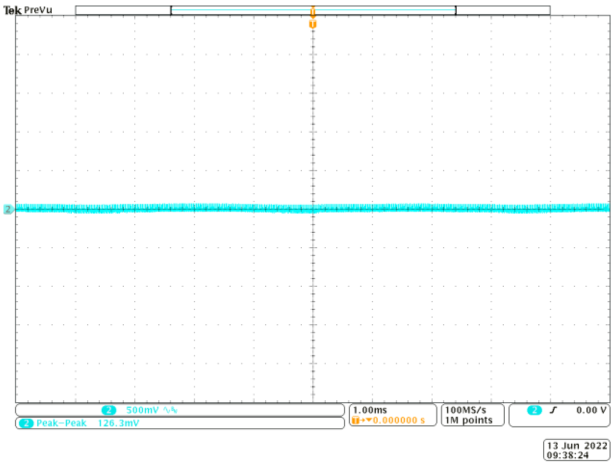


Figure 39. 90Vac/60Hz@28V/5A ΔV=126.3mV

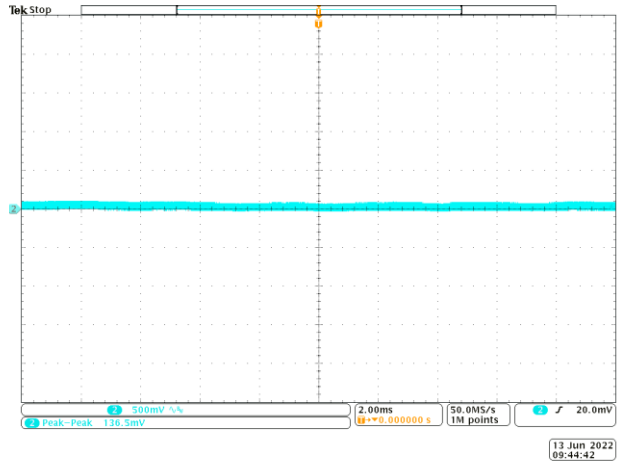


Figure 40. 264Vac/50Hz@28V/5A ΔV=136.5mV

5.2.6 Dynamic load

Load: 0.1A~ 100% Load, T=5mS, Slew Rate=250mA/μs (PCB End)

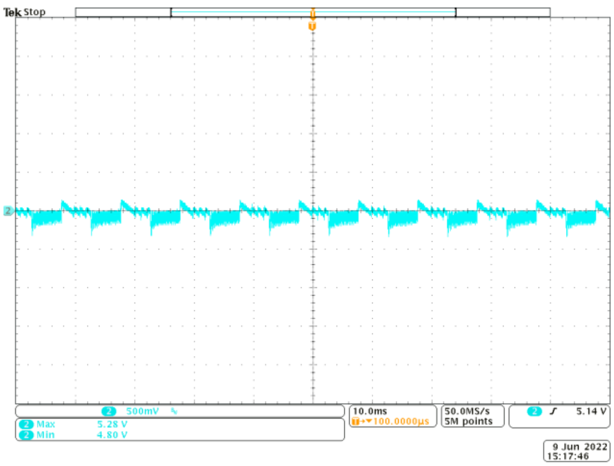


Figure 41. 90Vac/60Hz Port-C@ Vout=5V

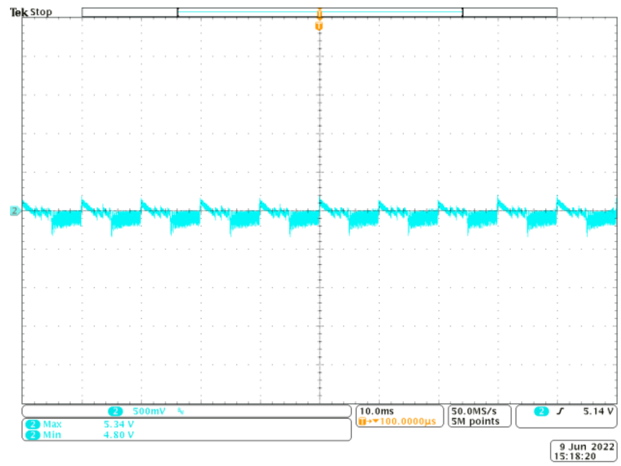


Figure 42. 264Vac/50Hz Port-C@ Vout=5V

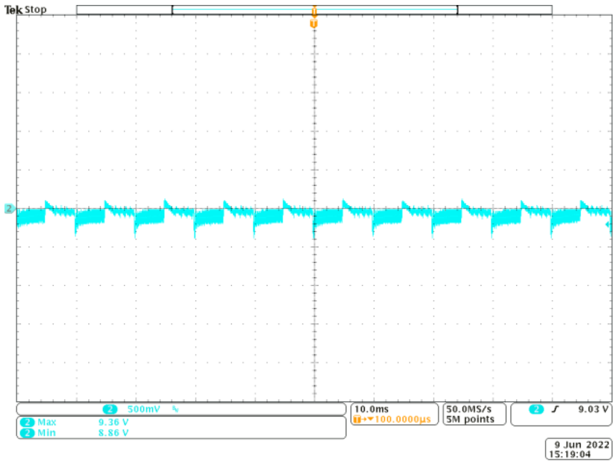


Figure 43: 90Vac/60Hz Port-C@ Vout=9V

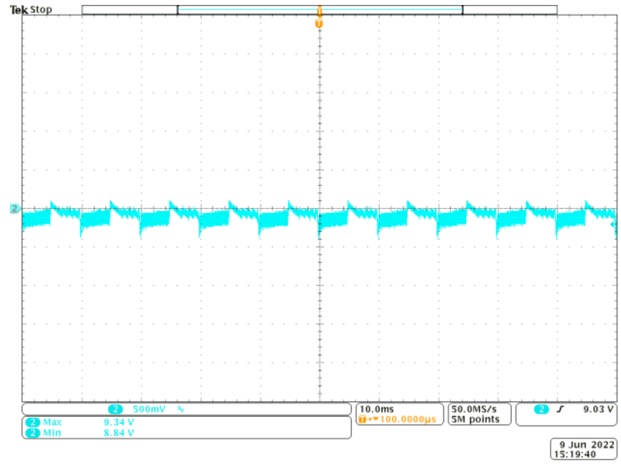


Figure 44: 264Vac/50Hz Port-C@ Vout=9V

	Vo_ Undershoot(V)	Vo_ Overshoot(V)		Vo_Undershoot(V)	Vo_Overshoot(V)
Vin=90Vac@5V	4.80	5.28	Vin=90Vac@9V	8.86	9.36
Vin=264Vac@5V	4.80	5.34	Vin=264Vac@9V	8.84	9.34

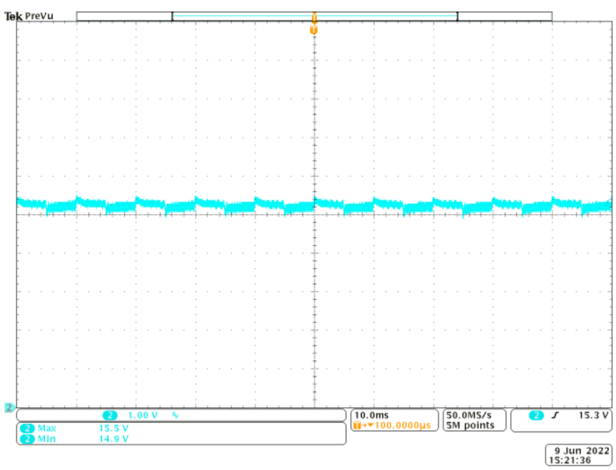


Figure 45. 90Vac/60Hz Port-C@ Vout=15V

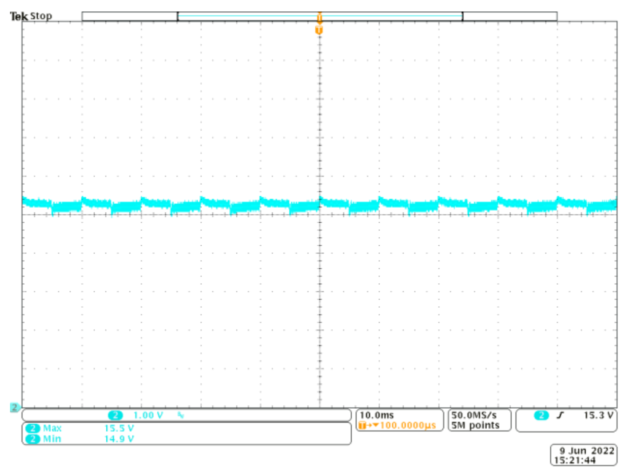


Figure 46. 264Vac/50Hz Port-C@ Vout=15V

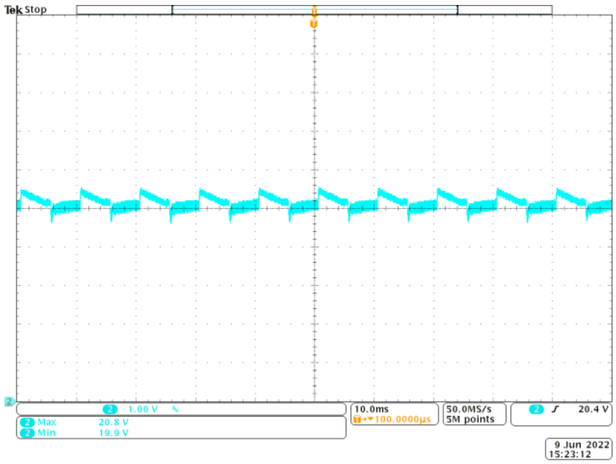


Figure 47. 90Vac/60Hz Port-C@ Vout=20V

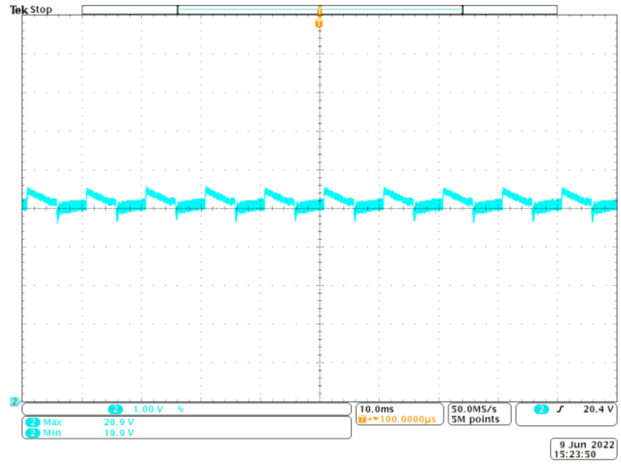


Figure 48. 264Vac/50Hz Port-C@ Vout=20V

	Vo_ Undershoot(V)	Vo_ Overshoot(V)		Vo_Undershoot(V)	Vo_Overshoot(V)
Vin=90Vac@15V	14.9	15.5	Vin=90Vac@20V	19.9	20.8
Vin=264Vac@15V	14.9	15.5	Vin=264Vac@20V	19.9	20.9

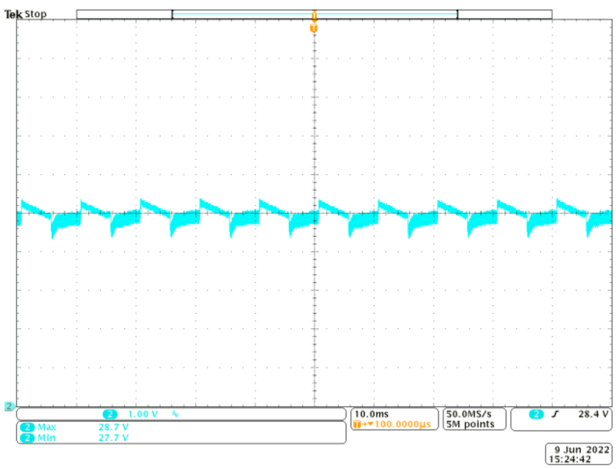


Figure 49. 90Vac/60Hz Port-C@ Vout=28V

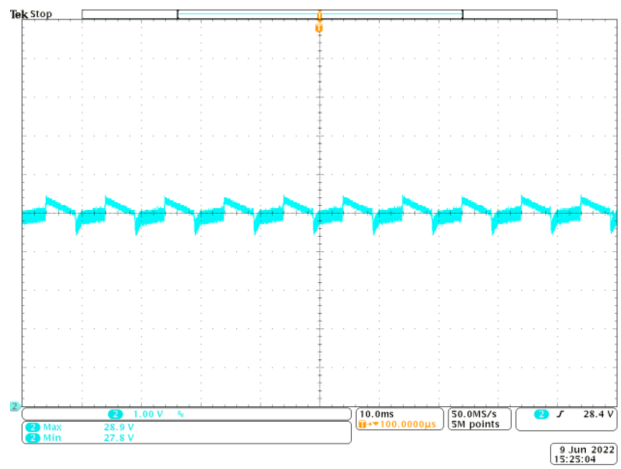


Figure 50. 264Vac/50Hz Port-C@ Vout=28V

	Vo_ Undershoot(V)	Vo_ Overshoot(V)
Vin=90Vac@28V	27.7	28.7
Vin=264Vac@28V	27.8	28.9

5.2.7 Output Voltage Transition Time from Low to High

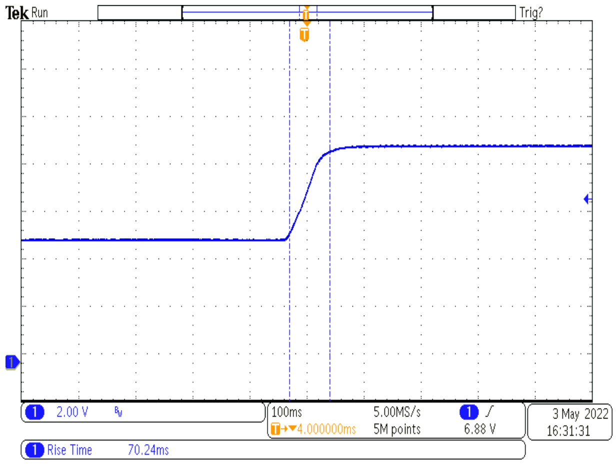


Figure 51. 5V→9V Rise Time = 70.24ms @90Vac

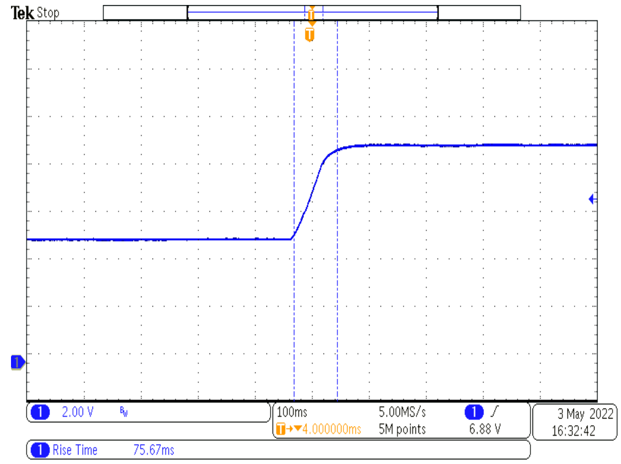


Figure 52. 5V→9V Rise Time = 75.67ms @264Vac

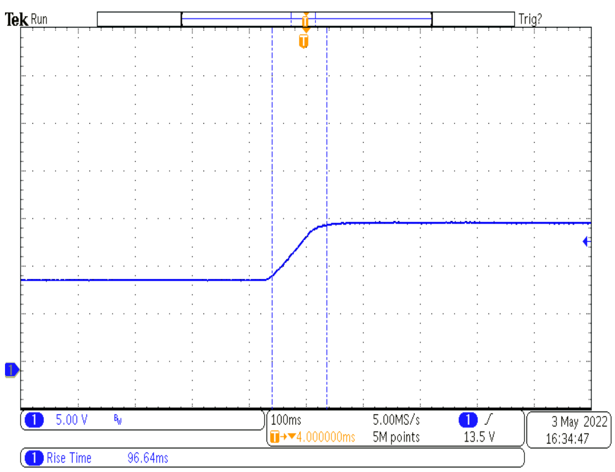


Figure 53. 9V→15V Rise Time = 96.64ms @90Vac

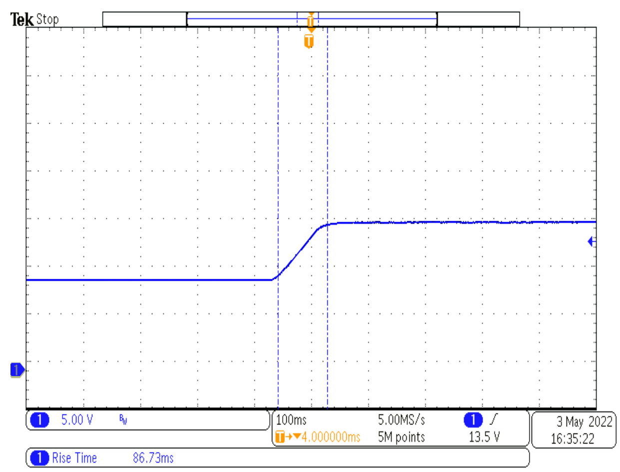


Figure 54. 9V→15V Rise Time = 86.73ms @264Vac

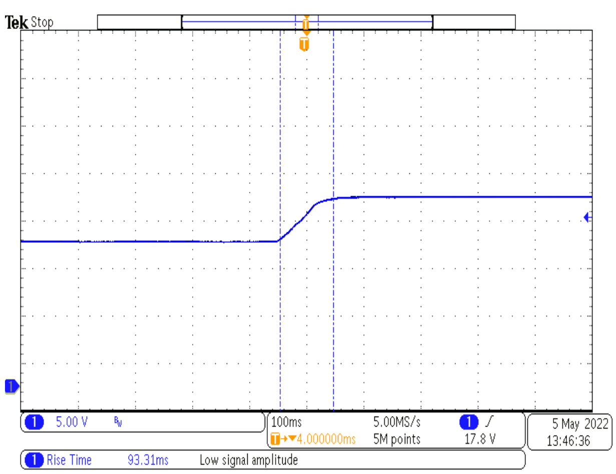


Figure 55. 15V→20V Rise Time = 93.31ms @90Vac

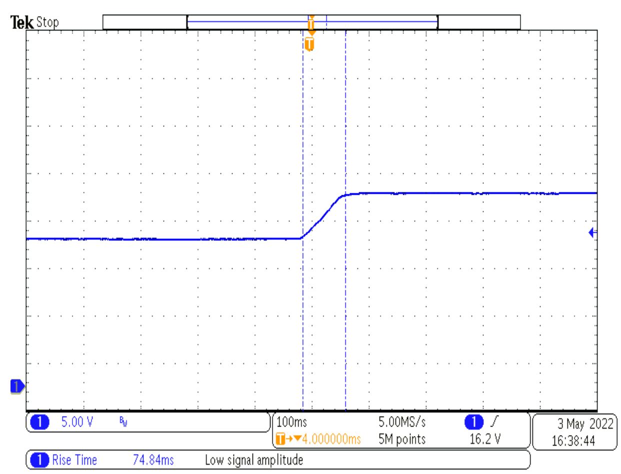


Figure 56. 15V→20V Rise Time = 74.84 ms @264Vac

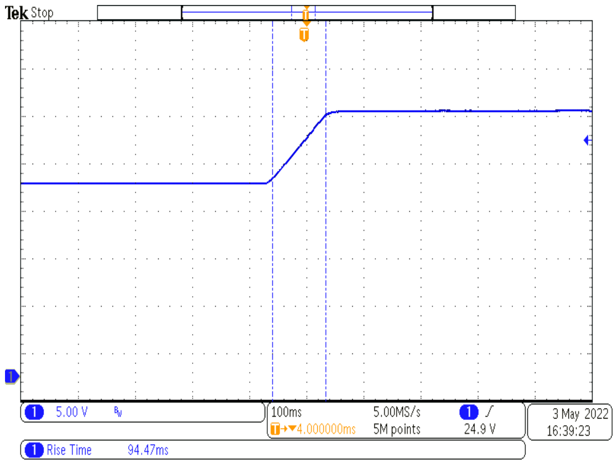


Figure 57. 20V→28V Rise Time = 94.47ms @90Vac

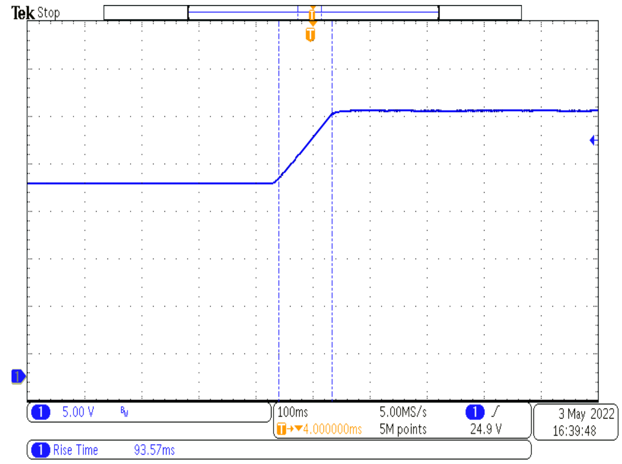


Figure 58. 20V→28V Rise Time = 93.57 ms @264Vac

5.2.8 Output Voltage Transition Time from High to Low

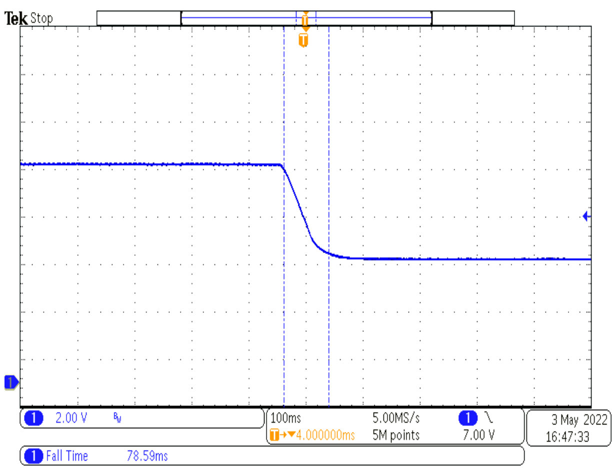


Figure 59. 9V→5V Fall Time = 78.59ms @90Vac

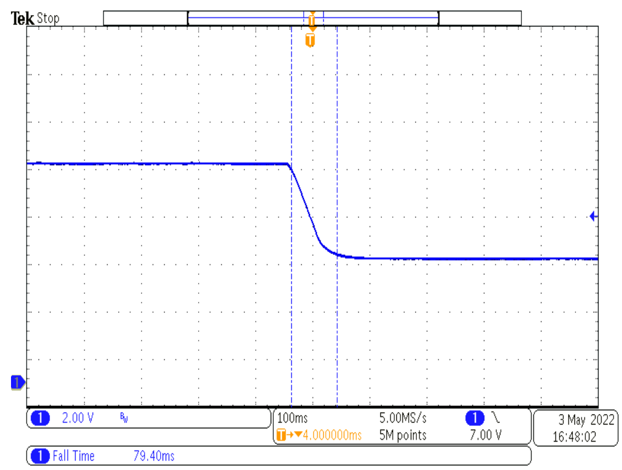


Figure 60. 9V→5V Fall Time = 79.40ms @264Vac

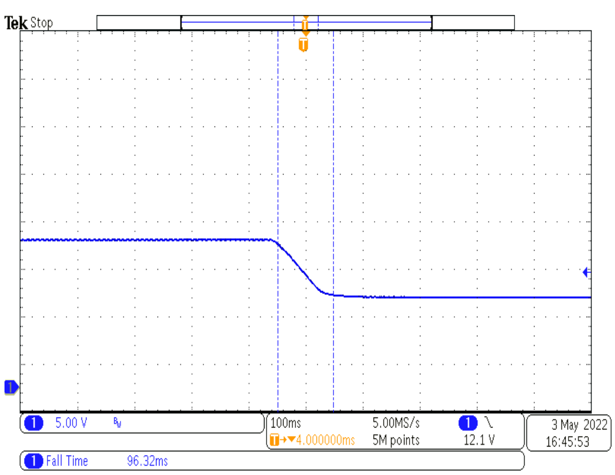


Figure 61. 15V→9V Fall Time = 96.32ms @90Vac

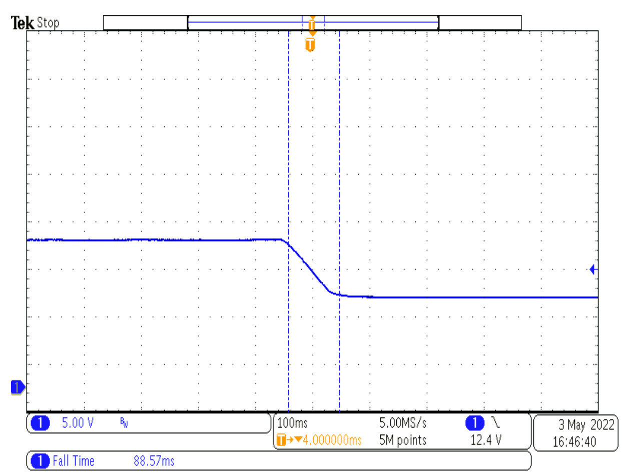


Figure 62. 15V→9V Fall Time = 88.57ms @264Vac

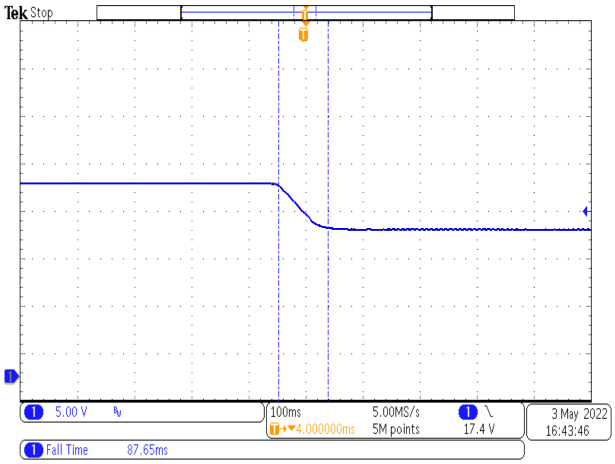


Figure 63. 20V→15V Fall Time = 87.65ms @90Vac

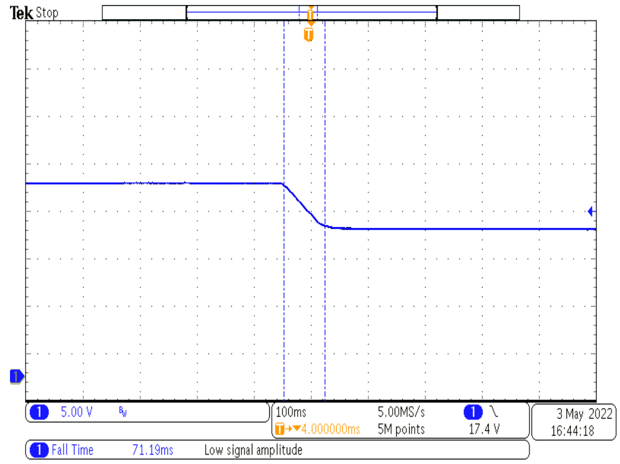


Figure 64. 20V→15V Fall Time = 71.19ms @264Vac

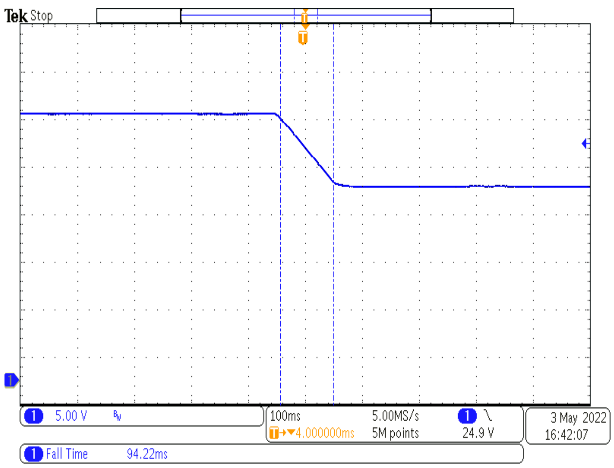


Figure 65. 28V→20V Fall Time = 94.22ms @90Vac

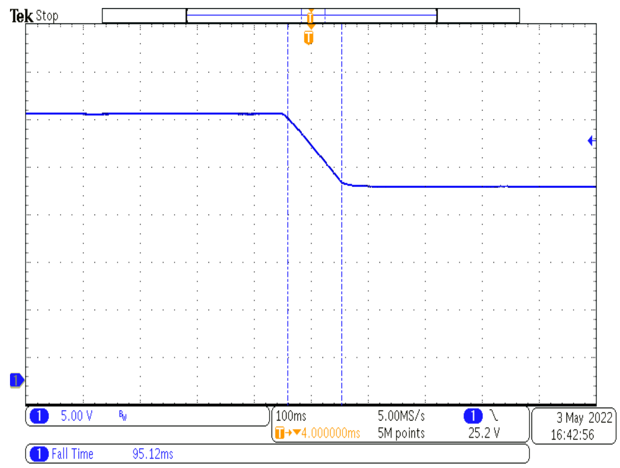


Figure 66. 28V→20V Fall Time = 95.12ms @264Vac

5.2.9 Thermal Testing

Test Condition: Vin=90Vac, Amb=25°C, Open Frame with Full Load 28V/5A

Main Voltage	Temperature (°C)												
	BD1	**BD2**	Q3	D2	Q5	Q6	Q2	Q4	U4	U2	NF2	L2	T1
90Vac/60Hz	103.2	102.1	93.5	88.3	79.2	74.7	72.3	72.0	74.2	81.5	72.2	96.3	80.3

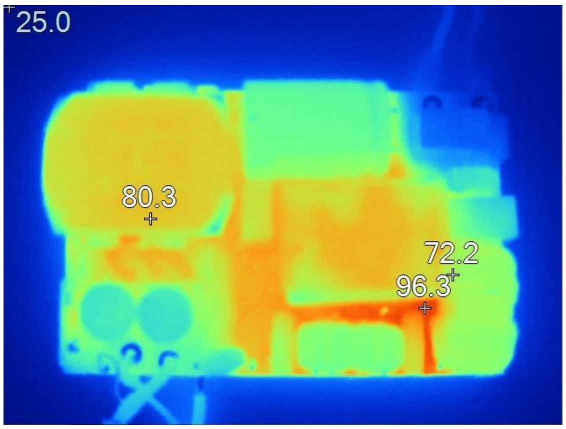


Figure 67. Top Components side

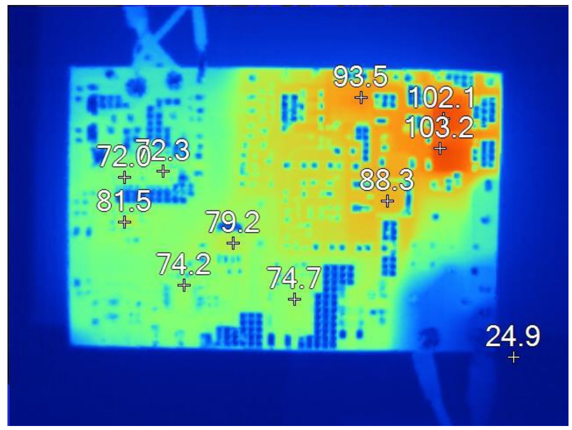


Figure 68. Bottom Suface Mount side

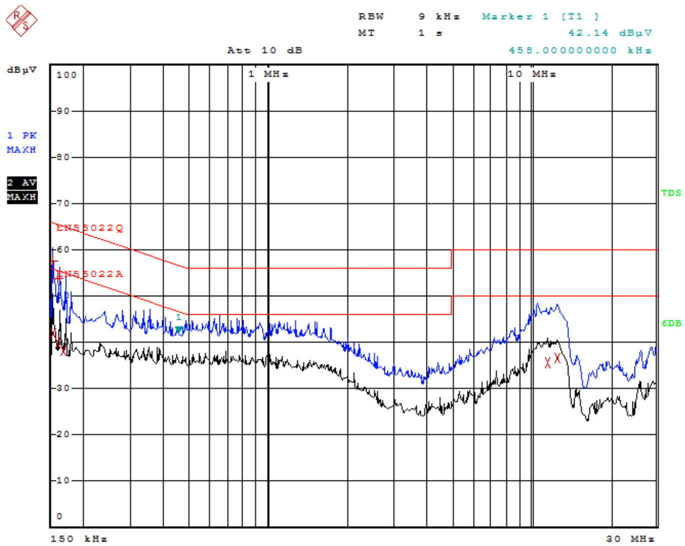
BD1 & BD1: Bridge Rectifier
Q6 : Primary Side High Voltage N-MOS
Q5 : Primary Side High Voltage P-MOS
Q2 & Q4 : Secondary Side Sync-Rectifier
Q3 : PFC N-MOS
D2 : PFC Diode
U4 : AP3306H, ACF Controller
U2 : APR3401, Sync-Rectifier Controller
NF2 : Line filter
L2 : PFC Choke
T1 : Main Transformer

Note: Component temperature can be further optimized with various system design and thermal management approaches by manufacturers.

5.3 EMI (Conduction) Testing

5.3.1 115VAC testing results

Output Condition : 20V/6.5A

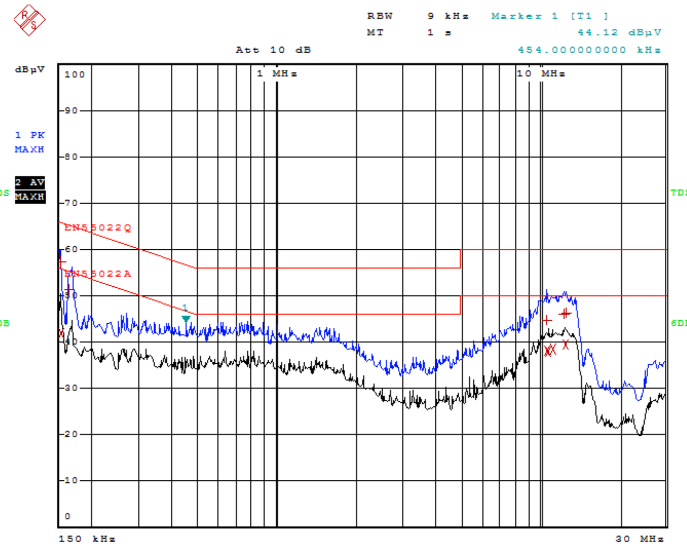


EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
1	Quasi Peak	154 kHz	57.57	-8.20
2	Average	154 kHz	41.97	-13.80
1	Quasi Peak	162 kHz	53.68	-11.68
2	Average	162 kHz	39.89	-15.47
2	Average	170 kHz	38.22	-16.74
2	Average	11.61 MHz	35.60	-14.39
2	Average	12.546 MHz	36.53	-13.46

Figure 69. 115VAC/60Hz L line



EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

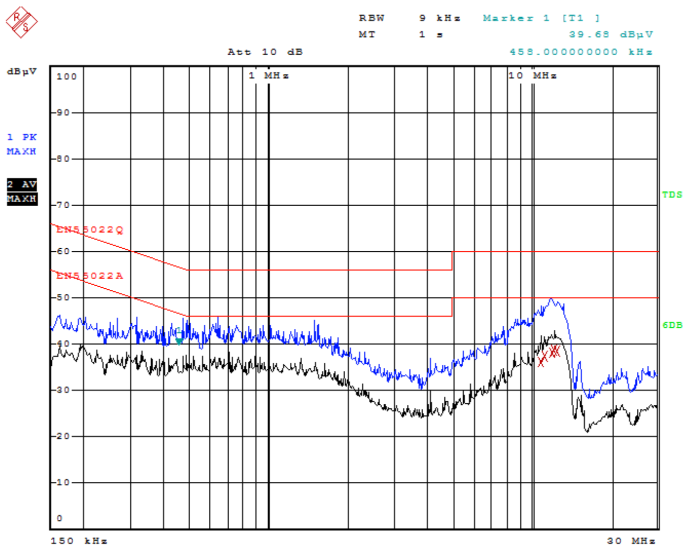
TRACE		FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
1	Quasi Peak	154 kHz	57.36	-8.41
2	Average	154 kHz	41.91	-13.86
1	Quasi Peak	166 kHz	51.38	-13.77
2	Average	10.598 MHz	38.06	-11.93
1	Quasi Peak	10.658 MHz	44.76	-15.24
2	Average	10.702 MHz	37.90	-12.09
2	Average	11.242 MHz	38.53	-11.46
1	Quasi Peak	12.25 MHz	46.13	-13.86
2	Average	12.474 MHz	39.43	-10.56
1	Quasi Peak	12.554 MHz	46.30	-13.69

Figure 70. 115VAC/60Hz N line

5.3.2 230VAC testing results

Output Condition : 20V/6.5A

Output Condition : 28V/5A

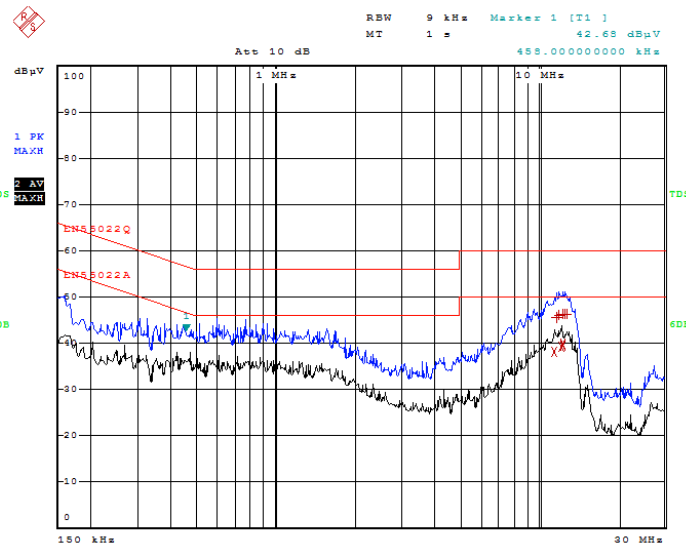


EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
2	Average	10.798 MHz	36.18	-13.81
2	Average	11.146 MHz	37.28	-12.71
2	Average	11.914 MHz	38.26	-11.73
2	Average	12.146 MHz	38.62	-11.38
2	Average	12.502 MHz	38.39	-11.60

Figure 71. 230Vac/50Hz L line



EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
2	Average	11.41 MHz	38.17	-11.82
2	Average	11.446 MHz	38.22	-11.77
1	Quasi Peak	11.642 MHz	45.64	-14.35
1	Quasi Peak	11.99 MHz	46.16	-13.83
2	Average	12.162 MHz	39.36	-10.63
2	Average	12.246 MHz	39.59	-10.40
1	Quasi Peak	12.322 MHz	46.33	-13.66
2	Average	12.322 MHz	39.64	-10.35
1	Quasi Peak	12.606 MHz	46.21	-13.78
1	Quasi Peak	12.67 MHz	46.22	-13.77

Figure 72. 230Vac/50Hz N line