PI3VDP411LS(T)
OC and EQ Settings on Notebook Application

by Ada Yip

PI3VDP411LS(T) on Notebook

The popularity of DisplayPorts (DP) in PC and notebook applications is rising. On current notebook applications, Pericom's PI3VDP411LS(T) can be used to perform digital video level shifting for dual mode DP signals from AC coupled digital video input to DVI or HDMI output. This application brief will examine the appropriate output swing, pre-/de-emphasis settings, and equalization setting.

PI3VDP411LS(T) Block Diagram

50Ω termination resistors are integrated at TMDS inputs for AC-coupled digital video inputs.

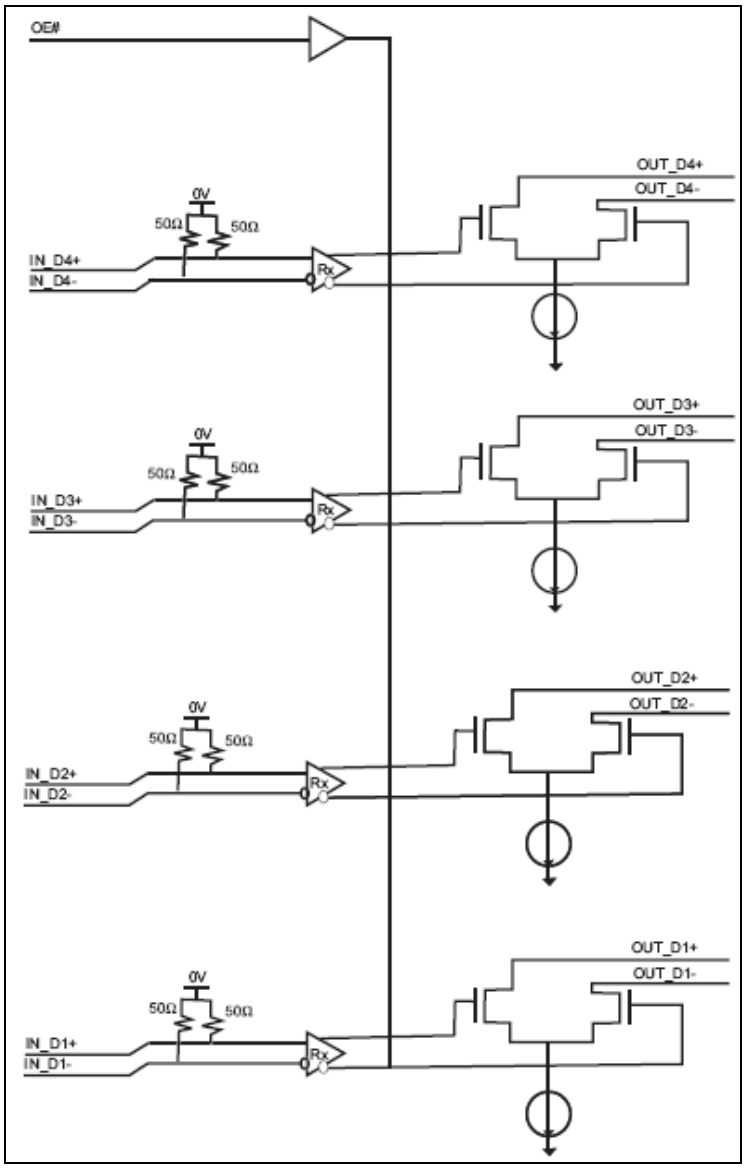

Figure 1: Termination Resistor Scheme

PI3VDP411LS(T) Control Pins

There is no internal pull-up or pull-down resistor on the OE# pin, which is shown in figure 1. Also, no such resistor is implemented in DDC_EN pin, or SCL/SDA pins as shown in figure 2 below.

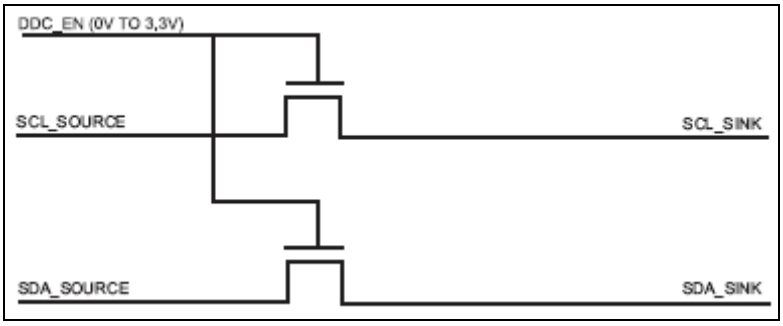

Figure 2: Enable & DDC Pin Scheme

On the contrary, 100kΩ internal pull-up resistors are integrated in OC and EQ pins.

Pin Name	Type	Description
OC_2 (1) (REXT)	3.3V single-ended control input	Acceptable connections to OC_1 (REXT) pin are: Resistor to GND; Resistor to 3.3V; NC. (Resistor should be 0-ohm).
OC_3(1)	Analog connection to external compcnent or supply	Acceptable connections to OC_3 pin are: short to 3.3V or to GND; NC.
OC_0(1) OC_1(1) EQ_0(1) EQ_1(1)	Outpu: and Input jitter elimination control	Control pins are to enable Jitter elimination features. For normal operation these pins are tied GND or to VCC3V. Please see the truth tables for more information.

Note:
1) internal 100Kohm pull-up

Table 1: OC & EQ Pin Definition

Typical OC & EQ Application

Since OC and EQ pins of PI3VDP411LS(T) are designed to have 100kΩ internal pull-up resistors, external pull-down resistors are required on PCB schematics to set some of these pins to Low level. It is recommended that users add pull-down resistor strapping for OC and EQ control pins as shown in figure 3.

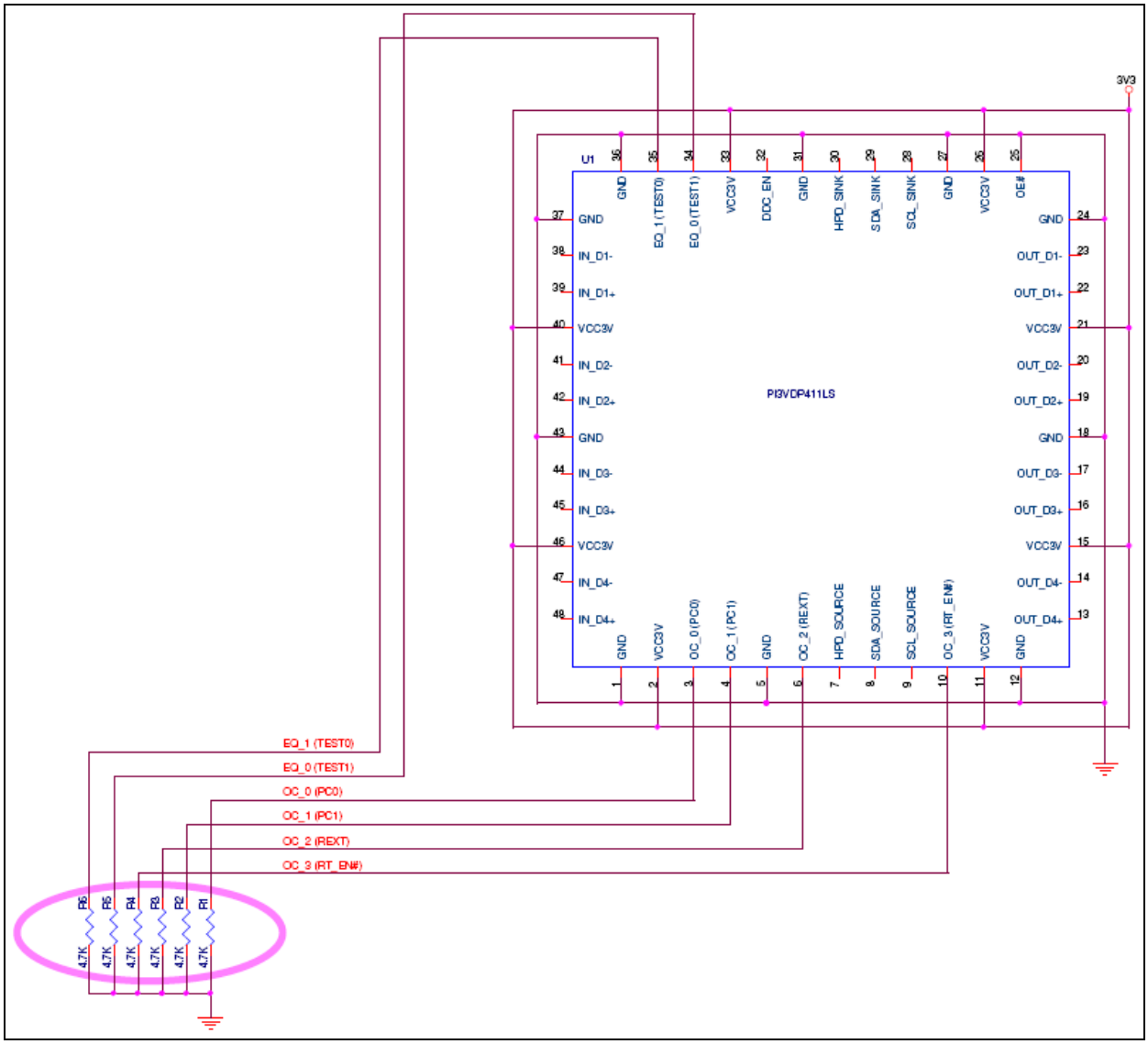

Figure 3: PI3VDP411LS PCB Schematic with Appropriate Pull-down Resistors at Control Pins

PI3VDP411LS(T) Swing and Pre-/De-emphasis Settings

Swing and Pre-/De-emphasis are used for compensating PCB trace or cable loss at output of PI3VDP411LS(T). Swing is the peak-to-peak voltage of a transmitted signal.

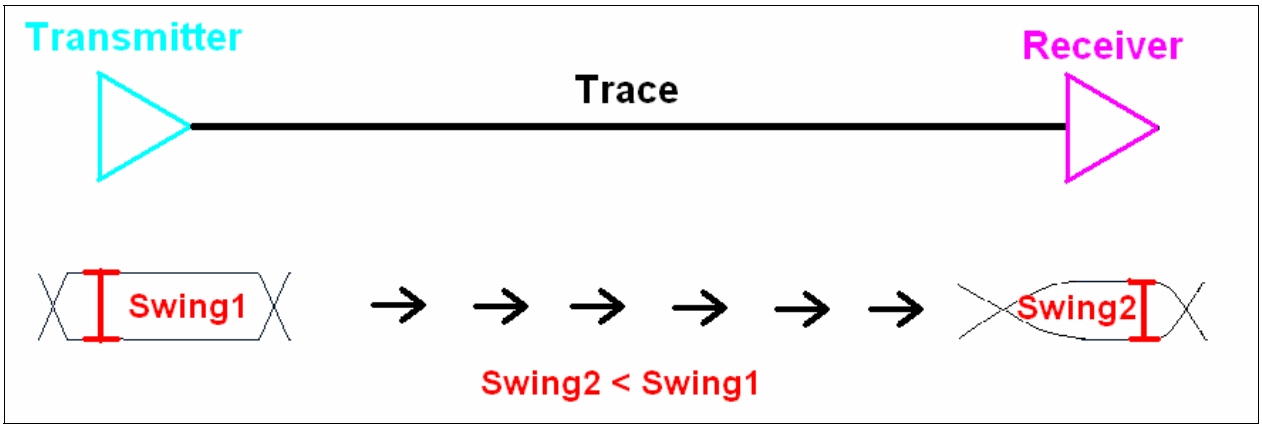

Figure 4: Function of Swing

Pre-emphasis increases initial drive to pre-compensate insertion loss through trace.

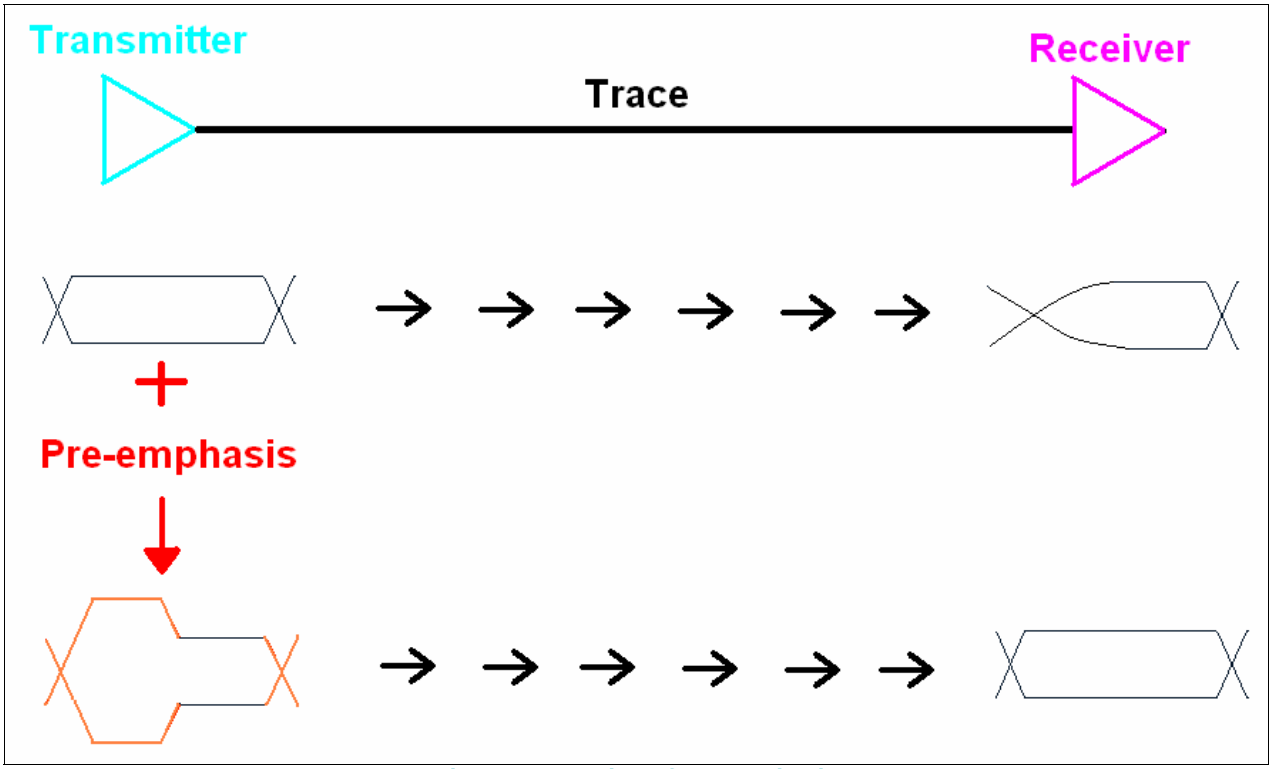

Figure 5: Function of Pre-emphasis

De-emphasis controls the swing of signal to prevent from inter-symbolic interference.

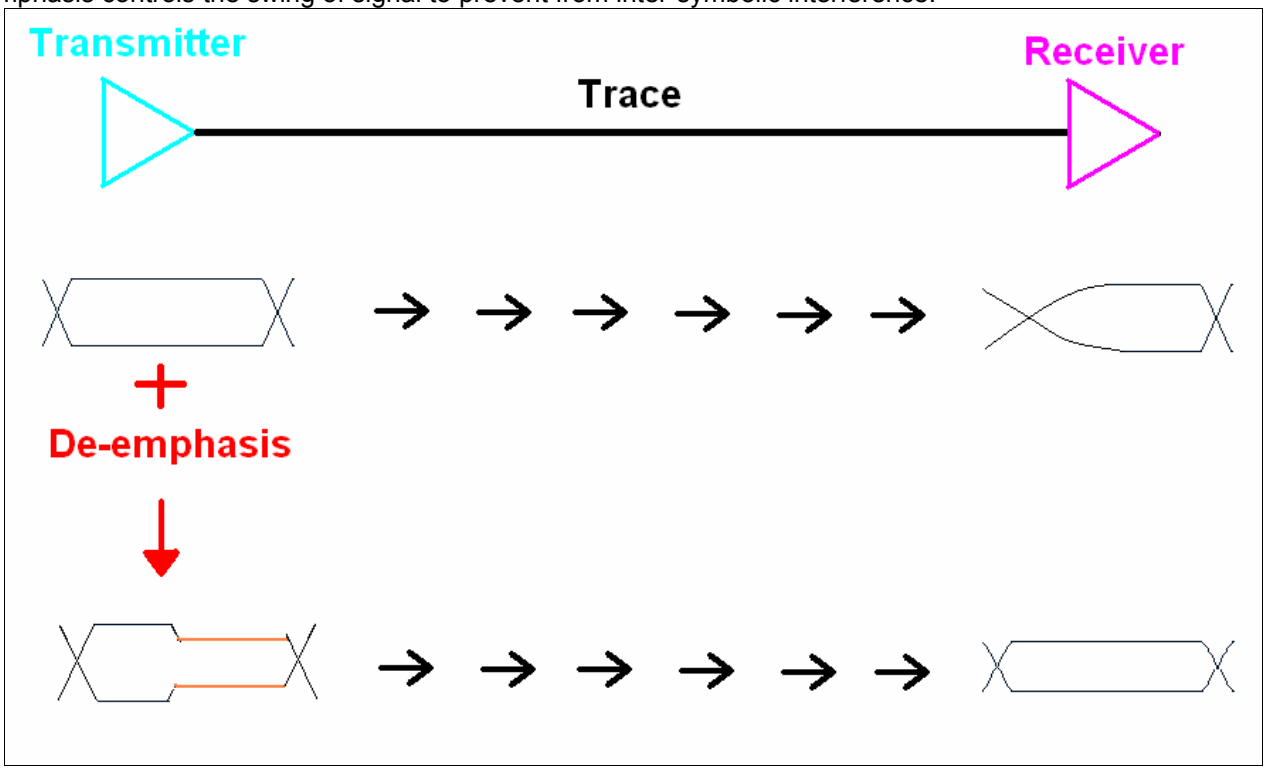

Figure 6: Function of De-emphasis

Four OC pins, OC_[3:0], are used to control TMDS output voltage swing (Vswing) and degree of pre-/de-emphasis. When all OC pins are pulled to High level internally by 100kΩ pull-up resistors, the default Vswing and De-emphasis are 1000mV and -9dB, respectively. To give more flexibility of OC settings on PCB, it is recommended to reserve pads for 4.7kΩ pull-down resistor on each of the four OC pins.

Table 2 below highlights typical OC control pin settings for Notebook application.

OC_3 =RT_EN#	OC_2 =REXT	OC_1 =PC1	OC_0 =PC0	Vswing (mV)	Pre-/De-emphasis (dB)	Application
0	0	0	0	500	0	Short Cable
0	0	0	1	600	0	Long Cable
0	0	1	0	750	0	
0	0	1	1	1000	0	
0	1	0	0	500	0	Short Cable
0	1	0	1	500	1.5	Short Cable
0	1	1	0	500	3.5	Long Cable
0	1	1	1	500	6	
1	0	0	0	400	0	
1	0	0	1	400	3.5	
1	0	1	0	400	6	
1	0	1	1	400	9	
1	1	0	0	1000	0	
1	1	0	1	1000	-3.5	
1	1	1	0	1000	-6	
1	1	1	1	1000	-9	

Table 2: OC Settings

PI3VDP411LS(T) Equalization Settings

Equalization is used to remove deterministic jitter introduced by impedance mismatch along a PCB trace. It also reduces signal swing.

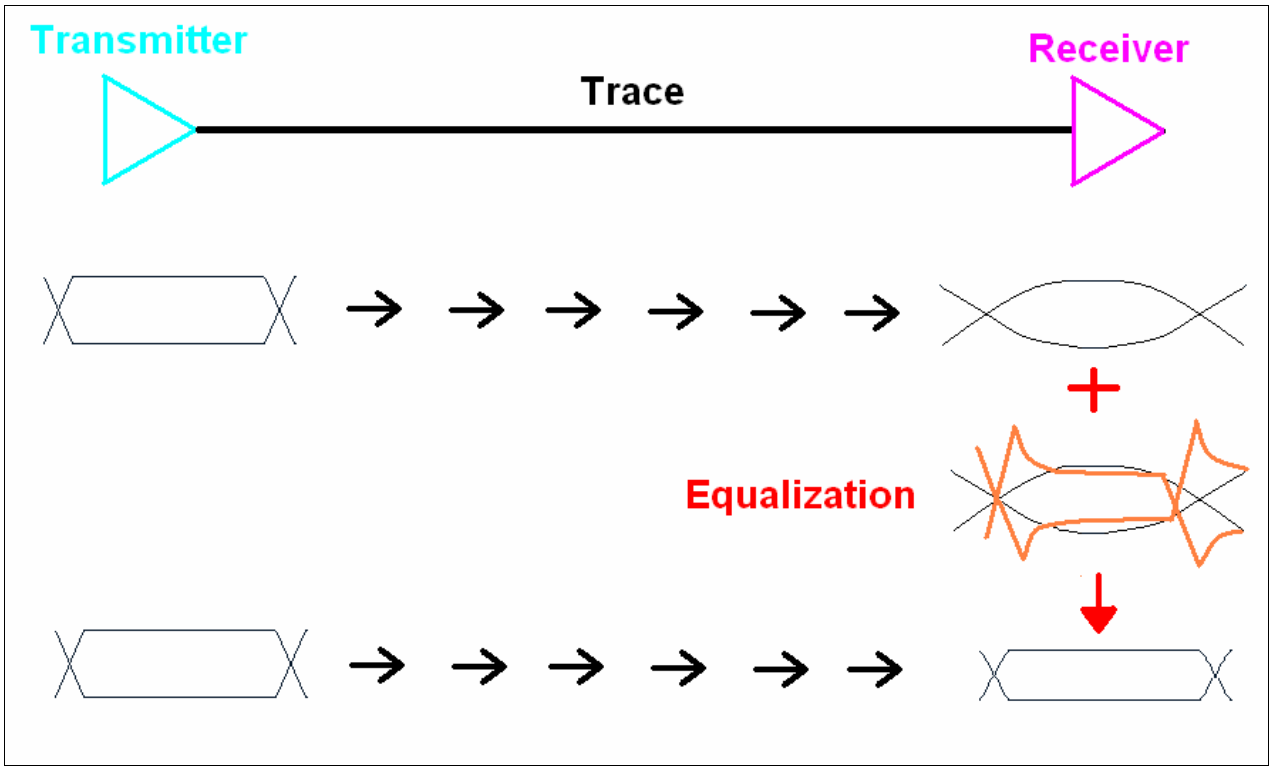

Figure 7: Function of Equalization

Two pins, EQ_[1:0], give us four choices of equalization to optimize performance of different trace lengths to DisplayPort inputs. Since the trace length between the core chip in notebook and PI3VDP411LS(T) DisplayPort input varies for various notebook PCB layout, Table 3 (below) provides a guideline for equalization settings. Like OC pins, EQ pins have internal 100kΩ pull-up resistors. If EQ pins are left floating, the default equalization setting will be 12dB. It is also recommended to reserve pads for 4.7kΩ pull-down resistors at EQ pins on PCB.

EQ_0 =TEST1	EQ_1 =TEST0	Equalization (dB)	Application
0	0	3	Shortest Trace Length
0	1	7.2	Shorter Trace Length
1	0	10	Longer Trace Length
1	1	12	Longest Trace Length

Table 3: EQ Settings

Optimum OC Settings with 25” Output Traces plus Cables

With the use of 1080p HDTV as sink, eye diagrams of different OC settings have been captured. 3dB equalization is employed on the application of 25-inch output traces plus cables. Four settings of OC_[3:0] which includes [0100], [0000], [0101] and [0110], are recommended. Of these settings, [0101] is the optimum setting for short cable application and [0110] may be a better choice for long cable application.

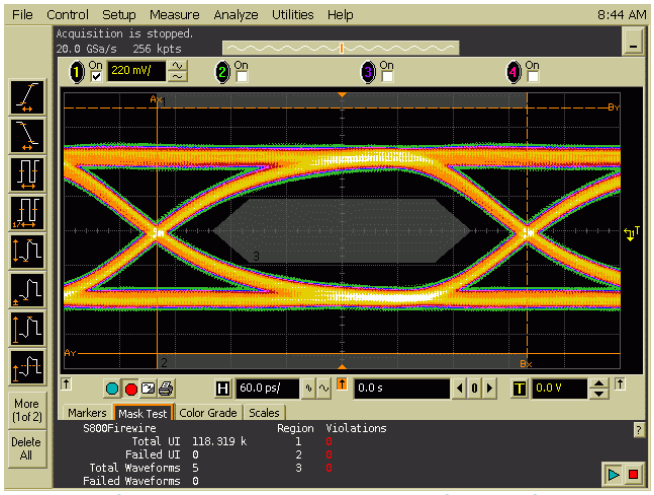

Figure 8a: Tx Eye at 500mVswing & 0dB Pre-emphasis, [0000]

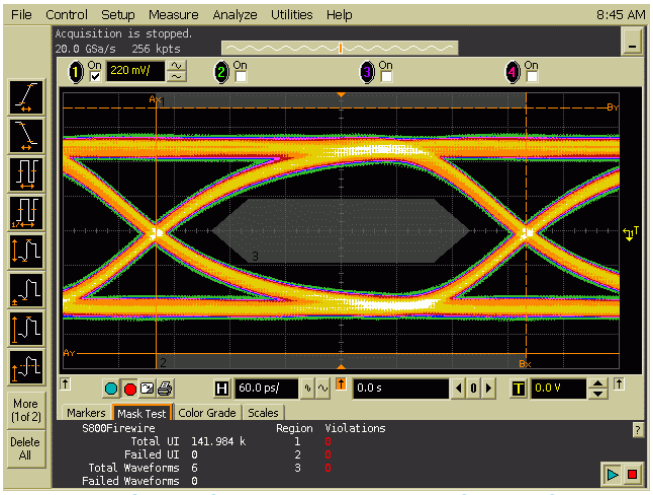

Figure 8b: Tx Eye at 600mVswing & 0dB Pre-emphasis, [0001]

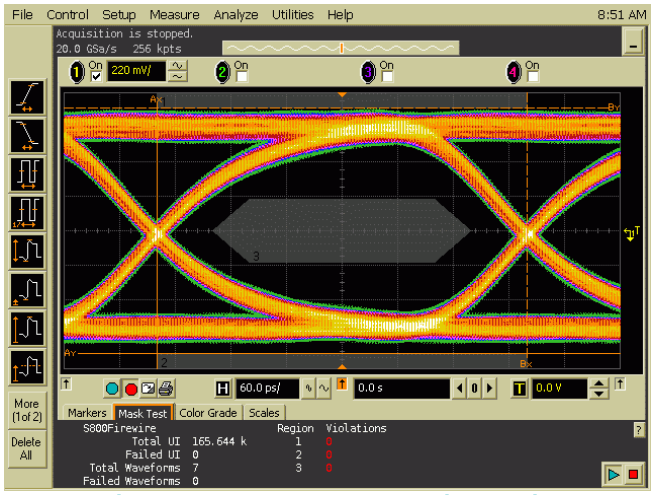

Figure 8c: Tx Eye at 750mVswing & 0dB Pre-emphasis, [0010]

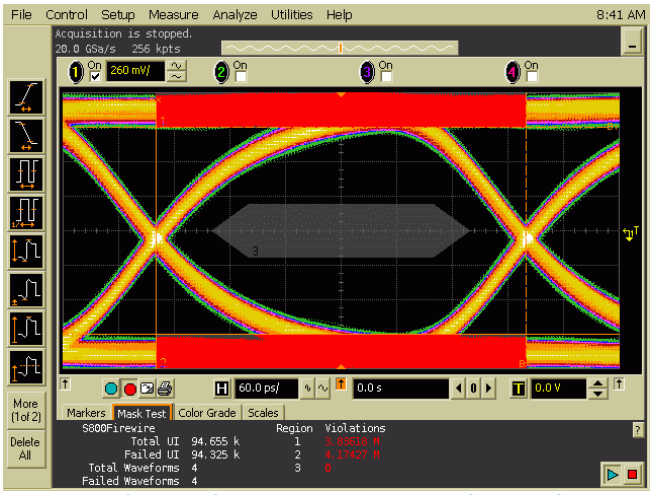

Figure 8d: Tx Eye at 1000mVswing & 0dB Pre-emphasis, [0011]

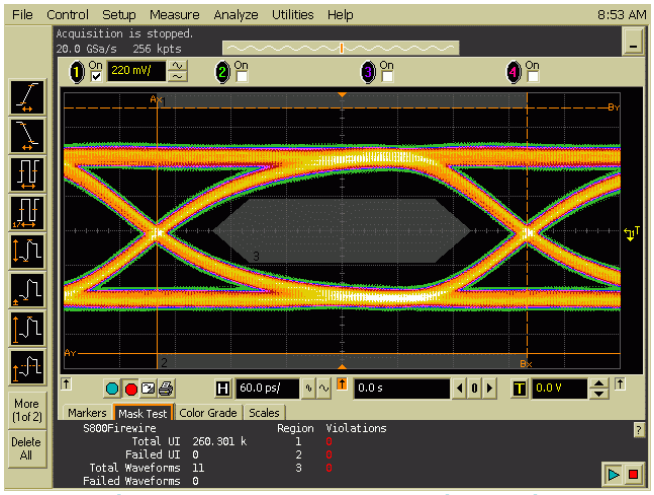

Figure 8e: Tx Eye at 500mVswing & 0dB Pre-emphasis, [0100]

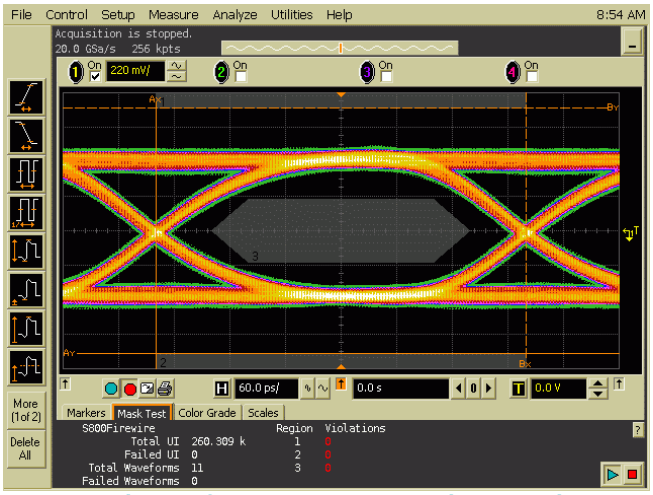

Figure 8f: Tx Eye at 500mVswing & 1.5dB Pre-emphasis, [0101]

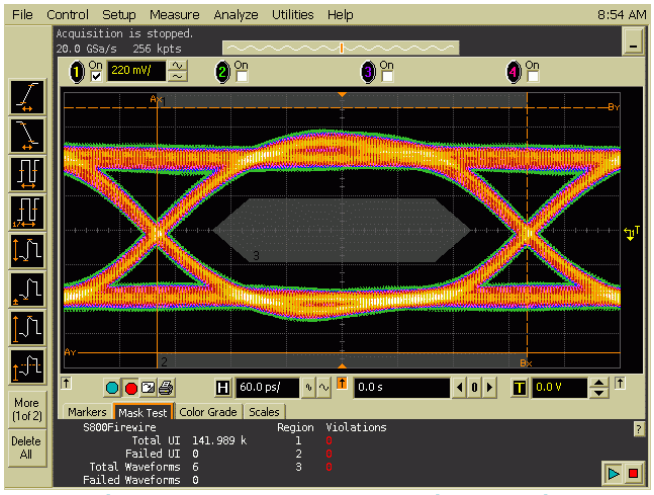

Figure 8g: Tx Eye at 500mVswing & 3.5dB Pre-emphasis, [0110]

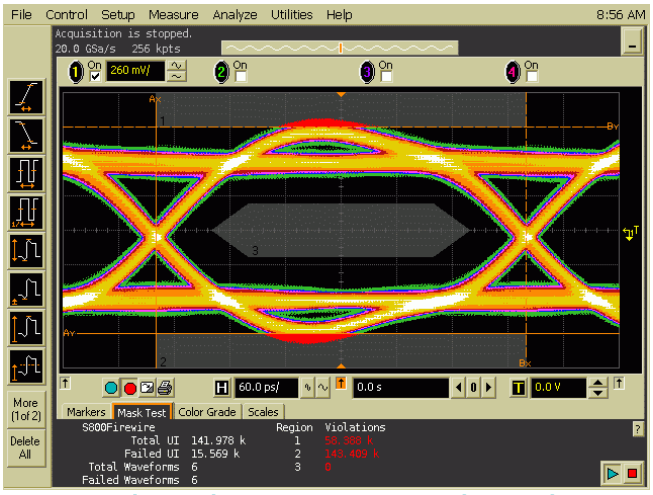

Figure 8h: Tx Eye at 500mVswing & 6dB Pre-emphasis, [0111]

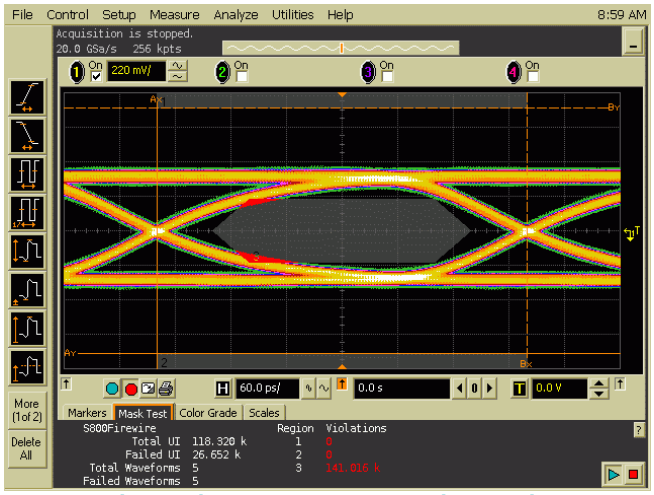

Figure 8i: Tx Eye at 400mVswing & 0dB Pre-emphasis, [1000]

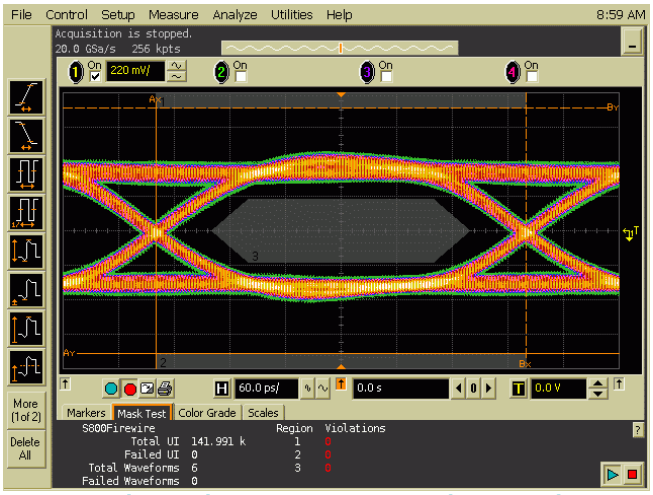

Figure 8j: Tx Eye at 400mVswing & 3.5dB Pre-emphasis, [1001]

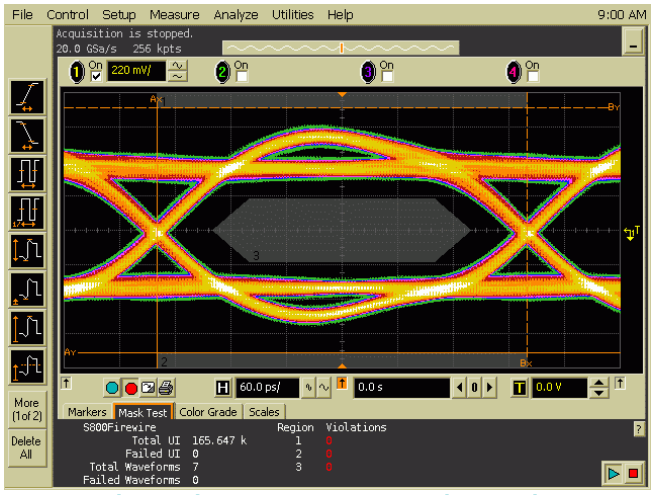

Figure 8k: Tx Eye at 400mVswing & 6dB Pre-emphasis, [1010]

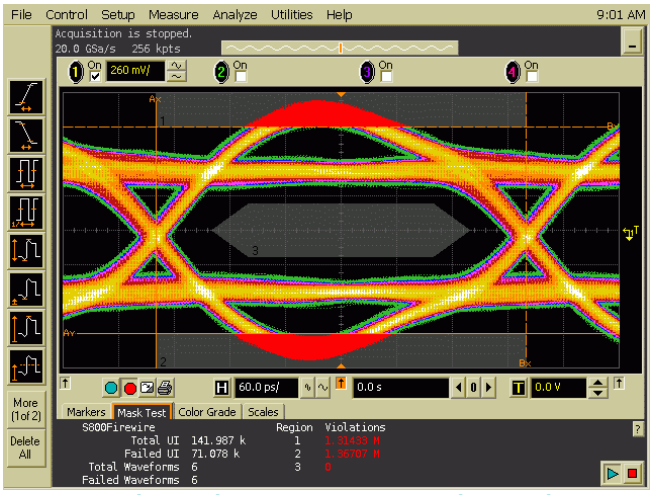

Figure 8l: Tx Eye at 400mVswing & 9dB Pre-emphasis, [1011]

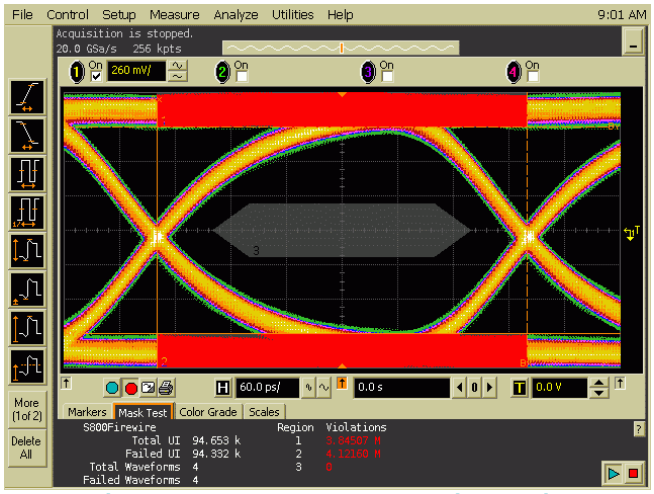

Figure 8m: Tx Eye at 1000mVswing & 0dB De-emphasis, [1100]

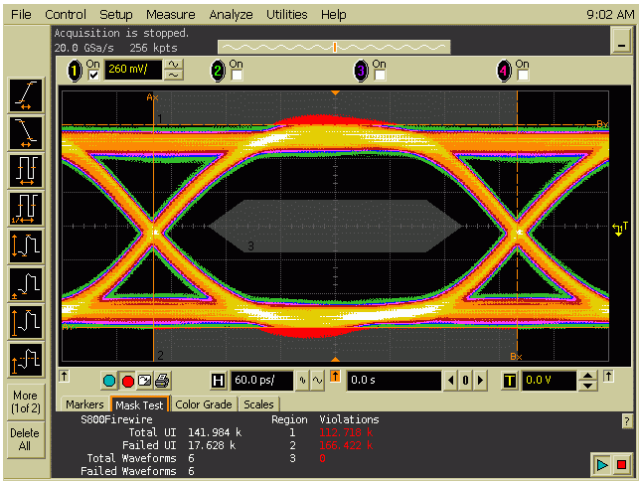

Figure 8n: Tx Eye at 1000mVswing & -3.5dB De-emphasis, [1101]

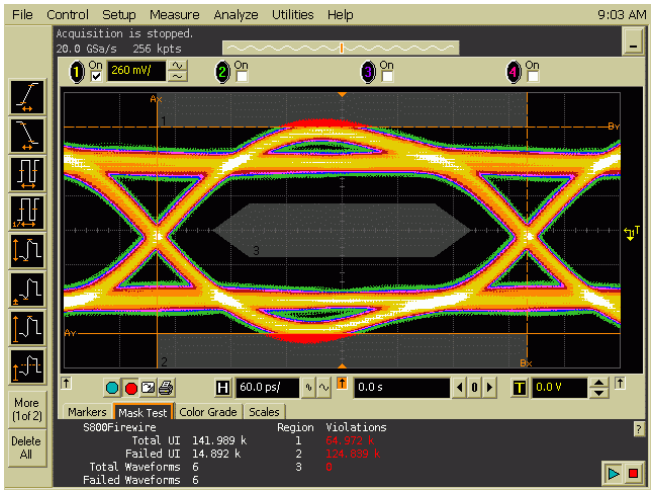

Figure 8o: Tx Eye at 1000mVswing & -6dB De-emphasis, [1110]

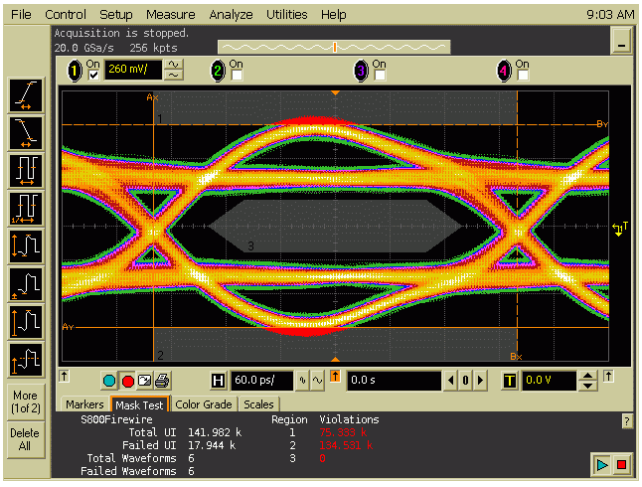

Figure 8p: Tx Eye at 1000mVswing & -9dB De-emphasis, [1111]

Optimum EQ Settings with 500mV Swing and 0dB Pre-emphasis

To show how equalization works on PI3VDP411LS(T), eye masks are captured to determine the optimum equalization settings for various cable lengths. Output swing and pre-emphasis are set to 500mV and 0dB, respectively, throughout the test.

Trace+Cable Length	Optimum EQ Setting
10 inch	3dB
16 inch	3dB
42 inch	7.2dB
58 inch	10dB

Table 4: Test Result of EQ Settings

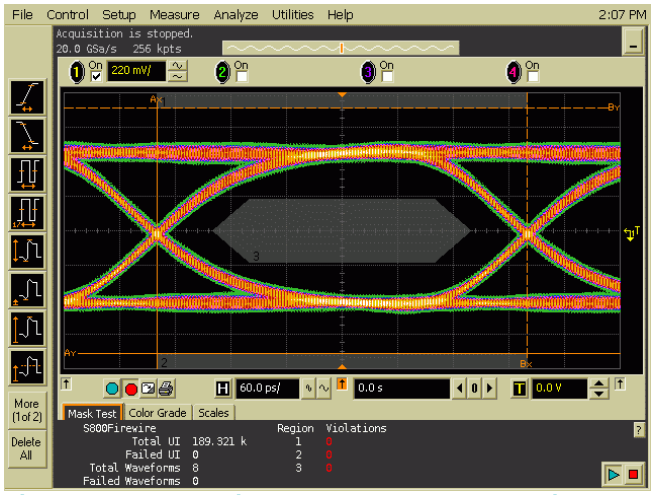

Figure 9a: 500mVswing Tx Eye at 10" Trace & 3dB EQ

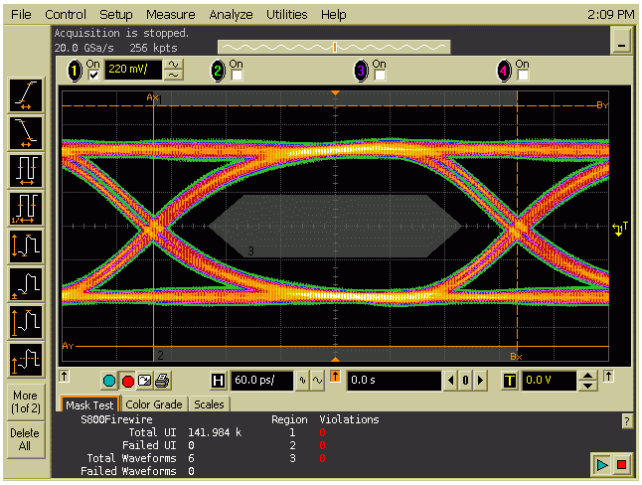

Figure 9b: 500mVswing Tx Eye at 10" Trace & 7.2dB EQ

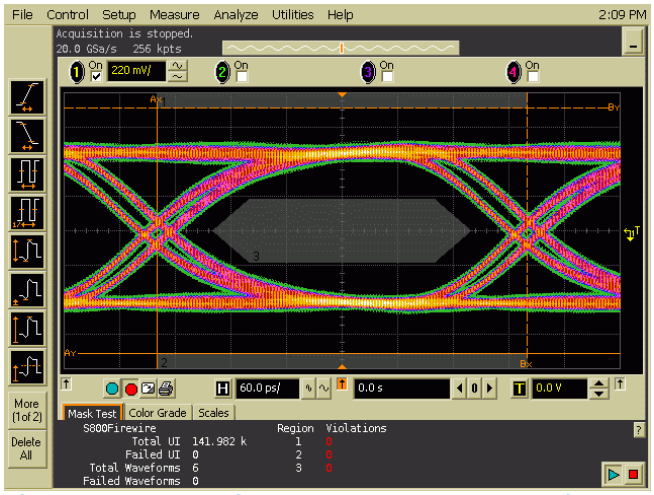

Figure 9c: 500mVswing Tx Eye at 10" Trace & 10dB EQ

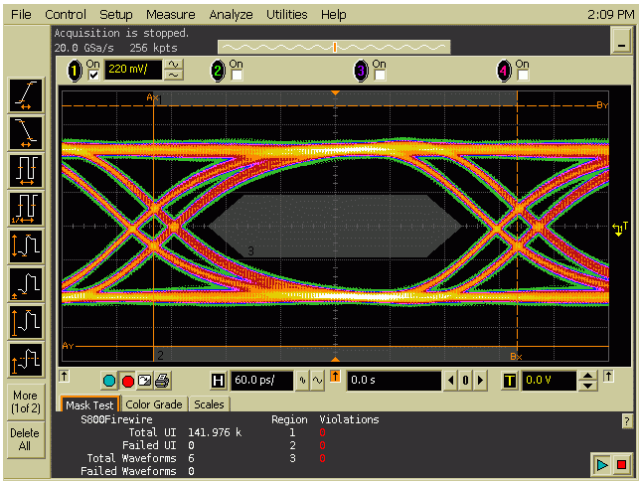

Figure 9d: 500mVswing Tx Eye at 10" Trace & 12dB EQ

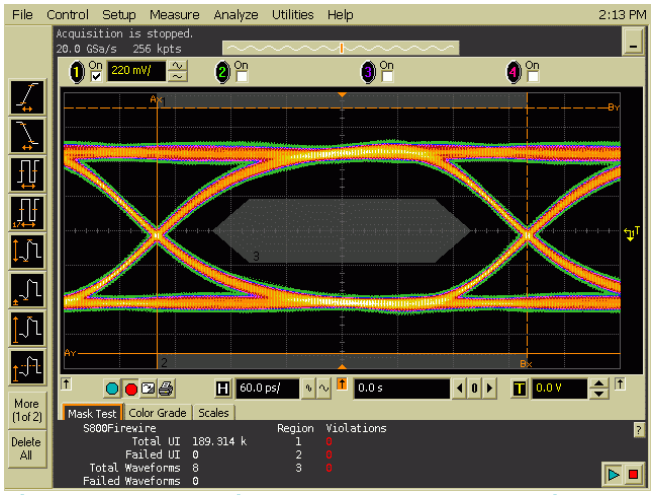

Figure 9e: 500mVswing Tx Eye at 16" Trace & 3dB EQ

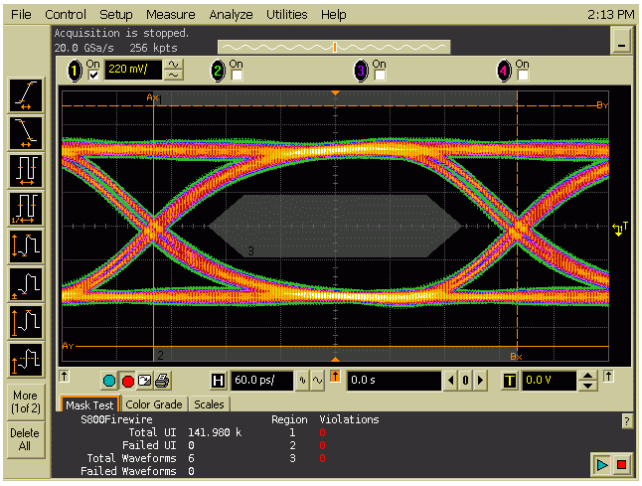

Figure 9f: 500mVswing Tx Eye at 16" Trace & 7.2dB EQ

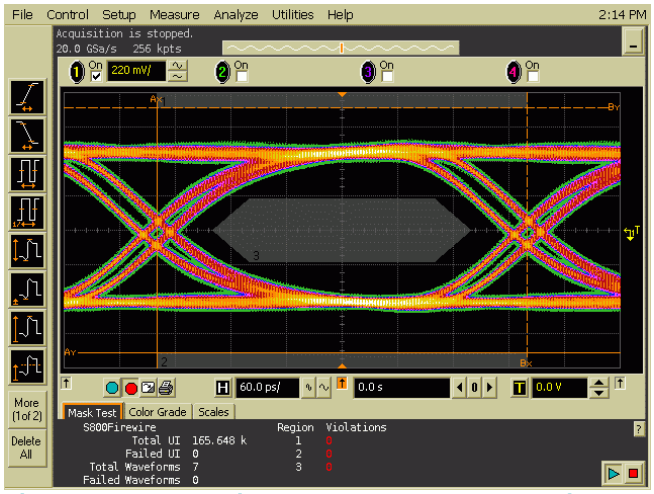

Figure 9g: 500mVswing Tx Eye at 16" Trace & 10dB EQ

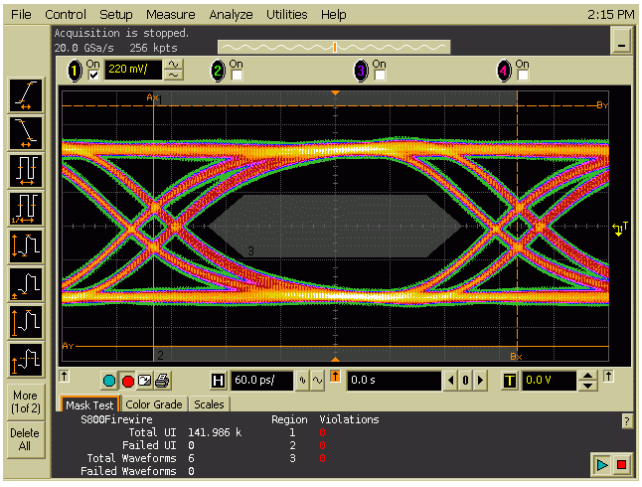

Figure 9h: 500mVswing Tx Eye at 16" Trace & 12dB EQ

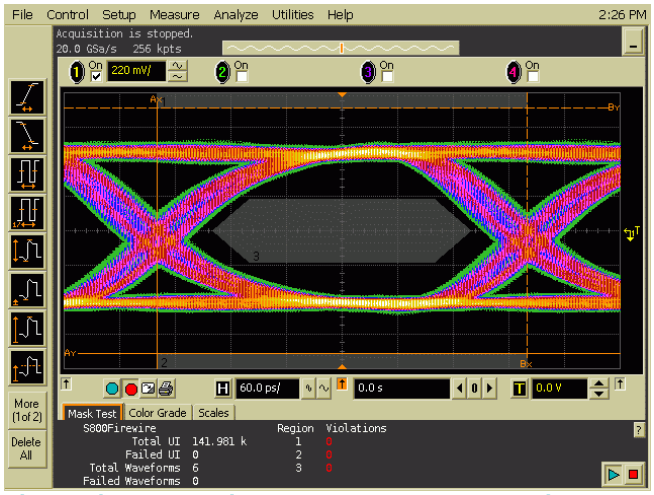

Figure 9i: 500mVswing Tx Eye at 42" Trace & 3dB EQ

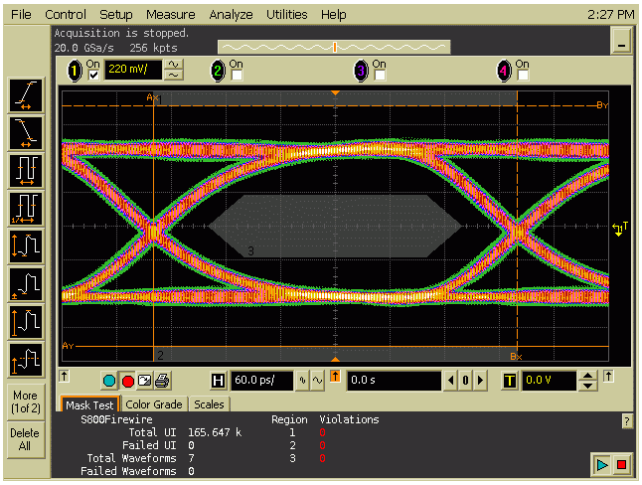

Figure 9j: 500mVswing Tx Eye at 42" Trace & 7.2dB EQ

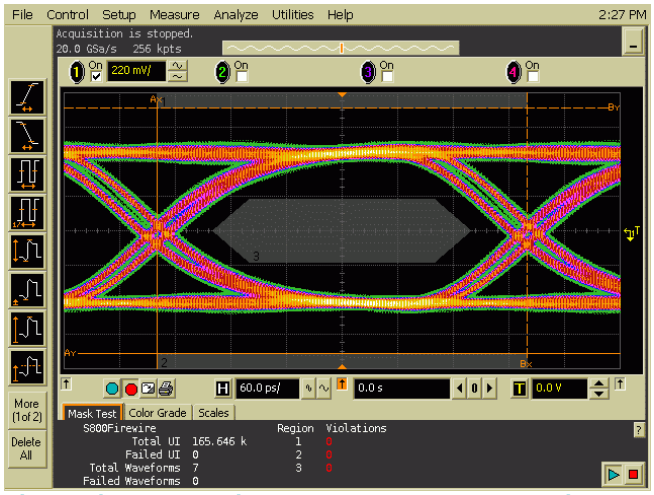

Figure 9k: 500mVswing Tx Eye at 42" Trace & 10dB EQ

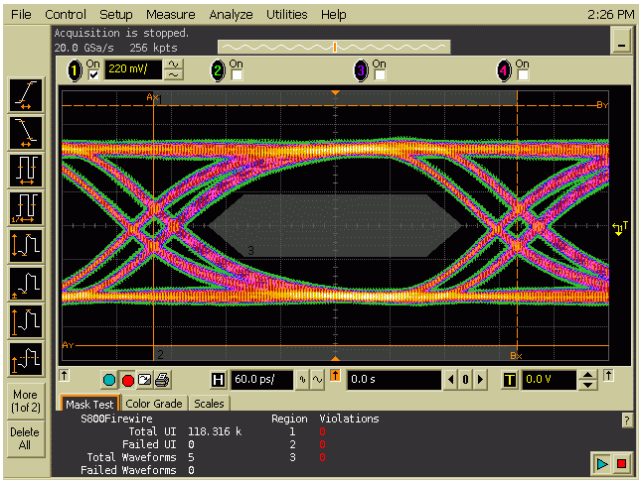

Figure 9l: 500mVswing Tx Eye at 42" Trace & 12dB EQ

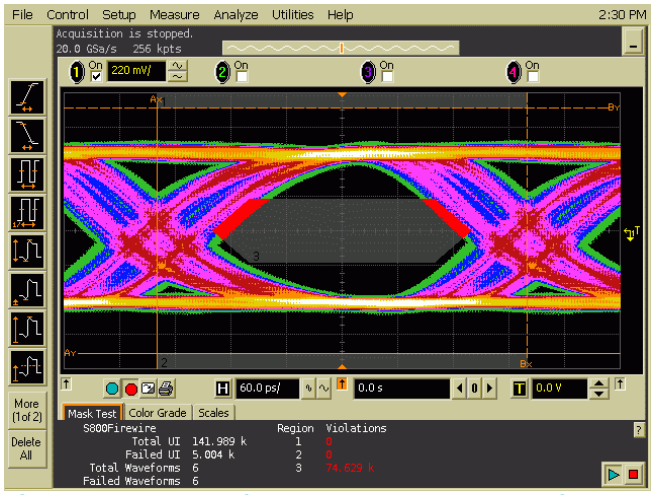

Figure 9m: 500mVswing Tx Eye at 58" Trace & 3dB EQ

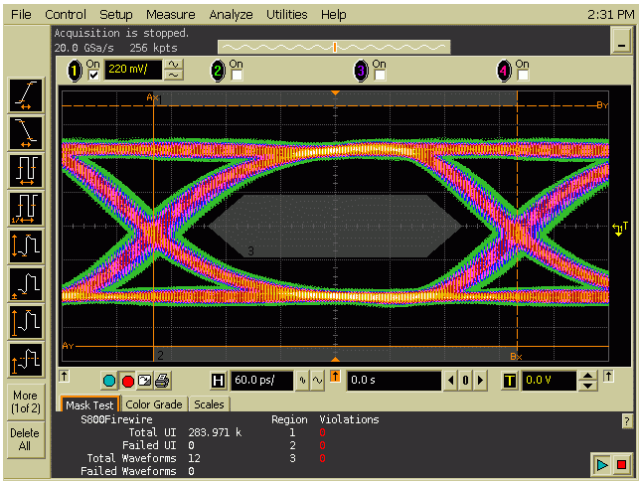

Figure 9n: 500mVswing Tx Eye at 58" Trace & 7.2dB EQ

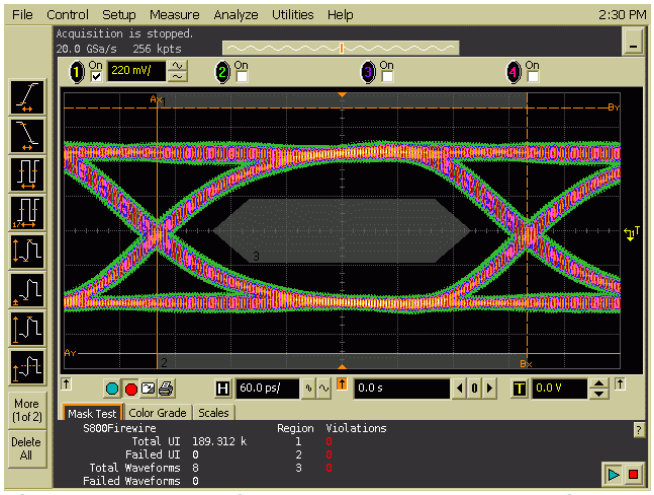

Figure 9o: 500mVswing Tx Eye at 58" Trace & 10dB EQ

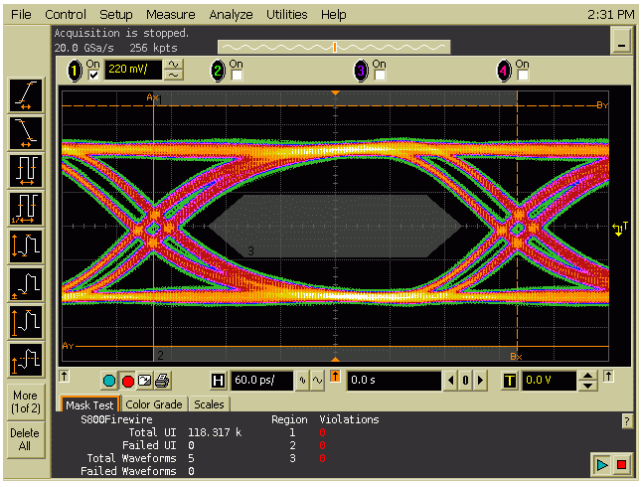

Figure 9p: 500mVswing Tx Eye at 58" Trace & 12dB EQ