Hardware Implementation Guide for PI7C8140A

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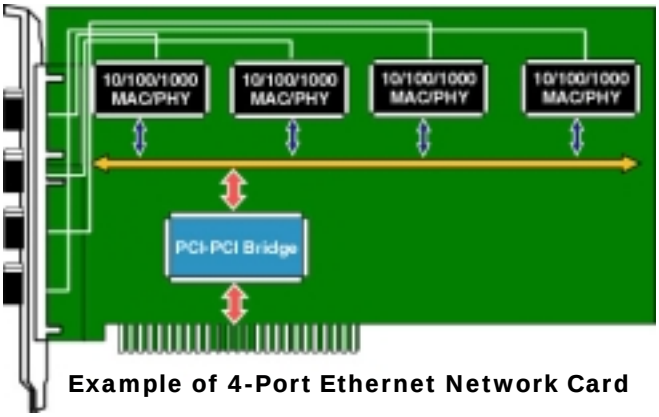
Introduction

The PCI interface was originally created for the personal computing industry. It used to be adapted by system designers who incorporated it into Datacom, Telecom, PCs, Servers, and many other systems. Today, the PCI interface is generally used as an expansion bus to add PCI slots onto system motherboards that have wide ranging applications. It is also used in add-in cards since most systems have PCI slots available to insert the PCI add-in cards. The PI7C8140A PCI-to-PCI Bridge is a 32-bit, 66 MHz capable chip that can be used either within an add-in card or on a motherboard.

Schematic and Layout Guidelines

This section has guidelines for hardware implementation of the Pericom PI7C8140A PCI-to-PCI Bridge in an add-in card or system motherboard.



Example of 4-Port Ethernet Network Card

Power

The chip core is operating with 3.3V V_{DD} power and support 3.3V and 5V environment signal.

Clock Frequency

Regardless of the status of M66EN (PCI connector signal 49B) at either PCI bus, the input clock frequency at signal P_CLK will always be the frequency used for S_CLKOUT[3:0]. A motherboard with PCI slots might have any speed device inserted, but an add-in card usually has embedded devices. Therefore an add-in card with appropriate 66 MHz PCI capable devices could be designed to 66 MHz tolerances, and function in both 33 and 66 MHz environments using the low cost PI7C8140 rather than higher pin count/cost alternative model bridges.

Miscellaneous Signal Connections

For PI7C8140:		
Pin name	**location**	**Requested value**
S_SERR_L	Pin 68	Pull high to V_{DD} through 5.1K ohm resistor
S_PERR_L	Pin 69	Pull up
S_STOP_L	Pin 70	Pull up
S_DEVSEL_L	Pin 71	Pull up
S_TRDY_L	Pin 72	Pull up
S_IRDY_L	Pin 73	Pull up
S_FRAME_L	Pin 74	Pull up
SCAN_TM_L	Pin **65**	Pull up
SCAN_EN	Pin **106**	Can be NC (no connect)
For **each PCI** slot:		
Pin name	**location**	**Requested value**
REQ#		Pull high to V_{DD} through external resistor
ACK64#		Pull up
REQ64#		Pull up
SMBCLK	(A40)	Pull up
SMBDAT	(A41)	Pull up

Output Clocks

Each secondary clock output is limited to one load, and 4 clocks driving each embedded PCI devices/slots. All secondary clock traces including feedback should have the same length as to deliver the clock at the same time at their respective destinations. This means that the furthest secondary bus device from the bridge governs the effective secondary bus clock trace lengths. Unused clock outputs can be disabled by writing to the bridge configuration register at offset 68h, or terminated electrically.

Clock lines are best terminated with a series termination resistor. The value of resistor is depends on the impedence of your transmission lines. Our 65-ohm trace impedence reference board uses 22-ohm resistors placed close to the bridge; some designs use as little as 10-ohms and others as much as 33-ohms, with 50-ohm to 75-ohm trace impedence's could be used from each PCI connector then routed around our bridge out to the primary PCI bus with some pull up resistor. There is no clock programming circuit required by hardware; normally all secondary clock outputs are enabled. Likewise there are no GPIO pins, JTAG scan port.

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3.3Vaux: This power source, if implemented on your design, should be applied from the primary PCI connector around the bridge to the secondary bus connectors.

Power Decoupling

In order to reduce noise at V_{DD} or ground from impacting the bridge, place 4 sets of decoupling capacitors top and bottom as close as possible to each corner of the bridge IC. These should be {0.1 uF, 0.01 uF, 0.001 uF} on bottom side and be {10 uF, 0.1 uF, 0.01 uF, 0.001 uF} top side. These are in addition to further decoupling at the PCI primary interface and secondary slots as needed per PCI specification 2.2, section 4.4.2.1: "power decoupling".

For add-in cards, please add the following decoupling capacitors at the edge connector, for 3.3V and 5V pins, with values {0.1 uF, 0.01 uF, 0.001 uF}. Use high quality, low ESR surface mounted ceramic capacitors.

PCI INTERRUPTS

PCI interrupts are processed at the motherboard south bridge, which sits on the primary PCI bus (thus upstream from the 8140). Thus there aren't signals at the bridge for interrupt processing; rather during layout the board designer routes the INTA#, INTB#, INTC#, and INTD# signals directly to the corresponding signals on the primary bus.

When the secondary bus is to have PCI connectors, the pin position of the PCI INTx# signals rotate from slot to slot, per PCI specification 2.2, section 2.2.6 (page 14).

Additional PCI signals per PCI specification 2.2, section 2.2.7: PRSNT[1:2] Normally these are pulled high with a decoupling capacitor to ground on the secondary bus.

PME# Power Management Event signal, an optional signal.
The 8140A doesn't have a PME# pin, so if your design plans to use power management events, bus the PME# signal on the secondary bus around the bridge and out the primary bus edge connector.

Hot-Swap

Compact PCI (cPCI) Hot-Swap (PICMG 2.1, R1.0) defines a process for installing and removing PCI boards form a Compact PCI system without shutting down the system power. The PI7C8140A is Hot-Swap Friendly silicon that supports all the cPCI Hot Swap Capable features and adds support for Software Connection Control. Being Hot Swap Friendly, the bridge supports the following:

- Compliance with PCI Specification 2.2
- Tolerates V_{CC} from Early Power
- Asynchronous Reset
- Tolerates Pre-charge Voltage
- I/O Buffers Meet Modified V/I Requirements
- Limited I/O Pin Leakage at Pre-charge Voltage

The bridge provides two pins to support hot swap: ENUM# and LOO. The ENUM# output indicates to the system that an insertion event occurred or that an extraction is about to occur. The LOO output lights an LED to signal insertion- and removal-ready status.

Four layer board recommendation

For 5V or mixed signaling environments, we recommend a 4-layer board arranged as follows:

Top	Route clock and other critical signals on top
Internal plane 1	Ground
Internal plane 2	3.3 V, 5V, 12V, -12V
Bottom	Signal connections

Do NOT route high frequency bus signals under the bridge.

Signal layers should be separated by ground planes, and no signals routed between ground and power planes. Use FR-4 material for board fabrication.

General layout guidelines:

1. Limit your trace lengths. Longer traces display more resistance and induction and introduce more delays. It also limits the bandwidth that varies inversely with the square of trace length.
2. Use higher impedence traces. Raising the impedence will also increase the bandwidth. Per PCI specification 2.2, section 4.4.3.3 trace impedence should be controlled to be within 60 to 100 ohms range.
3. Do not use any clock signal loops. Keep clock lines straight when possible.
4. For related clock signals that have skew specifications, match the clock trace lengths.
5. Do not route signals in the ground and V_{CC} planes.
6. Do not route signals close to the edge of the PCB board.
7. Make sure there is a solid ground plane beneath the bridge IC (PI7C8140A).
8. The power plane should face the return ground plane. No signals should be routed between power and ground.
9. Route clock signals on the top layer and avoid vias for these signals. Vias change the impedence and introduce more skew and reflections.
10. Do not use any connectors on clock traces.
11. Use wide traces for power and ground.
12. Keep high-speed noise sources away from the PI7C8140A.
13. Remember that per PCI spec 2.2 sec 4.4.3.1, the PI7C8140A should have a primary PCI edge connector to PQFP pad trace distance of not more than 1.5 inches (37.5 mm) for signals coming from the primary PCI interface. Secondary interface signals would then be limited as in PCI motherboard layout rules.

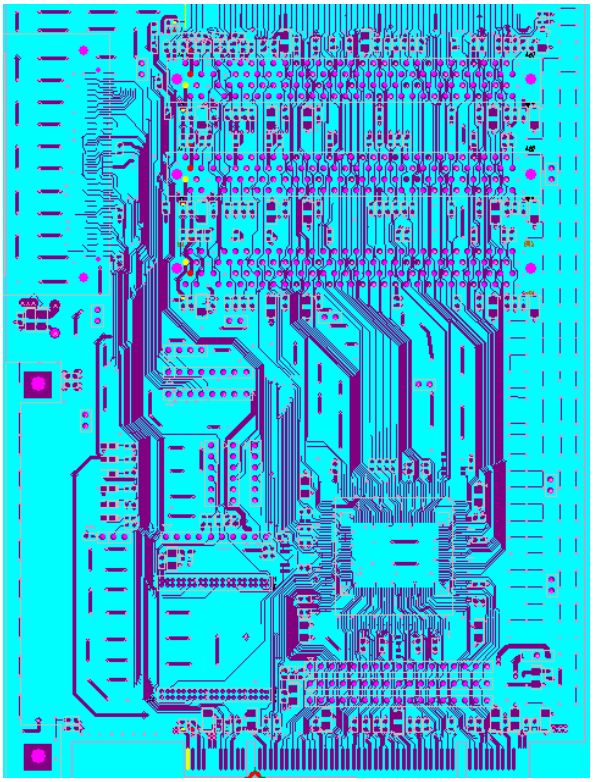

Figure 1: Top Layer

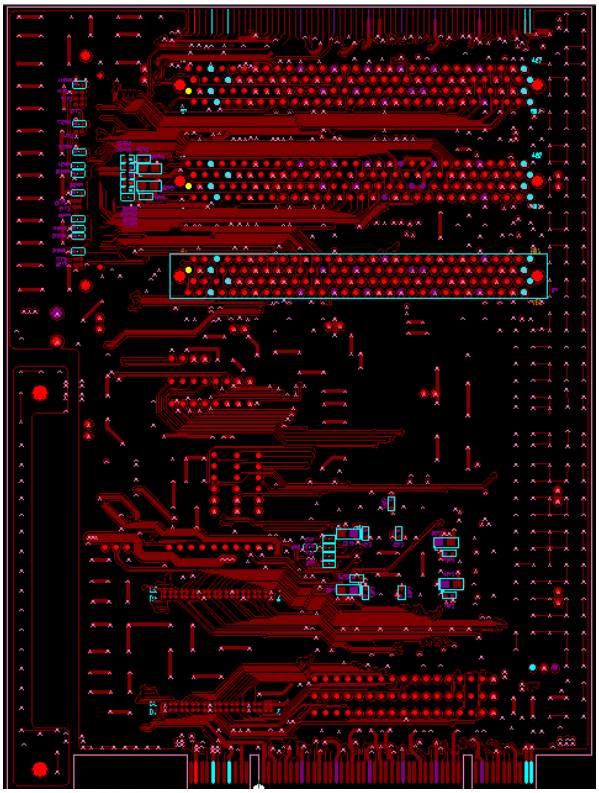

Figure 2: Bottom layer

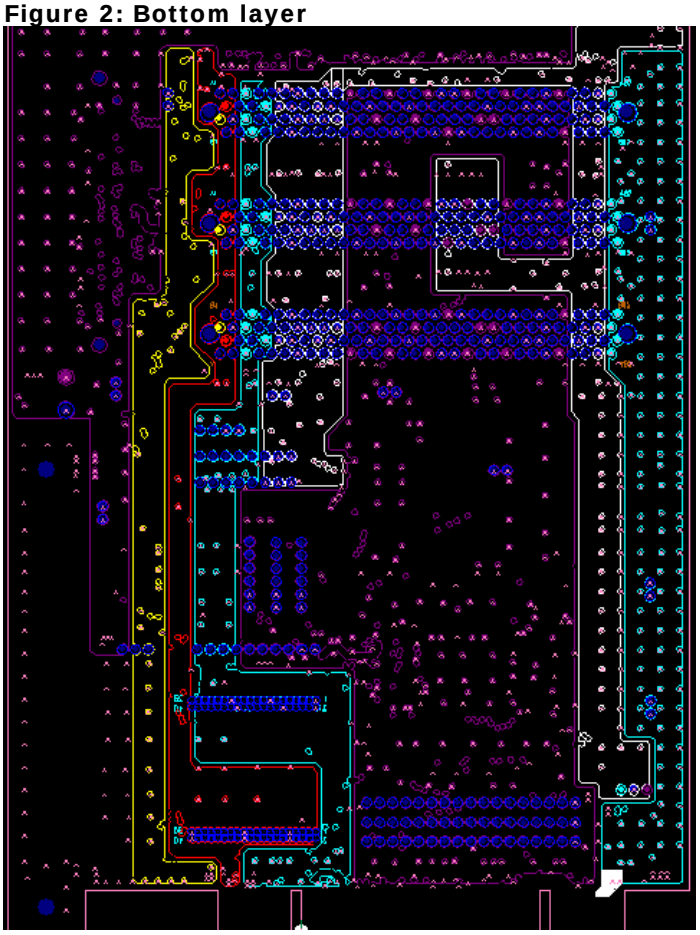

Figure 3: Power layer

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References

1. Pericom Semiconductor App Note #58. *"Hardware Implementation Guide for the PI7C8152"*
2. Pericom Semiconductor App Note #22. *"Solutions to Current High-Speed Board Design"*
3. PCI Local Bus specification 2.2 section 4.4 *"Expansion Board Specification" [decoupling* through *routing recommendations* and *impedence* sections*]* p.150-152.
4. PCI Local Bus specification 2.2 section 4.2.6 *Pinout recommendation.* p131.
5. PCI Local Bus specification 2.2 section 4.3.3. *Pull-ups* p.136.
6. Compact PCI PICMG 2.0 R3.0. p.17-20 *"Electrical Requirements"*.
7. Pericom Semiconductor App Note #31 *"Zero-Delay Clock Buffer Layout and Schematic Guidelines"*. p1.

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