Interface Between NECL and LVDS

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Introduction

Because of the inherent characteristics of bipolar circuit techniques, which use differential pairs for logic state switching and an emitter follower for the output stage, the ECL (Emitter Coupled Logic) family has been widely used for high-speed signal interface (see Figure 1). Although the operating voltage has been moved from +5V or –5V parts to +3.3V parts, some legacy devices and very high-speed operation still use ECL logic devices for subsystem and peripheral devices. As more applications use LVDS as an interface media, owing to its low EMI and better signal integrity for long distance transmission, this paper suggests methods for interfacing between NECL and LVDS. For PECL and LVDS interface, please refer to Pericom's Application Brief 23 and Pericom's LVDS driver and receiver data sheets (PI90LV17 and PI90LV18). Some ECL logic and LVDS operation conditions are listed in Table 1.

Table 1. ECL logic family and LVDS operating conditions.

Family	V_{CC}	V_{EE}	V_{oh} (max)	V_{oh} (min)	V_{ol} (max)	Vol (min)
NECL	GND	–5.2V	–0.88V	–1.025V	–1.62V	–1.81V
PECL	5V	GND	4.12V	3.975V	3.38V	3.19V
LVPECL	3.3V	GND	2.42V	2.275V	1.68V	1.49V
LVDS	3.3V	GND	1.6V	—	—	0.9V

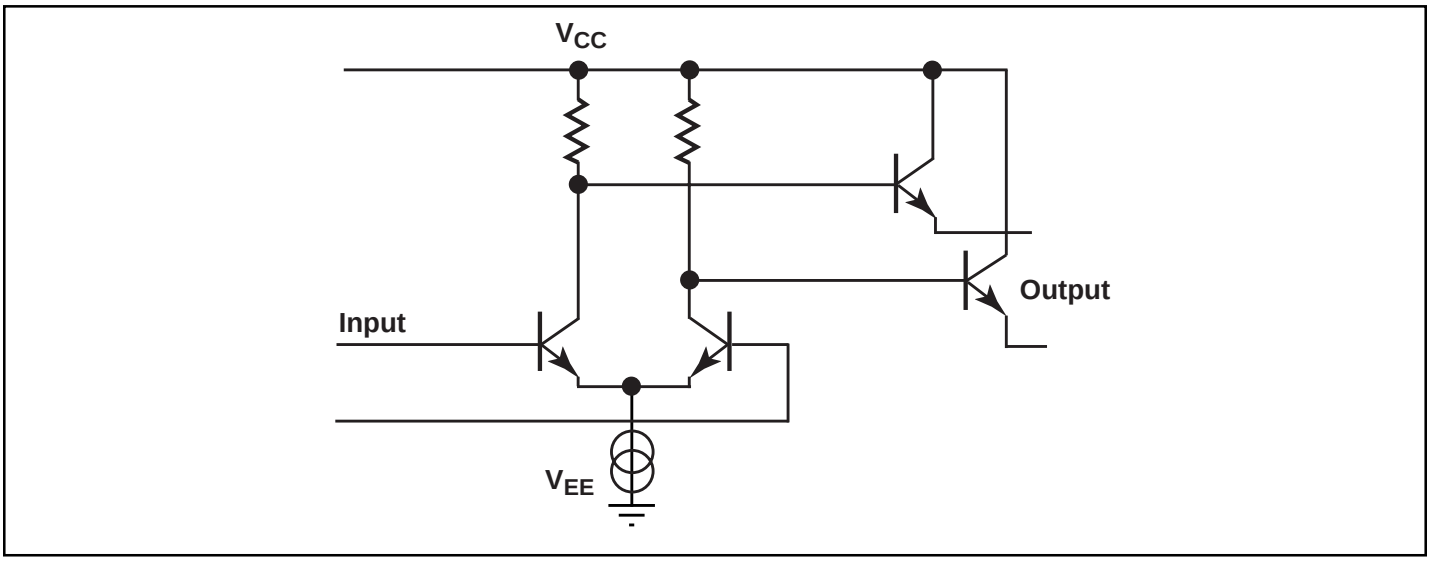

Figure 1. Typical ECL logic circuit structure

The LVDS device operates from a 3.3V positive supply voltage, whereas a NECL device operates from a –5.2V negative supply voltage. If we want to combine these two different operating conditions we must adjust the difference. A common way to do this is to add coupling capacitors between these two parts for DC bias point reconstruction and use a resistive network to adjust the signal within the receiver's input range.

LVDS to NECL Interface

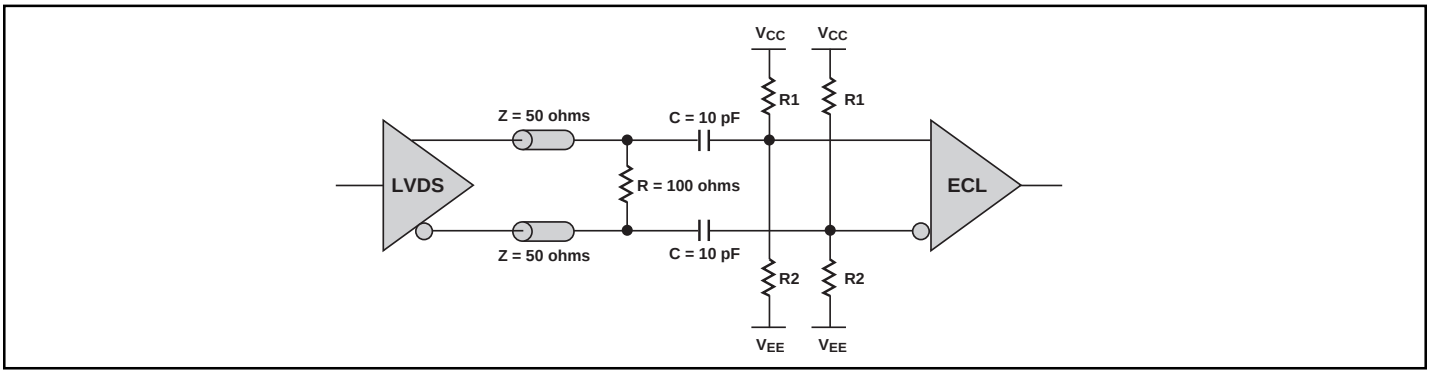

Figure 2. LVDS to NECL Interface.

In Figure 2, coupling capacitors (C = 10pF) block DC voltage coming from the LVDS driver. The DC bias point for the NECL receiver is constructed by the resistive network R1 and R2. A typical LVDS swing is ±350mV with 100-ohm load resistor. Therefore, bias voltage, Vbias, can be calculated from the limitations of V_{oh} (min) and V_{ol} (max).

For positive direction swing: Vbias + Vswing > Voh(min)

For negative direction swing: Vbias - Vswing < VoL (max)

Then

Vbias + 0.35V > –1.025V

Vbias – 0.35V < –1.62V

We can get the limitations for Vbias as

–1.375V < Vbias < –1.27V

For V_{CC} = GND and V_{EE} = –5.2V, we can choose R1 = 1K ohm and R2 = 3K ohms when Vbias = 1.3V.

NECL to LVDS Interface

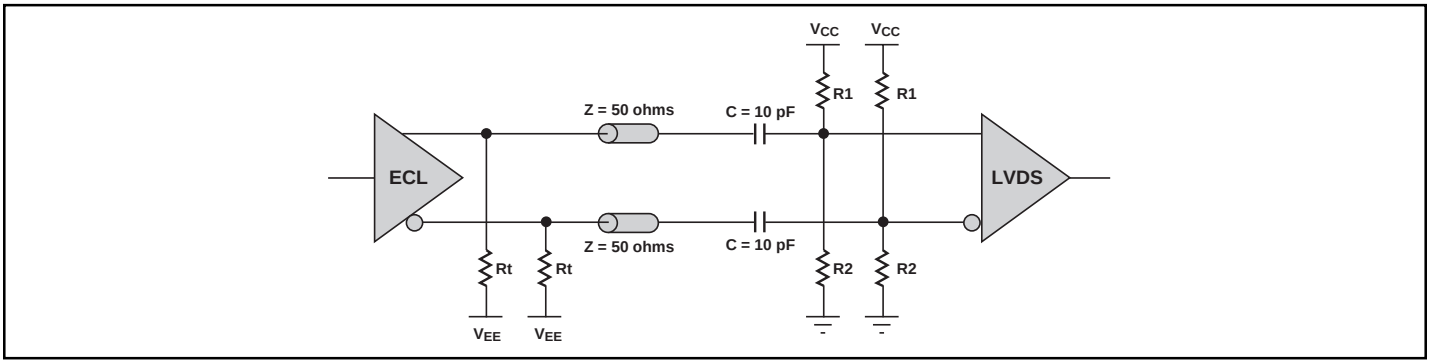

Figure 3. NECL to LVDS Interface.

The ECL device has an emitter follower for the output stage (Figure 1) that needs termination resistors at output pins. To not affect impedance seen by the ECL device as 50 ohms, termination resistance can be chosen to be as large as possible by comparing it with 50 ohms. Actual resistor value depends on the signal's falling speed demand. As ECL has no sink capability, termination resistor Rt, and the loading capacitor, determinethe falling signal's speed. Resistors R1 and R2 provide input bias voltage to the LVDS receiver and also provide the transmission line termination resistor.

So, R1 and R2 should satisfy the following conditions,

R1 // R2 = 50 ohms

V_{CC} * [R2 / (R1 + R2)] = Vbias

For LVDS receiver's input common mode voltage of 1.2V, then

R1 // R2 = 50 ohms

3.3V * [R2 / (R1 + R2)] = 1.2V

So, R1 = 138 ohms and R2 = 79 ohms.

Conclusion:

Using AC signal coupling and DC bias voltage reconstruction, we can easily acheive the adaptation between NECL and LVDS signals. To get the parameter settings according to the circuit's boundary conditions, the analytic method that we present here for circuit parameters analysis can help to get adequate parameter settings.