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Chapter1. Introduction

1.1 General Description

AP3917B is an off-line universal AC Voltage input step-down regulator that provides accurate constant voltage (CV), outstanding low standby power, light loading efficiency and dynamics performance based on non-isolated buck topology.
The AP3917B EV1 Evaluation Board provides good design example for a cost-effective 1.44W single output 12V@120mA power application useful in home appliance powers.

1.2 AP3917B Key Features

- Universal 85V to 265V V_{AC} Input
- Internal MOSFET 650V (16Ω)
- Maximum output Current: 170mA typ.@5V output
- Up to 2W Output Power
- Low Standby Power Consumption (<30mW at no loading)
- High Light Loading Efficiency and average efficiency can meet DOE IV and CoC V5 Tier 2
- Frequency Modulation to suppress EMI to meet EN55022 and FCC part 15 class B
- Rich Protection including: OTP, OLP, OLD,SCP
- Extremely low system component count
- Totally Lead-free & Fully RoHS Compliant (SO-7)
- Halogen and Antimony Free. "Green" Device

1.3 Applications

- Non-Isolated Home Appliances including: AC Fans, Rice Cooker, Air conditioner, Coffee Machines, Soy Milk Machines, etc.
- Auxiliary Power to IoT Devices.

1.4 Board Pictures

Figure 1: Top View

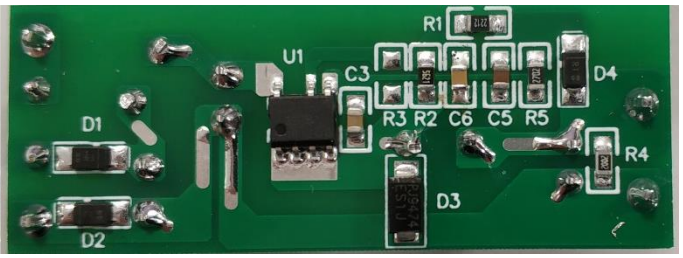

Figure 2: Bottom View

Chapter2. Power Supply Specification

2.1 system performance

The system performance included in and output characters, specifications, EMC, protection, etc.

		Min.	Typ.	Max.	Comments
Input characters					
Input AC voltage rating		100V/60Hz	115/230	240V/50Hz	Two wires, no PE
Input AC voltage range		85V/60Hz	-	265V/50Hz	
Input AC frequency range		47Hz	50/60	63Hz	
Output characters					
Output voltage		11.4V	12V	12.6V	Tested at board terminal
Output tolerance		-		±5%	
Loading current		0	-	120	mA
Performance Specifications					
Standby power		-	25.0	30mW	@230V/50Hz
Efficiency standard	10% load eff.	59.42%	69.93%	-	DoE VI: 69.39% CoC V5 tier 2: 69.42%/59.42%
	Avg. eff.	69.42%	83.15/79.41%	-	
Load regulation		-	±1.17%	±5%	Tested at board terminal
Line regulation		-	±0.18%	±2%	Tested at board terminal
Ripple & Noise		-	90mV	100mV	@full load and full voltage range
Startup time		-	41ms	50ms	85V/60Hz
EMC Test					
ESD test	Air	15kV	-	-	@100ohm concrete resistor
	Contact	8kV	-	-	
EFT test		2kV	-	-	±5kHz/100kHz
Surge Test		1kV	-	-	Differential mode, 2ohm, 1.2/50us
Conducted EMI	110V	6dB margin	-	-	FCC Part 15 Class B
	230V	6dB margin	-	-	EN55032
Protection Functions					
SCP test		-	-		OK
OLD test		-	-	-	OK
OLP test		-	8.2V	-	OK
OTP test		135℃	150℃	165℃	OK

2.2 Environment

Operation temperature: -20℃~85℃
Operation Humidity: 20%~90% R.H.
Storage temperature: 0~40℃
Storage Humidity: 0%~95% R.H.

Chapter3. Schematic and Bill of Material

3.1 Schematic

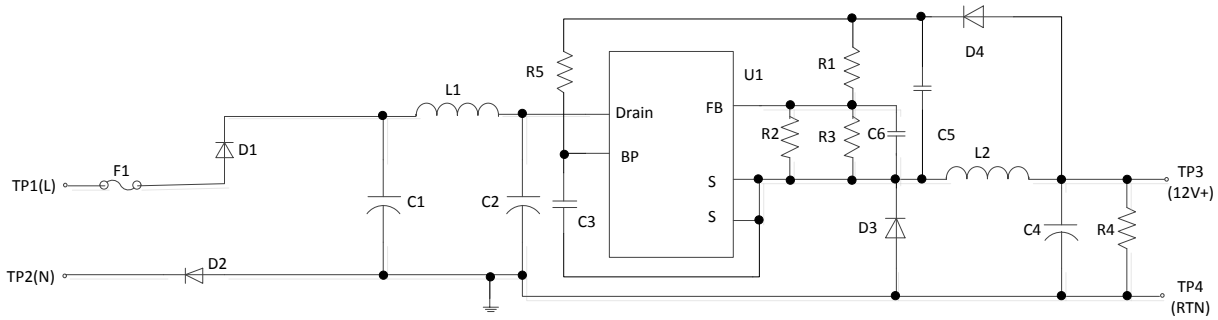

Figure 3: Evaluation Board Schematic

3.2 Bill of Material

Table 1: Bill of Material

Items	Designator	Description	Footprint	Qty.	Manufacturer
1	F1	10R, Fusible resistor	Φ3*10mm	**1**	OAHE
2	D1, D2	S1MWF, Slow type, mark F9	SOD123FL	**2**	Diodes
3	C1, C2	2.2uF/400V, Electrolytic capacitor	Φ6*9mm	**2**	Aishi
4	C3	2.2uF/25V, X7R	SMD 0805	**1**	Telesky
5	C4	150uF/25V, Electrolytic capacitor	Φ6*11mm	**1**	Aishi
6	C5	470nF/50V, X7R	SMD 0805	**1**	Telesky
7	C6（optional)	470pF/50V, X7R	SMD 0805	**1**	Telesky
8	D3	ES1J, Trr 35ns	SMA	**1**	Diodes
9	D4	RS1MSWFQ, Fast type diode, mark R1	SOD123F	**1**	Diodes
10	L1	1mH, Color ring inductor	DIP, 0510	**1**	Deloop
11	L2	1mH, Choke inductor	Φ9*12mm	**1**	Deloop
12	R1	22.1kΩ	SMD 0805, 1%	**1**	Panasonic
13	R2	5.62kΩ	SMD 0805, 1%	**1**	Panasonic
14	R3	NC	-	**0**	-
15	R4	20kΩ	SMD 0805, 5%	**1**	Panasonic
15	R5	27kΩ	SMD 0805, 5%	**1**	Panasonic
16	U1	AP3917B	SO7	**1**	Diodes
Total		17pcs			

Chapter4. The Evaluation Board Connections

4.1 PCB Layout

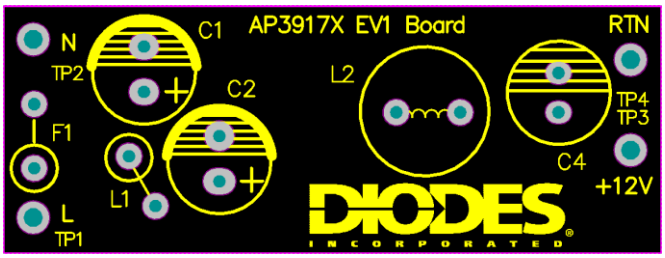

Figure 4: PCB Board Layout Top View

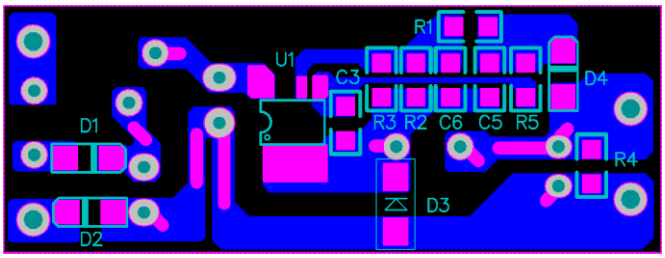

Figure 5: PCB Board Layout Bottom View

4.2 Circuit Description

4.2.1 Input EMI Filtering

The input stage is composed of fusible resistor F1, rectifier bridge DB1, filtering inductor L1, Capacitors C1 and C2. Resistor F1 is a flame proof, fusible, wire-wound resistor. It limits inrush current to safe levels for input rectifier diodes, provides differential mode noise reduction and acts as an input fuse in the event of short circuit.

4.2.2 Control IC

AP3917C co-packages a 650V power MOSFET and control circuitry into a cost-effective SO-7 package. The device is self-starting from the Drain pin with local supply decoupling provided by a small capacitor C4 (at least 100nF) connected to the BP pin when AC source is applied.

4.2.3 Output Rectification

During the ON time of U1, current ramps in L2 and is simultaneously delivered to the load. During the OFF time the inductor current ramps down via the free-wheeling diode D1, feedback diode D2, and the load. Diode D1 should be an ultra-fast diodes (Trr<50ns or lower). Capacitor C4 should be selected to have an adequate ripple margin (low ESR type).

4.2.4 Output Feedback

The voltage across L2 is rectified by C5 and D2 during the off-time of U1. For forward voltage drop of D1 and D2 is approximately equal, the voltage across C5 tracks the output voltage. To provide a feedback signal, the voltage across C5 is divided by R1 and R2. This voltage is specified for U1 at FB pin (2.5V). This allows the simple feedback to meet the required overall output tolerance of ±5% at rated output current.

4.3 Quick Start Guide

1. The evaluation board is preset at 12V/175mA from output.
2. Ensure that the AC source is switched OFF or disconnected before doing connection.
3. Connect the AC line wires of power supply to "L" & "N" connectors on the left side of the board.
4. Turn on the AC main switch.
5. Measure "+V" & "GND" connectors to ensure correct output voltage, 12V.

CAUTION: This EV board is non-isolated. Do not touch anywhere there are electrical connections because they are all coupled to high voltage potential.

Chapter 5. System Test

5.1 Input & Output Characteristics

5.1.1 Input Standby Power

Standby power and output voltage is measured after 10-minute aging. The voltage data is tested at the PCB terminal. All data is tested at ambient temperature.

Table 2: Standby Power at no load Target Output Voltage

Input Voltage	Pin (mW)	Vo (V)
85V/60Hz	18.2	12.060
115V/60Hz	18.8	12.052
230V/50Hz	22.6	12.039
265V/50Hz	24.8	12.041

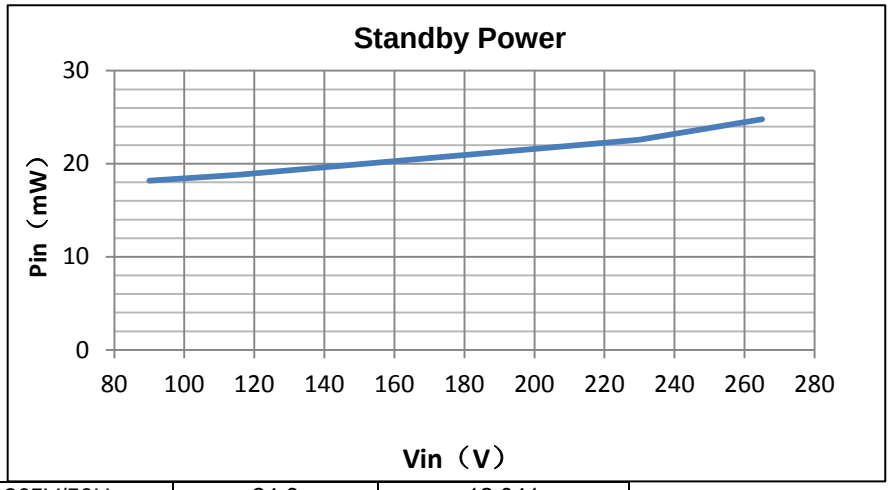

Figure 6: Standby Power versus Vin Curve

5.1.2 Efficiency

The efficiency data is measured after 10-minute aging, and it is tested at the PCB terminal. All the data is tested at ambient temperature.

Table 3: Efficiency Measurement

AC input voltage	Items	10%	25%	50%	75%	100%	Avg. Eff.
115V/60Hz	Vo (V)	12.010	11.889	11.822	11.770	11.984	83.15
	Io (A)	0.012	0.030	0.060	0.090	0.120	
	Pin (W)	0.185	0.434	0.852	1.268	1.720	
	Efficiency (%)	77.90	82.18	83.25	83.54	83.61	
230V/50Hz	Vo (V)	12.005	11.867	11.803	11.765	11.732	79.41
	Io (A)	0.012	0.030	0.060	0.090	0.120	
	Pin (W)	0.206	0.464	0.890	1.315	1.742	

	Efficiency (%)	69.93	76.72	79.57	80.52	80.82	

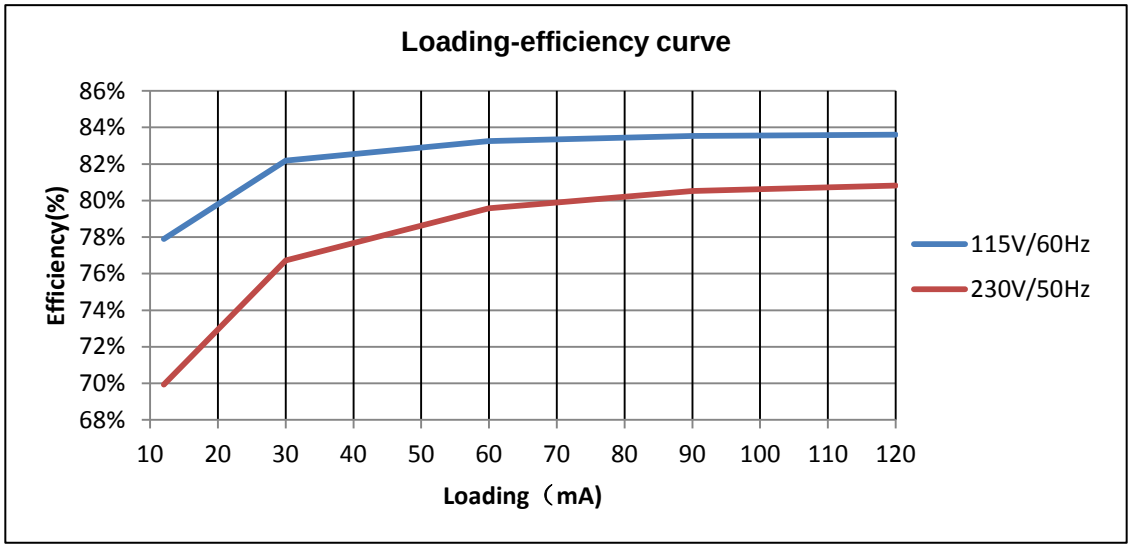

Figure 7: Loading-Efficiency Curve

5.1.3 Line and Load Regulation

The line and load regulation data is measured after 10-minute aging. The voltage data is tested at the PCB terminal. All the data is tested at ambient temperature.

Table 4: Line and Load Regulation Data

AC input voltage	Loading(mA)						
	0	10	20	30	40	50	60
85V/60Hz	12.060	12.053	12.016	11.997	11.965	11.936	11.913
115V/60Hz	12.052	12.054	12.014	11.985	11.962	11.937	11.912
230V/50Hz	12.039	12.035	11.993	11.967	11.943	11.933	11.904
265V/50Hz	12.041	12.036	11.996	11.954	11.944	11.921	11.922
Line Regulation	±0.13%	±0.08%	±0.10%	±0.18%	±0.09%	±0.07%	±0.08%
AC input voltage	**Loading(mA)**						**Load Regulation**
	70	80	90	100	110	120	
85V/60Hz	11.904	11.891	11.882	11.873	11.875	11.861	±1.17%
115V/60Hz	11.903	11.895	11.884	11.872	11.864	11.865	±1.16%
230V/50Hz	11.882	11.887	11.876	11.863	11.852	11.853	±1.04%
265V/50Hz	11.881	11.874	11.861	11.852	11.841	11.842	±1.10%
Line Regulation	±0.10%	±0.09%	±0.10%	±0.09%	±0.14%	±0.10%	

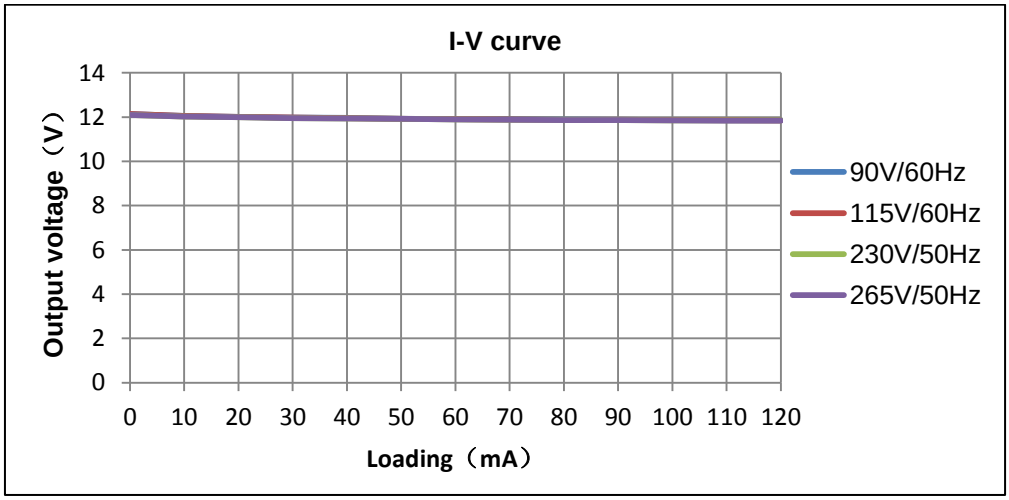

Figure 8: Output Voltage versus Loading Curve

5.2 Key Performance Test

5.2.1 Start Up Performance

The start-up time is measured with a differential probe across AC inputs, "L" and "N" connectors and a common low-voltage probe across output terminals, "+V" and "GND" connectors. Before starting up, buck capacitors should be discharged.

Table 5: Start Up Performance

AC input voltage	Loading conditions		Figures
	No load	Full load	
85V/60Hz	17.4ms	41.1ms	Fig. 9, Fig. 10
115V/50Hz	17.6ms	40.1ms	-
230V/50Hz	16.4ms	35.2ms	-
265V/60Hz	16.2ms	20.3ms	Fig. 11, Fig. 12

CH1:Vin; CH3:Vo

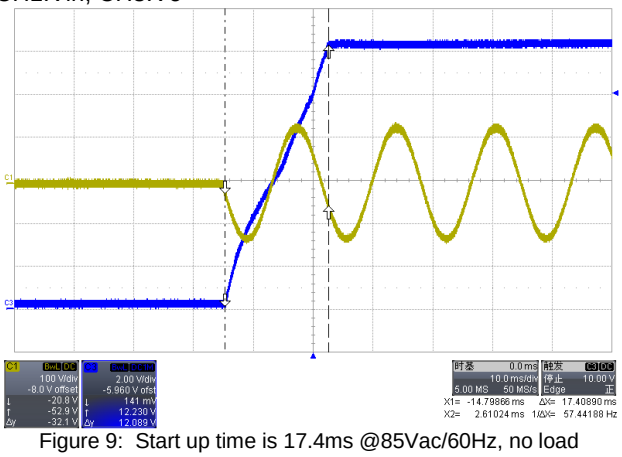

Figure 9: Start up time is 17.4ms @85Vac/60Hz, no load

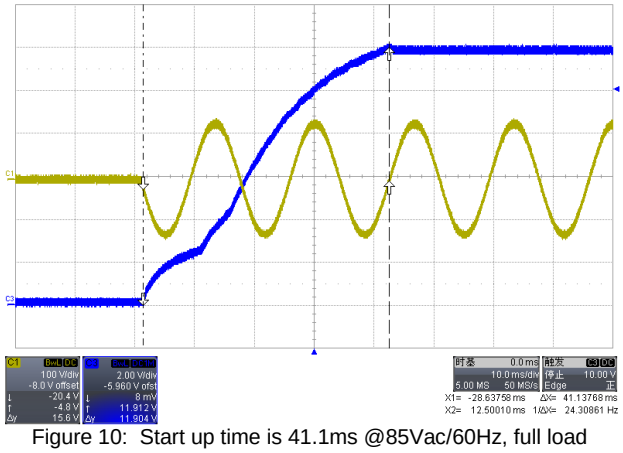

Figure 10: Start up time is 41.1ms @85Vac/60Hz, full load

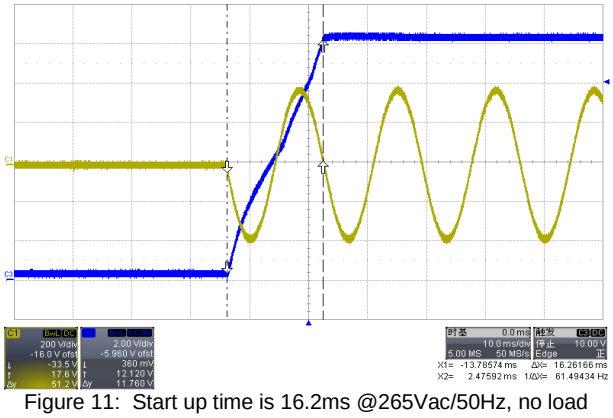

Figure 11: Start up time is 16.2ms @265Vac/50Hz, no load

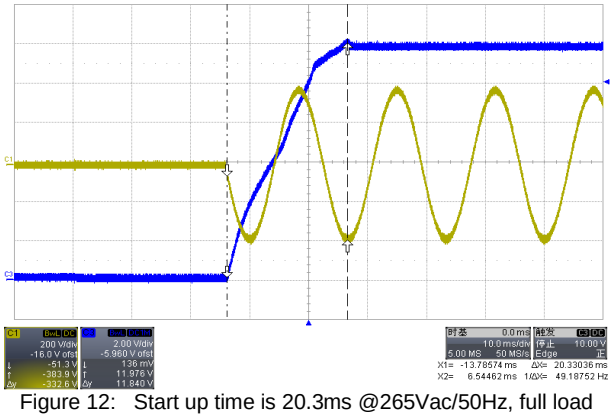

Figure 12: Start up time is 20.3ms @265Vac/50Hz, full load

5.2.2 Rise Rime

The rise time is measured with a common low-voltage probe across output terminals, "+V" and "GND" connectors. Before starting up, output capacitors should be discharged.

Table 6: Rise Time

AC input voltage	Loading conditions		Figures
	No load	Full load	
85V/60Hz	14.6ms	28.4ms	Fig. 13, Fig.14
115V/50Hz	14.4ms	27.0ms	-
230V/50Hz	13.9ms	17.3ms	-
265V/60Hz	13.8ms	13.4ms	Fig. 15, Fig.16

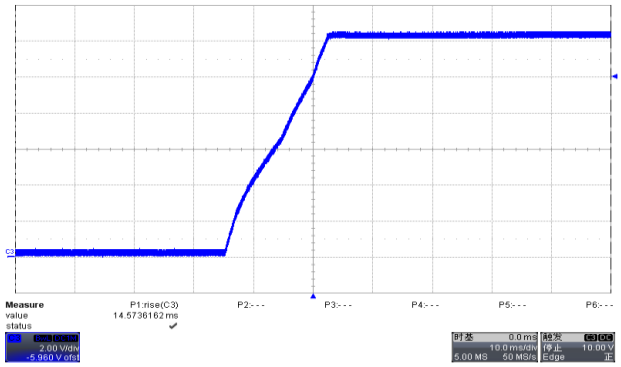

Fig. 13, Rise time is 14.6ms @85Vac/60Hz, no load

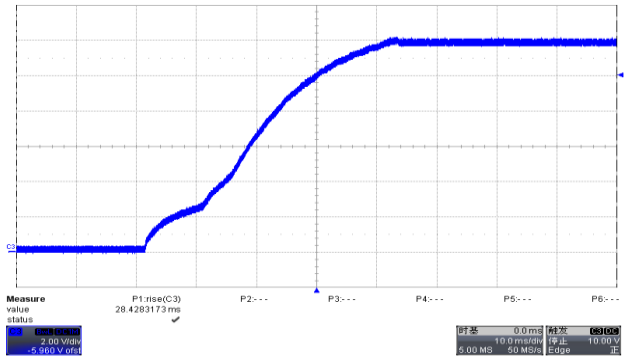

Fig 14, Rise time is 28.4ms @85Vac/60Hz, full load

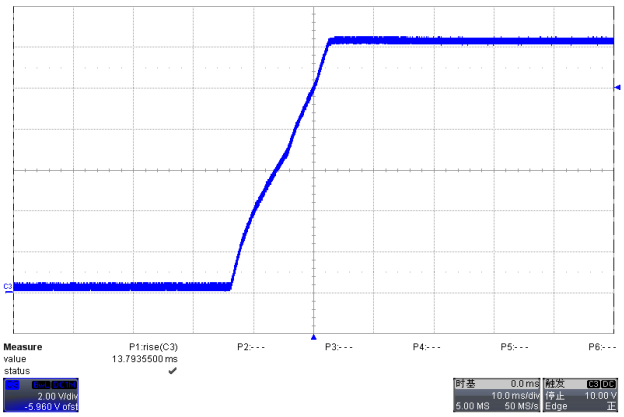

Figure 15: Rise time is 13.8ms @265Vac/50Hz, no load

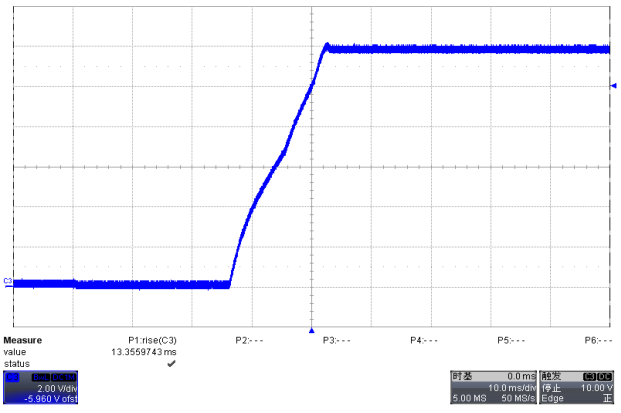

Figure 16: Rise time is 13.4ms @265Vac/50Hz, full load

5.2.3 Voltage Stress

The voltage is measured between the "Drain" and "S" pins of AP3917B. The test needs differential probes.

Table 7: MOSFET Drain-Source Voltage Stress

AC input voltage	Loading conditions		Figures
	No load	Full load	
85V/60Hz	135V	150V	Fig. 17, Fig 18
115V/50Hz	172V	186V	-
230V/50Hz	338V	354V	-
265V/60Hz	392V	402V	Fig. 19, Fig. 20

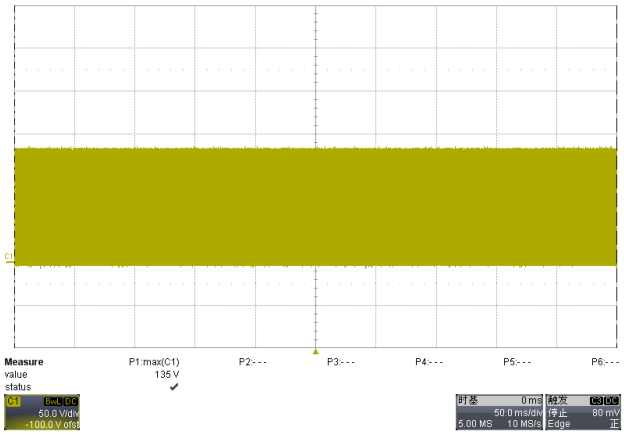

Figure 17: MOS drain-source 135V@85V/60Hz, no load

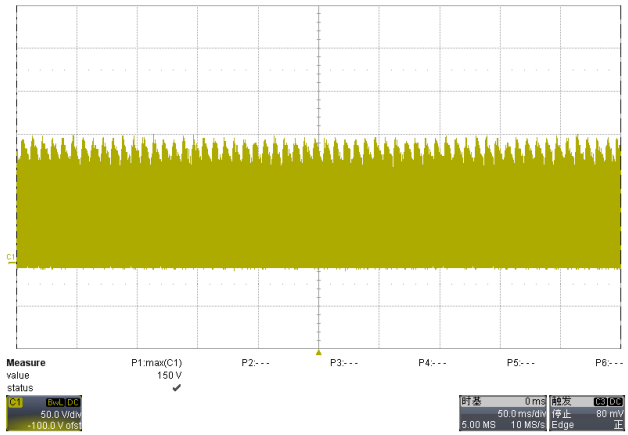

Figure 18: MOS drain-source 150V@85V/60Hz, full load

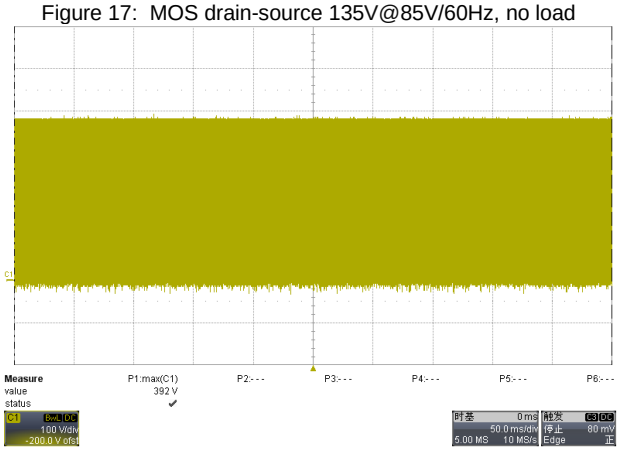

Fig. 19, MOS drain-source 392V@265V/50Hz, no load

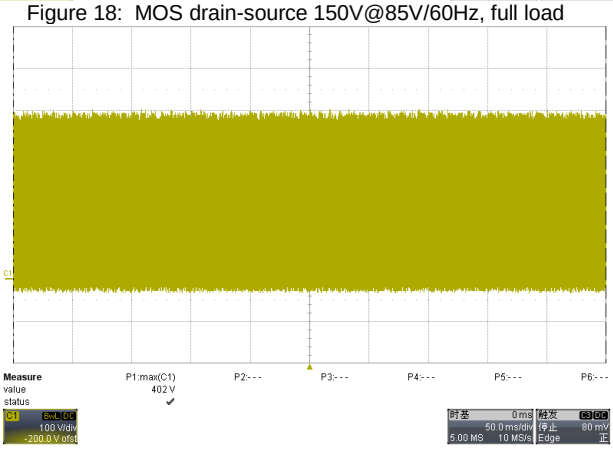

Fig. 20, MOS drain-source 402V@265V/50Hz, full load

5.2.4 Output Ripple & Noise

The dynamic response of output voltage is tested at the PCB terminal and the bandwidth is limited to 20MHz. Loading is set 0A as low load and 175mA as high load. Besides, the period is 2 seconds and the ramp is set at 250mA/us.

Table 8: Ripple & Noise

AC input voltage	Loading condition		Figures
	No load	Full load	
85V/60Hz	45mV	90mV	Fig. 21, Fig.22
115V/50Hz	45mV	86mV	-
230V/50Hz	51mV	90mV	-
265V/60Hz	51mV	126mV	Fig. 23, Fig. 24

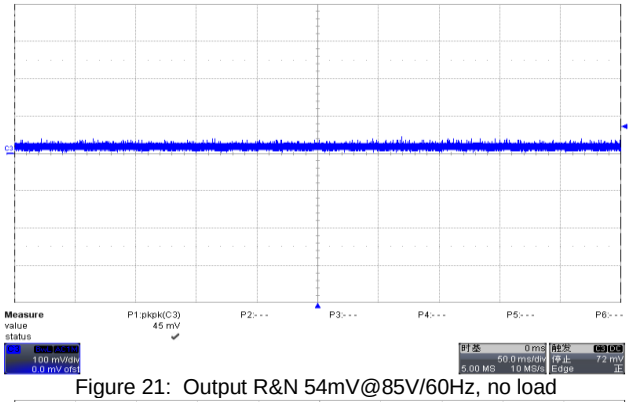

Figure 21: Output R&N 54mV@85V/60Hz, no load

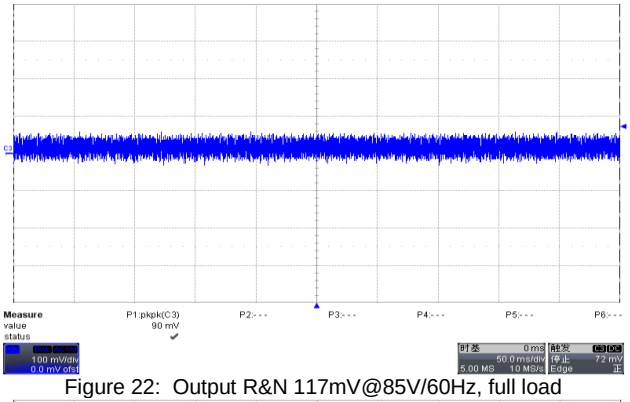

Figure 22: Output R&N 117mV@85V/60Hz, full load

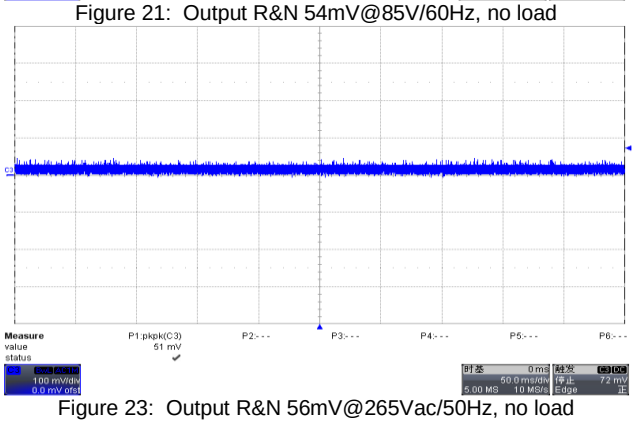

Figure 23: Output R&N 56mV@265Vac/50Hz, no load

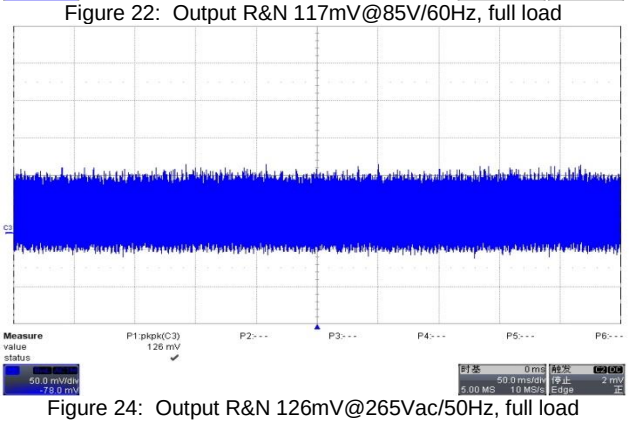

Figure 24: Output R&N 126mV@265Vac/50Hz, full load

5.2.5 Dynamic Response

The dynamic response of output voltage is tested at the PCB terminal and the bandwidth is limited to 20MHz. Loading is set 0A as low load and 120mA as high load. Besides, the period is 2 seconds and the ramp is set at 250mA/us.

Table 9: Dynamic Response

AC input voltage	Output voltage(V)			Figures
	Max Vo(V)	Min Vo(V)	Delta Vo(V)	
85V/60Hz	12.58	11.37	1.22	Fig. 25
115V/60Hz	12.58	11.30	1.09	-
230V/50Hz	12.58	11.30	1.28	-
265V/50Hz	12.58	11.24	1.34	Fig. 26

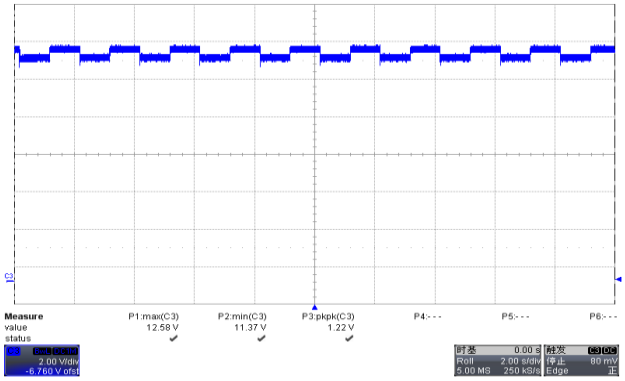

Figure 25: Vo:12.58~11.37V@0~120mA, 1s, 250mA/us, 85V/60Hz

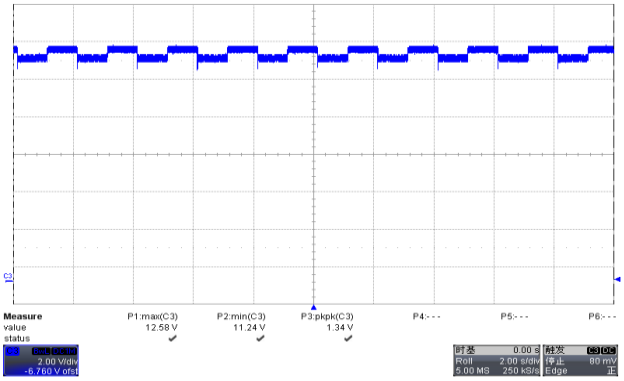

Figure 26: Vo:12.58~11.24V@0~120mA, 1s, 250mA/us, 265V/50Hz

5.3 Protection Test

5.3.1 Short Circuit Protection (SCP) Test

The SCP test is measured under the condition that output cable terminals are shorted. The resistance of output cable is 50mΩ.

Table 10: Short Circuit Protection test

AC input voltage	Max Vo (mV)	Max Io(mA)	Vds(V)	Average input power (W)	Figures
85V/60Hz	300	295	158	0.471	Fig. 27
115V/60Hz	460	378	196	0.717	-
230V/50Hz	972	685	382	0.456	-
265V/50Hz	593	448	414	0.218	Fig. 28

CH1: Vds; CH3: Vo; CH4: Io

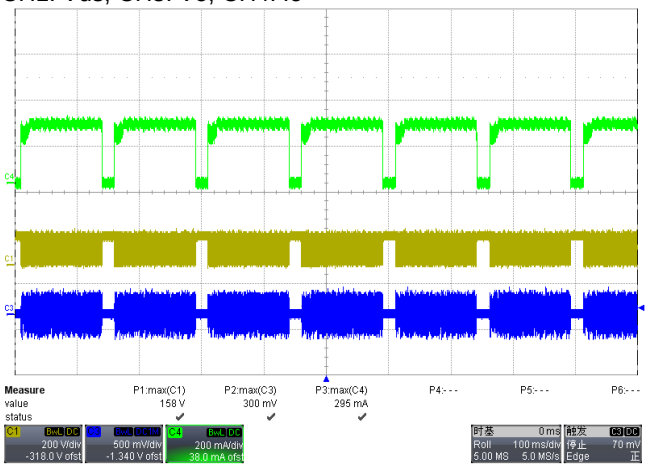

Figure 27: Output current 295mA, output voltage 300mV, Vds 158V@output short circuit, 85V/60Hz

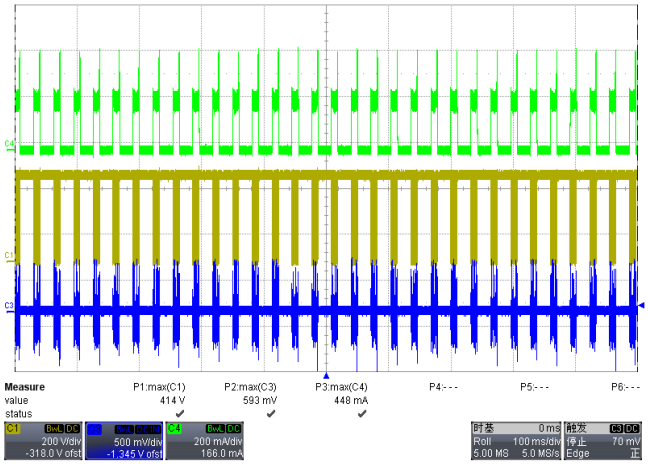

Figure 28: Output current 448mA, output voltage 593mV, Vds 414V@output short circuit, 265V/50Hz

5.3.2 Open Loop Detection (OLD) protection Test

The open loop detection protection is measured when FB pin is connected to Source pin.

Table 11: Open Loop Detection Test

AC input voltage	Output voltage(V)		Figures
	No load	Full load	
85V/60Hz	4.99	2.08	Fig. 29
115V/60Hz	5.01	2.09	(omitted)
230V/50Hz	5.05	2.11	(omitted)
265V/50Hz	5.19	2.11	Fig. 30

CH1: Vds; CH3: Vo; CH4: Io

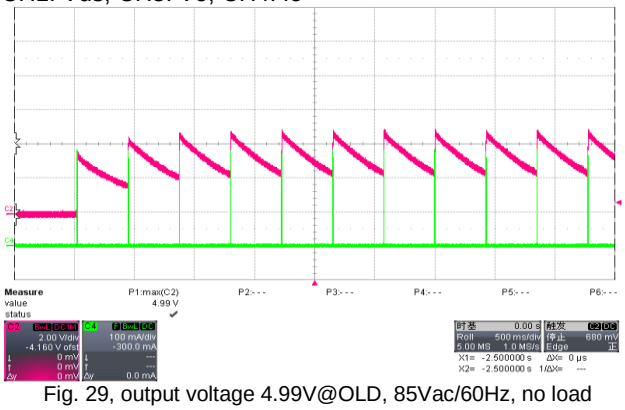

Fig. 29, output voltage 4.99V@OLD, 85Vac/60Hz, no load

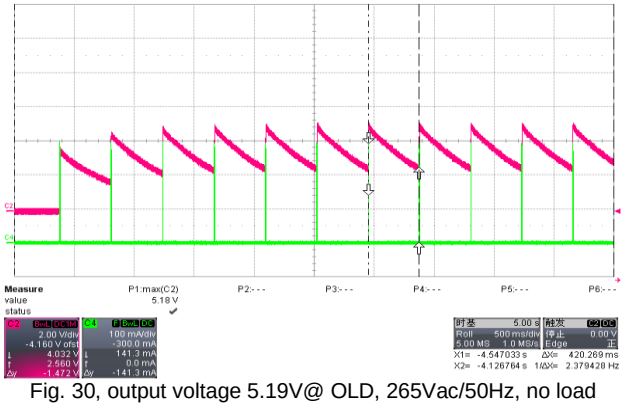

Fig. 30, output voltage 5.19V@ OLD, 265Vac/50Hz, no load

5.3.3 Over Load Protection (OLP) Test

The over load protection point is tested as below: increase the loading by 10mA/step until the system cannot maintain a stable output, and then mark the loading level as over load protection point.

Table 12: Over Load Protection point test

AC input voltage	Over load protection point(mA)
85V/60Hz	170
115V/60Hz	170
230V/50Hz	170
265V/50Hz	170

5.4 Thermal Test

The thermal test is under ambient temperature after 1-hour aging. The board has no case in open frame. Thermal imager is used to observe the surface temperature of AP3917B and the free-wheeling diode, D1.

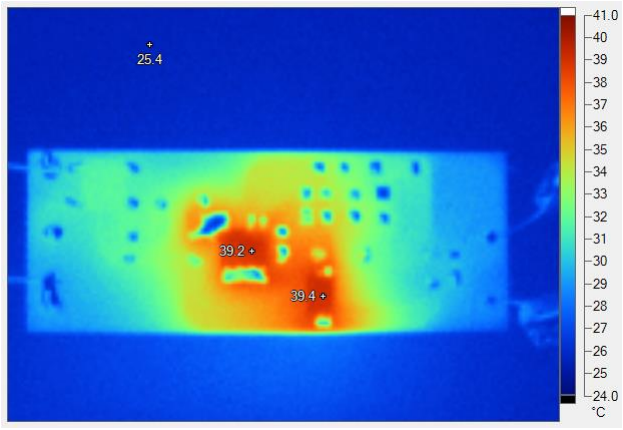

Figure 31: IC 39.2℃, free-wheeling diode 39.4℃@full load, 85V/60Hz, ambient temperature 25.4℃.

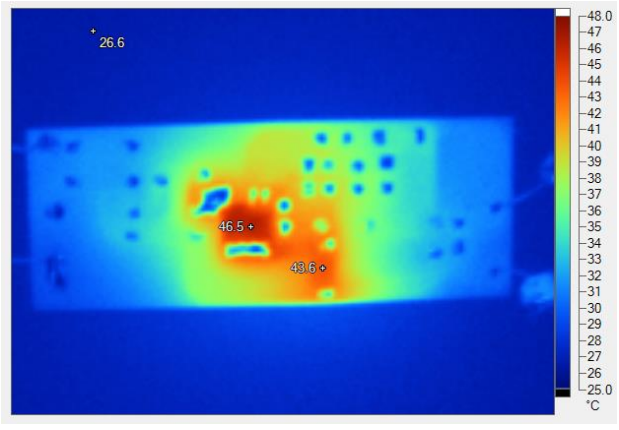

Figure 32: IC 46.5℃, free-wheeling diode 43.6℃@full load, 265V/50Hz, ambient temperature 26.6℃.

5.5 System EMI Scan

The power supply meets EN55022 Class B (for 230Vac input) and FCC part 15 (for 110Vac input) EMI requirements with more than 6dB margin.

5.5.1 Conducted EMI Test of 230V@full load

The test result can pass EN55022 Class B limit with more than 6dB margin.

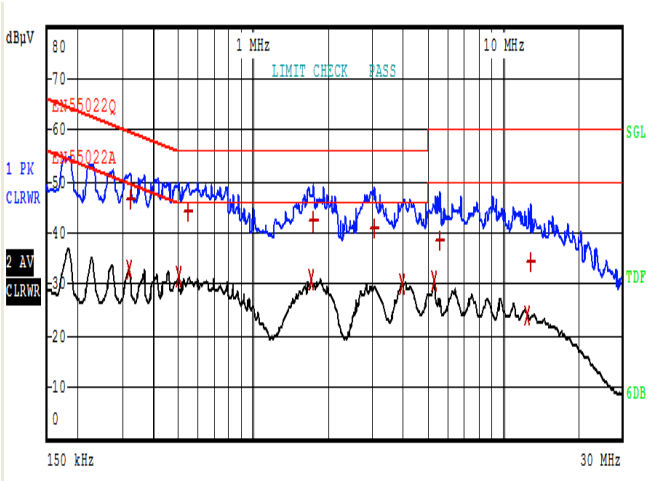

Fig. 33, L line conducted waveform@230V, full load.

EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
2	Average	319.532962956 kHz	32.82	-16.89
1	Quasi Peak	322.728292586 kHz	46.76	-12.86
2	Average	500.008614528 kHz	31.74	-14.25
1	Quasi Peak	546.852057924 kHz	43.99	-12.00
2	Average	1.7002252517 MHz	31.04	-14.95
1	Quasi Peak	1.73439977926 MHz	42.13	-13.86
1	Quasi Peak	3.02793216507 MHz	40.75	-15.24
2	Average	3.9219482581 MHz	30.21	-15.78
2	Average	5.28619370567 MHz	30.71	-19.28
1	Quasi Peak	5.55584271143 MHz	38.70	-21.29
2	Average	12.4388782936 MHz	23.88	-26.11
1	Quasi Peak	12.8157887448 MHz	34.22	-25.77

Fig. 34, L line conducted data@230V, full load.

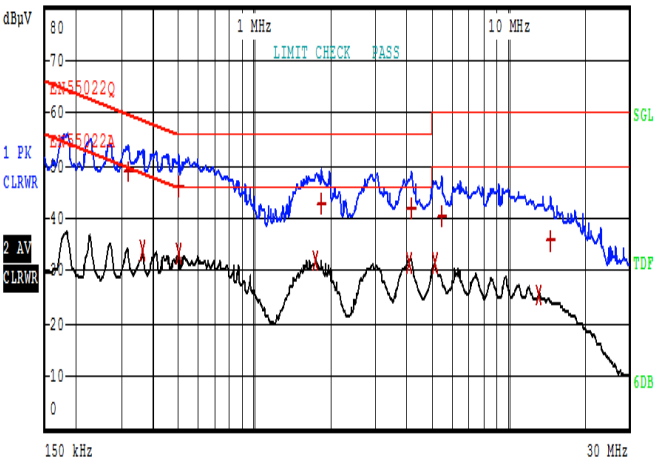

Figure 35: N line conducted waveform@230V, full load.

EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
1	Quasi Peak	319.532962956 kHz	49.10	-10.61
2	Average	360.057740611 kHz	33.75	-14.97
1	Quasi Peak	500.008614528 kHz	46.26	-9.73
2	Average	500.008614528 kHz	33.38	-12.61
2	Average	1.73439977926 MHz	31.96	-14.03
1	Quasi Peak	1.8228715989 MHz	42.77	-13.22
2	Average	4.04078721227 MHz	31.62	-14.37
1	Quasi Peak	4.12200703523 MHz	41.83	-14.16
2	Average	5.13072753076 MHz	31.48	-18.51
1	Quasi Peak	5.44637066114 MHz	40.56	-19.43
2	Average	13.2041199595 MHz	25.58	-24.41
1	Quasi Peak	14.5855630539 MHz	35.59	-24.40

Figure 36: N line conducted data@230V, full load.

5.5.2 Conducted EMI Test of 110V@full load

The test result can pass FCC part 15 limit with more than 6dB margin.

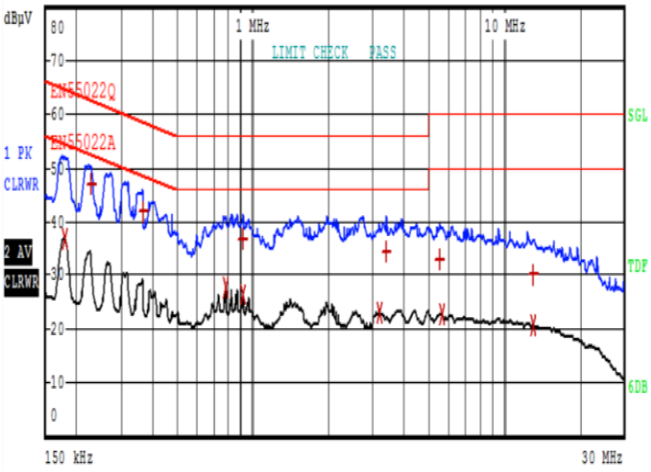

Figure 37: L line conducted waveform@110V, full load.

EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
2	Average	177.645664706 kHz	36.65	-17.93
1	Quasi Peak	227.818484195 kHz	47.10	-15.42
1	Quasi Peak	363.658318017 kHz	42.08	-16.56
2	Average	774.672132397 kHz	27.98	-18.01
1	Quasi Peak	908.363999266 kHz	36.81	-19.18
2	Average	908.363999266 kHz	26.33	-19.66
2	Average	3.18238713651 MHz	23.29	-22.70
1	Quasi Peak	3.37816807242 MHz	34.28	-21.72
1	Quasi Peak	5.50083436776 MHz	32.77	-27.22
2	Average	5.61140113855 MHz	22.63	-27.36
1	Quasi Peak	12.9439466322 MHz	30.03	-29.96
2	Average	12.9439466322 MHz	20.78	-29.21

Figure 38: L line conducted data@110V, full load.

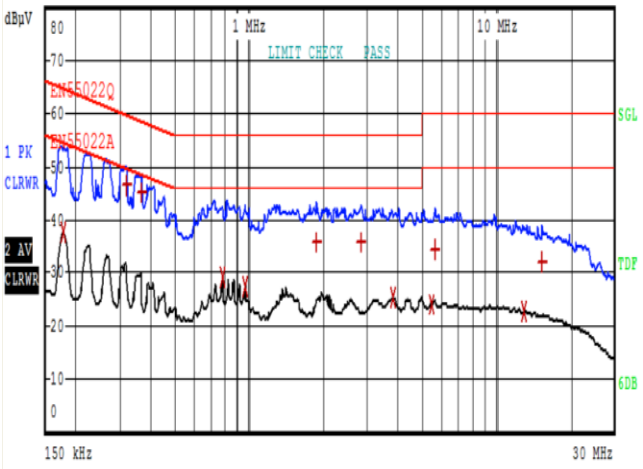

Figure 39: N line conducted waveform@110V, full load.

EDIT PEAK LIST (Final Measurement Results)

Trace1: EN55022Q
Trace2: EN55022A
Trace3: ---

TRACE		FREQUENCY	LEVEL dBµV	DELTA LIMIT dB
2	Average	175.886796739 kHz	37.46	-17.21
1	Quasi Peak	319.532962956 kHz	46.33	-13.38
1	Quasi Peak	363.658318017 kHz	45.12	-13.51
2	Average	774.672132397 kHz	29.36	-16.63
2	Average	954.699692378 kHz	27.59	-18.40
1	Quasi Peak	1.85951131803 MHz	35.94	-20.05
1	Quasi Peak	2.82420699879 MHz	35.75	-20.24
2	Average	3.80660433999 MHz	25.37	-20.63
2	Average	5.44637066114 MHz	24.27	-25.72
1	Quasi Peak	5.61140113855 MHz	34.50	-25.49
2	Average	12.8157887448 MHz	22.90	-27.09
1	Quasi Peak	15.177795402 MHz	31.97	-28.02

Figure 40: N line conducted data@110V, full load.

6. Revision control Table

Revision	Items Changed & added	The changing reason
1.0	Release	
Rev1.0 to Rev1.1	Relocated the F1 fusible resistor to L side from N	Ensure the fusible resistor protection open on Live side

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