APPLICATION NOTE 1125
SINGLE PHASE SYNCHRONOUS BUCK CONTROLLER

General Description

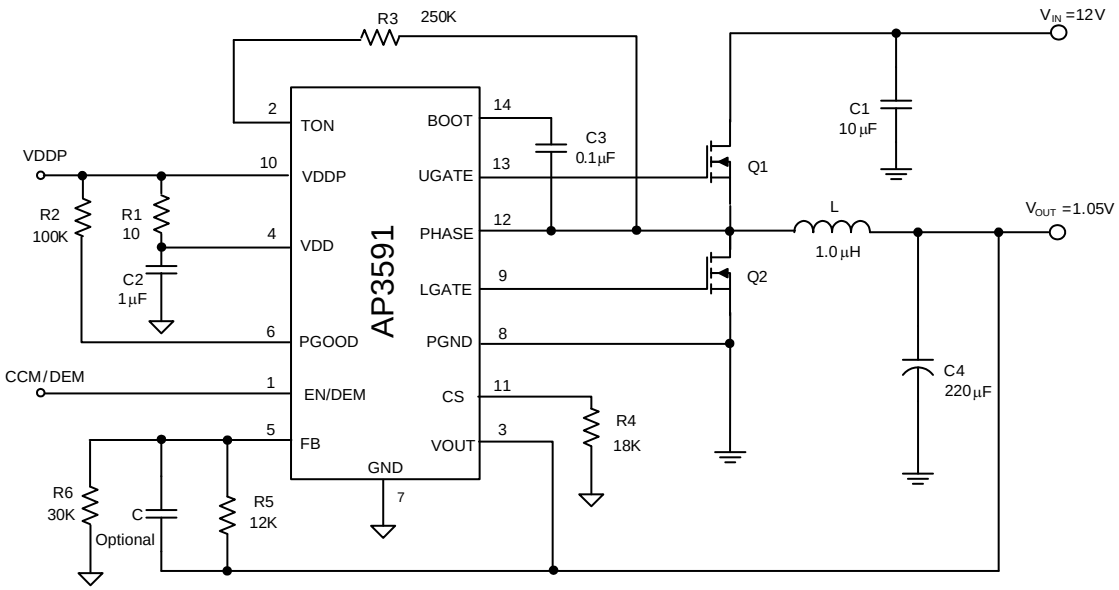
The AP3591 is a synchronous adaptive on-time buck controller providing high efficiency, excellent transient response and high DC output accuracy for low voltage regulation in notebook application.

The constant-on-time PWM control scheme handles wide input/output voltage ratios with ease and provides low external component count and fast transient response.

The operation mode is selectable by EN voltage. A Diode Emulation Mode (DEM) is activated for increasing efficiency at light loads, while PWM mode is activated only for low noise operation. The AP3591 also integrates internal Soft-start, UVLO, OVP, OTP, and programmable OCP to protect the circuit. A Power Good signal is employed to monitor output voltage.

The AP3591 is available in U-QFN3535-14 package.

EV Board Schematic



Application Information

BOM of Typical Application (V_{OUT} = 1.05V)

Symbol	Value	Description	Manufacturer	Part Number
C1	10µF/25V	ESR<4mΩ@400kHz	Murata	GRM31CR61E106KA12
C4	220µF/6.3V	ESR<9mΩ@300kHz	Sanyo	6SVPE220M
L	1.0µH	DCR<4mΩ, I_{MAX}=24A	Vishay	IHLP5050CEER1R0M01
Q1	N-MOSFET	I_{DMAX}=30A, $R_{DS(ON)}$=14mΩ	Infineon	BSC119N03S
Q2	N-MOSFET	I_{DMAX}=30A, $R_{DS(ON)}$=14mΩ	Infineon	BSC119N03S

Application Information (Cont.)

Output Voltage Set Equation

The output voltage of the AP3591 V_{OUT} is set by an external resistor divider from V_{OUT} to ground, the V_{OUT} is adjustable by changing the R1 and R2 values. The divider tap is connected to the FB pin, and the typical value of the voltage at the FB pin is 0.75V. The following equation is used to set V_{OUT}:

$$V_{OUT} = V_{FB} * (1 + \frac{R1}{R2})$$

$0.75V \le V_{OUT} \le 5.5V$, $V_{FB} = 0.75V$

For example, if output voltage of 1.05V is needed, with a chosen R2 value of 30kΩ, the value of R1 can be calculated according to the equation, so a 12kΩ resistor should be chosen for R1.

V_{OUT}	R2	R1
1.05V	30KΩ	12KΩ
1.8V	30KΩ	42KΩ
3.3V	100KΩ	340KΩ
5V	100KΩ	567KΩ

Inductor Selection

To select an inductor for use in AP3591 applications, it is worth noting that the inductor current saturation rating should be larger than the possible peak inductor current to ensure proper operation, and find a low-pass inductor having the lowest possible DC resistance that fits in the allowed dimensions. Ferrite cores are often the best choice, although powdered iron is inexpensive and can work well at 200kHz. The core must be large enough and not saturate at the peak inductor current (I_{PEAK}):

$$I_{PEA} = I_{LOAD(MAX)} + \left(\frac{L_{IR}}{2}\right) * I_{LOAD(MAX)}$$

Using an inductor, the saturation current of which is lower than required can cause a dramatic drop in the inductance and can decay the maximum output current levels severely. Larger value inductors result in lower ripple currents, and smaller value inductors result in higher ripple currents. A 1µH inductor will be the best choice for most AP3591 applications when the output voltage is 1.05V. The following equation can also help give a good approximate value for the inductor.

$$L = \frac{t_{ON} * (V_{IN} - V_{OUT})}{L_{IR} * I_{LOAD(MAX)}}$$

t_{ON}: On-time, the value is about 300ns to 500ns, t_{ON} = 14.5p x R_{TON} x (V_{OUT} + 0.1) / V_{IN} + 50ns;

L_{IR}: The ratio of the peak-to-peak ripple current to the maximum average inductor current.

Output and Input Capacitor Selection

Input Capacitor

At least a 10µF input capacitor is recommended to reduce the input ripple and switching noise for normal operating conditions, while a 10µF to 22µF capacitor may be required for higher power and dynamic loads. Larger values and lower ESR (Equivalent Series Resistance) may be needed if the application requires very low input ripple. It follows that the ceramic capacitors are good choices for applications. Note that the input capacitor should be located as close as possible to the IC.

Output Capacitor

The output filter capacitor must have low enough ESR to meet output ripple and load-transient requirement, yet have high enough ESR to satisfy stability requirements. Also, the output capacitance value must be high enough to absorb the inductor energy going from a full-load to no-load condition without tripping the OVP circuit.

Application Information (Cont.)

For CPU core voltage converters and other applications where the output is subject to violent load transient, the output capacitor's size depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$ESR \leq \frac{V_{PP}}{I_{LOAD(MAX)}}$$

In non-CPU applications, the output capacitor's size depends on how much ESR is needed to maintain at an acceptable level of output voltage ripple:

$$ESR \leq \frac{V_{PP}}{L_{IR} * I_{LOAD(MAX)}}$$

Organic semiconductor capacitor(s) or specially polymer capacitor(s) are recommended.

Output Capacitor Stability

Stability is determined by the value of the ESR zero relative to the switching frequency. The point of instability is given by the following equation:

$$f_{ESR} = \frac{1}{2 * \pi * ESR * C_{OUT}} \leq \frac{f_{SW}}{4}$$

Do not put high value ceramic capacitors directly across the outputs without taking precautions to ensure stability. Large ceramic capacitors can have a high ESR zero frequency and cause erratic and unstable operation. However, it is easy to add sufficient series resistance by placing the capacitors a couple of inches downstream from the inductor and connecting V_{OUT} or FB divider close to the inductor. There are two related but distinct ways including double-pulsing and feedback loop instability to identify the unstable operation. Double-pulsing occurs due to noise on the output or because the ESR is so low that there is not enough voltage ramp in the output voltage signal. This "fools" the error comparator into triggering a new cycle immediately after a 400ns minimum off-time period has expired. Double-pulsing is more annoying than harmful, resulting in nothing worse than increased output ripple. However, it may indicate the possible presence of loop instability, which is caused by insufficient ESR. Loop instability can result in oscillation at the output after line or load perturbations that can trip the over voltage protection latch or cause the output voltage fall below the tolerance limit. The easiest method for stability checking is to apply a very zero-to-max load transient and carefully observe the output-voltage-ripple envelope for overshoot and ringing. It helps to simultaneously monitor the inductor current with AC probe. Do not allow more than one ringing cycle after the initial step-response under-or over-shoot.

MOSFET Selection

The AP3591 requires two N-Channel power MOSFETs, these should be selected based upon $R_{DS(ON)}$, gate supply requirements and thermal management requirements.

In high current applications, the MOSFET power dissipation, package selection, and heatsink are the dominant design factors. The power dissipation includes two loss components: conduction loss and switching loss.

The conduction losses are the largest component of power dissipation for the high-side and the low-side MOSFET. These losses are distributed between the two MOSFETs according to duty factor (see the equations below). Only the high-side MOSFET has switching losses since the low-side MOSFETs body diode or an external Schottky rectifier across the lower MOSFET clamps the switching node before the synchronous rectifier turns on. These equations assume linear voltage current transitions and do not adequately model power loss due to the reverse-recovery of the low-side MOSFET body diode. The gate-charge losses are dissipated by AP3591 and don't heat the MOSFETs. However, large gate-charge increases the switching interval t_{SW}, which increases the high-side MOSFET switching losses. Ensure that all MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal resistance specifications. A separate heatsink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

For the high-side and low-side MOSFETs, the losses are approximately given by the following equations:

$$P_{HIGH-SIDE} = I_{OUT}^2 * (1 + T_C) * R_{DS(ON)} * D + 0.5 * I_{OUT} * V_{IN} * t_{SW} * f_{SW}$$

$$P_{LOW-SIDE} = I_{OUT}^2 * (1 + T_C) * R_{DS(ON)} * (1 - D)$$

Application Information (Cont.)

Where I_{OUT} is the load current, T_C is the temperature dependency of $R_{DS(ON)}$, f_{SW} is the switching frequency, t_{SW} is the switching interval, D is the duty cycle.

Note that both MOSFETs have conduction losses while the high-side MOSFET includes an additional transition loss. The switching interval, t_{SW}, is the function of the reverse transfer capacitance C_{RSS}. The $(1+T_C)$ term is a factor in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "$R_{DS(ON)}$ vs. Temperature" curve of the power MOSFET.

Thermal Considerations

For continuous operation, do not exceed absolute maximum operation junction temperature. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following equation:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

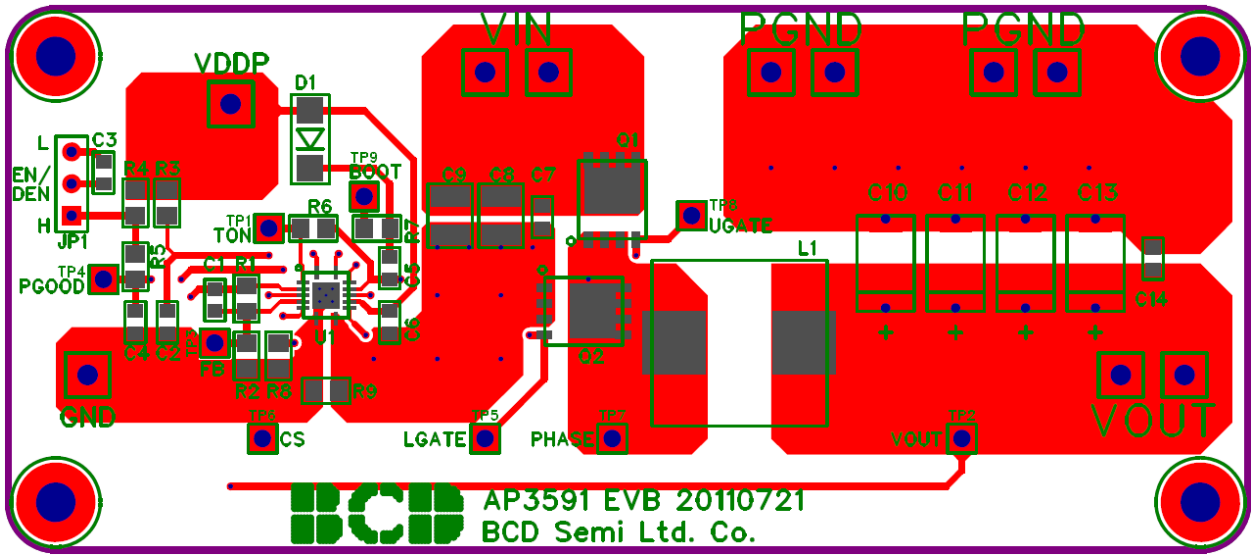
Where $T_{J(MAX)}$ is the maximum operation junction temperature +125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

PCB Layout Guidance

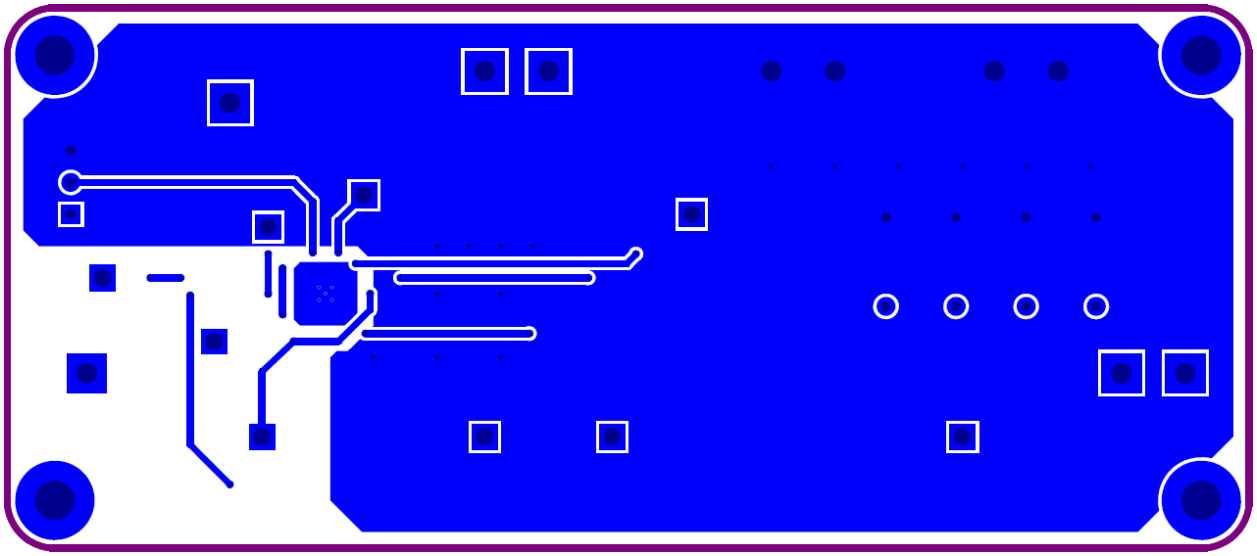
Layout is very important in high frequency switching converter design. If the layout is designed improperly, the PCB could radiate excessive noise and contribute to the converter instability. The following points must be followed for a proper layout of AP3591.

1. Connect an RC low-pass filter from VDDP to VDD, 1μF and 10Ω are recommended. Place the filter capacitor close to the IC.
2. Keep current limit setting network as close as possible to the IC. Routing of the network should avoid coupling to high voltage switching node.
3. Connections from the drivers to the respective gate of the high side or the low side MOSFET should be as short as possible to reduce stray inductance.
4. Place the source of the high-side MOSFET and the drain of the low-side MOSFET as close as possible. Minimizing the impedance with wide layout plane between the two pads reduces the voltage bounce of the node. In addition, the large layout plane between the drain of the MOSFETs (VIN and PHASE node) can get better heat sinking.
5. All sensitive analog traces and components such as VOUT, FB, GND, EN/DEM, PGOOD, CS, VDD, and TON should be placed away from high voltage switching nodes such as PHASE, LGATE, UGATE, or BOOT nodes to avoid coupling. Use internal layer(s) as ground plane(s) and shield the feedback trace from power traces and components.
6. Current sense connections must always be made using Kelvin connections to ensure an accurate signal, with the current limit resistor located at the device.
7. Power sections should connect directly to ground plane(s) using multiple vias as required for current handling (including the chip power ground connections). Power components should be placed to minimize loops and reduce losses.

PCB Layout Example



Top Layer



Bottom Layer

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