Application Notes for AP3765A System Solution

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1. Introduction

The AP3765A uses Pulse Frequency Modulation (PFM) method to realize Discontinuous Conduction Mode (DCM) operation for Flyback power supplies. The operating principle of PFM is different with Pulse Width Modulation (PWM), so the design of transformer is also different.

The AP3765A can provide accurate constant voltage (CV), constant current (CC) regulation with Primary Side Regulation (PSR) structure. It uses internal line compensation and cable compensation to reduce the number of external system components. Fixed cable compensation (6%) is used to adapt the voltage drop on output cable and good CV regulation is achieved. Besides, audio noise is reduced by the creative audio suppression technique.

The AP3765A is designed for driving bipolar transistor in Flyback converter, with more driving current of about 40mA. With system parameters properly designed, AP3765A can achieve standby power less than 150mW.

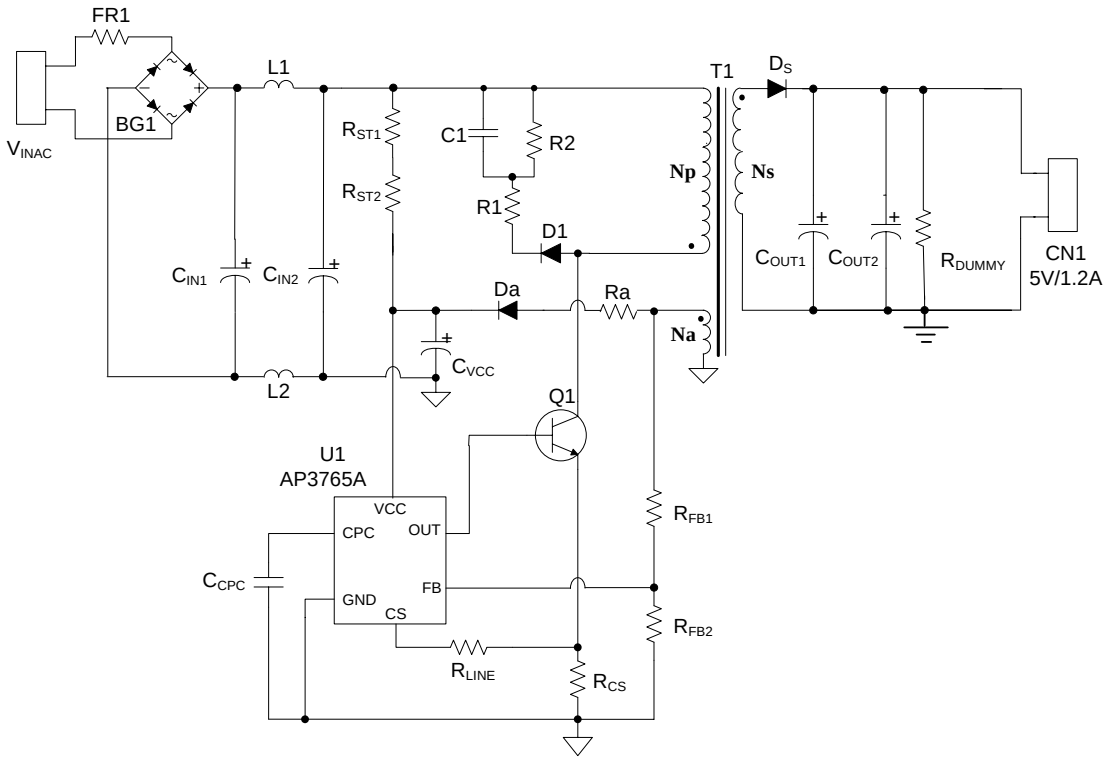

Figure 1. Typical Application Circuit of AP3765A

Figure 1 is the typical application circuit of AP3765A, which is a conventional Flyback converter with a 3-winding transformer---primary winding (N_P), secondary winding (N_S) and auxiliary winding (N_A). The auxiliary winding is used for providing V_{CC} supply voltage for IC and sensing the output voltage feedback signal to FB pin.

Figure 2 shows the typical waveforms which demonstrate the basic operating principle of AP3765A application. And the parameters are defined as following.

V_{dri}---The driving signal of primary power switch
I_p---The primary side current
I_s ---The secondary side current
I_{PK}---Peak value of primary side current
I_{PKS}---Peak value of secondary side current
V_{SEC}---The transient voltage at secondary winding
V_S---The stable voltage at secondary winding when

rectification diode is in conducting status, which equals the sum of output voltage V_{OUT} and the forward voltage drop of diode

V_{AUX}---The transient voltage at auxiliary winding

V_A--- The stable voltage at auxiliary winding when rectification diode is in conducting status, which equals the sum of voltage V_{CC} and the forward voltage drop of auxiliary diode

t_{SW} ---The period of switching frequency

t_{ONP} ---The conduction time when primary side switch is "ON"

t_{ONS} ---The conduction time when secondary side diode is "ON"

t_{OFF} ---The dead time when neither primary side switch nor secondary side diode is "ON"

t_{OFFS} --- The time when secondary side diode is "OFF"

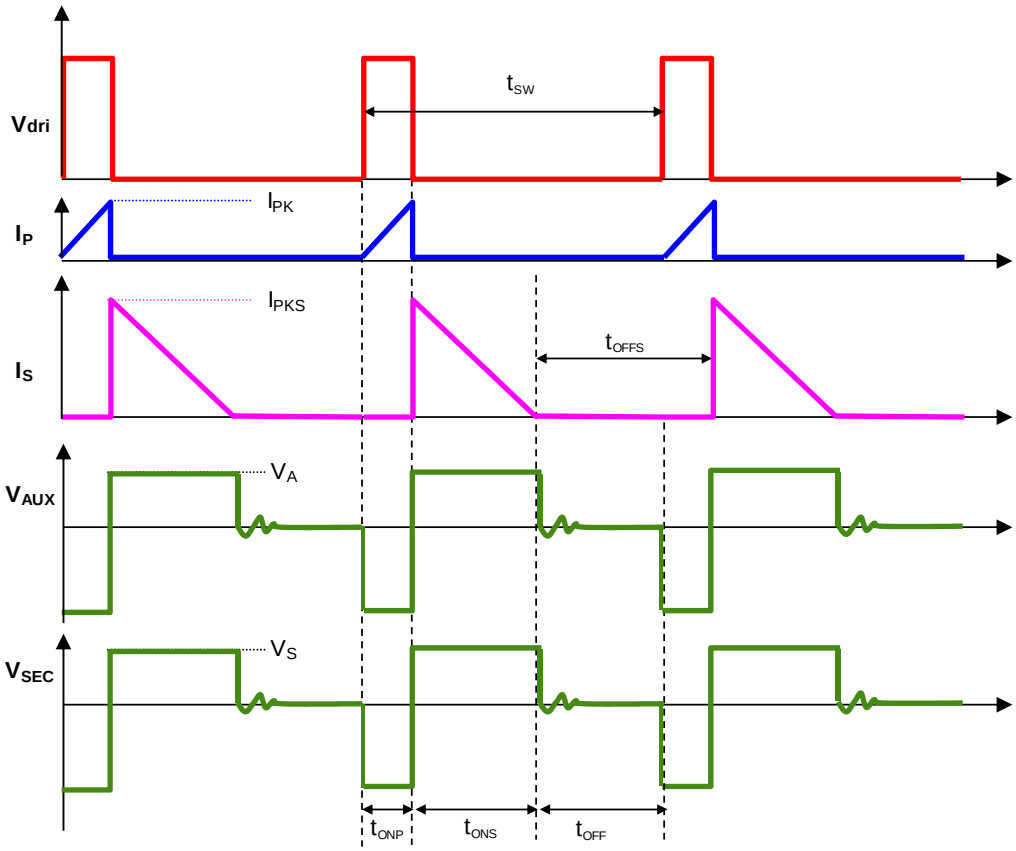

Figure 2. Operation Waveforms of Flyback PSR Control System

2. Guideline of System Design

1. Low Standby Power Design
2. Switching Frequency Design
3. Transformer and Power Devices Design
4. Feedback Resistors Design
5. Line Compensation Design

2.1 Low Standby Power Design

In order to achieve low standby power, AP3765A decreases the minimum operating voltage. And the startup resistors R_{ST1}+R_{ST2} should be high enough to further lower the power loss. However, there is a tradeoff between low standby power P_{ST} and small startup time t_{START}, which is

$$t_{START} = (R_{ST1} + R_{ST2}) \cdot C_{vcc} \cdot V_{TH\_ST} / V_{INDC\_MIN} \quad (1)$$

Where V_{TH_ST} is the Startup Threshold of V_{CC}, and V_{INDC_MIN} is the rectified DC voltage from the lowest AC input.

Besides, the selection of dummy load resistor is a tradeoff between standby power and I-V curve. The recommended value of dummy load resistor R_{DUMMY} is 4.7kΩ to 10kΩ for an application with 5V output voltage.

2.2 Switching Frequency Design

As we know, in DCM Flyback converter, the stored energy of primary side will be transferred to secondary side at the time when the primary switch is turned off. And assume the current transfer efficiency from primary to secondary is η_i, then

$$Ipks = Ipk \cdot N_{PS} \cdot \eta_i \tag{2}$$

Here, N_{PS} is the turn ratio of primary winding to secondary winding.

It is obvious in Figure 2 that the output current "I_O" is the average current of secondary side "I_S",

$$Io = \frac{1}{2} Ipks \cdot \frac{t_{ONS}}{t_{SW}} \tag{3}$$

Then,

$$Io = \frac{1}{2} Ipk \cdot N_{PS} \cdot \eta_i \cdot \frac{t_{ONS}}{t_{SW}} \tag{4}$$

Always voltage of CPC pin (V_{CPC}) is determined by,

$$Vcpc = VDD \cdot \frac{t_{ONS}}{t_{SW}} \tag{5}$$

Here VDD is a constant voltage generated by IC. Then,

$$\frac{Vcpc}{I_O} = \frac{2 \cdot VDD}{N_{PS} \cdot \eta_i \cdot I_{PK}} \tag{6}$$

If η_T is efficiency of power transmission from transformer primary to the output, then

$$P_O = V_O \cdot I_O = \frac{1}{2} \cdot L_P \cdot I_{pk}^{\ 2} \cdot f_{SW} \cdot \eta_T \tag{7}$$

Where, f_{SW} is the switching frequency. So,

$$\frac{f_{SW}}{I_O} = \frac{2 \cdot V_O}{L_P \cdot I_{pk}^{\ 2} \cdot \eta_T} \tag{8}$$

When voltage at the sense resistor reaches the reference voltage set by AP3765A, the switch will be turned off and primary current reaches its maximum value,

$$I_{PK} = \frac{V_{cs\_ref}}{R_{cs}} \tag{9}$$

When the constant reference V_{CS_REF} is used, the peak current I_{PK} is constant. From formula (6) and (8), it is obvious that V_{CPC} and f_{SW} increases linearly with the output current I_O.

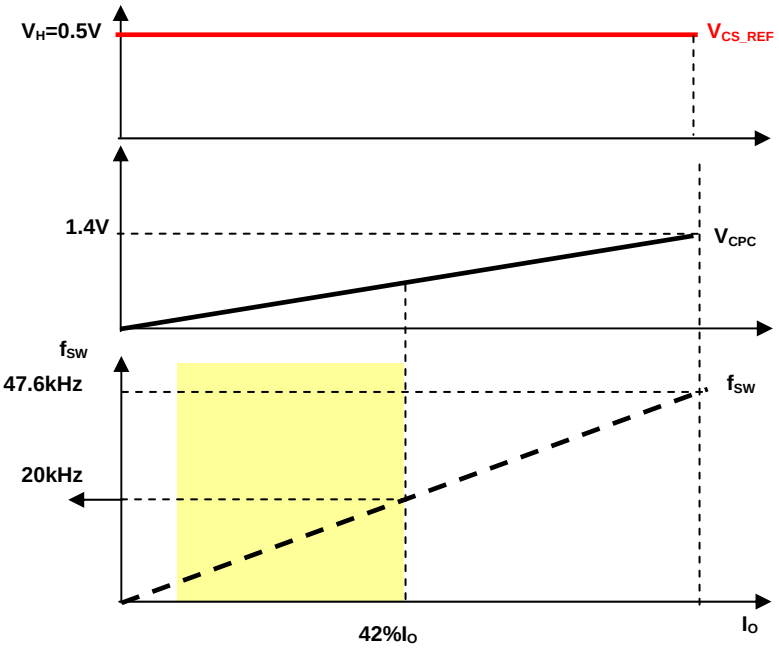

Figure 3. Relationship Between V_{CPC}, f_{SW} and I_O at Constant Peak Current Mode

In AP3765A, in order to realize audio noise suppression, two-segmented of current reference voltage V_{CS_REF} is used. The reference is about 0.5V when I_O>=42%*I_{O_MAX} and is decreased to 0.5V/1.5 when I_O<42%* I_{O_MAX}, as follows in Figure 4.

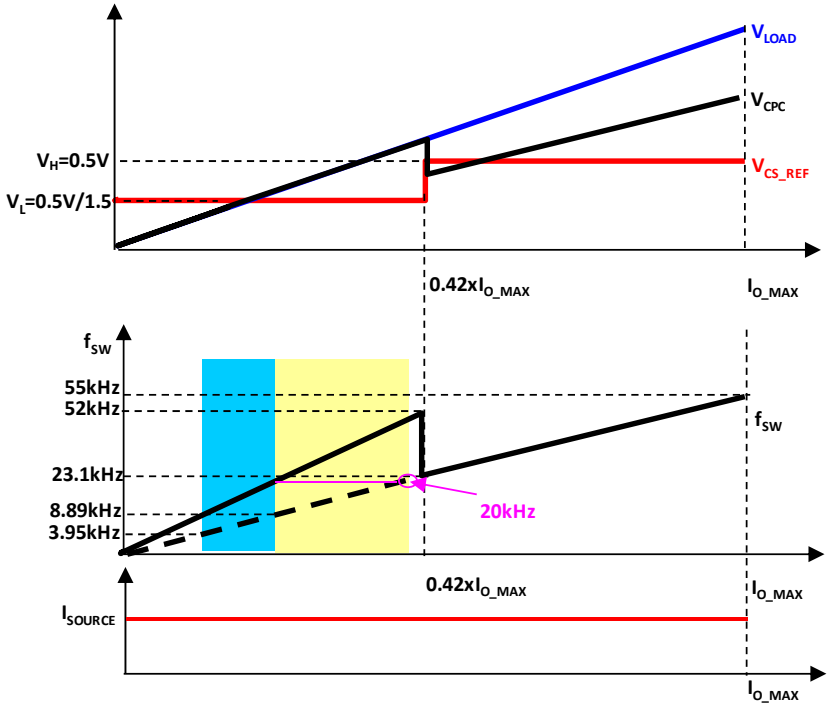

Figure 4. Relationship Between V_{CPC}, f_{SW} and I_O at Variable Peak Current Mode

Then from formula (6) and (8), we can see the V_{CPC} and f_{SW} both has a leap at about 42% of maximum load. At the leap point, if the peak current is decreased by 1.5 times, the voltage of CPC pin at low I_{PK} will be increased to 1.5 times, and the switching frequency f_{SW} at low I_{PK} will be increased to 1.5^2 times. So the load range in audio is largely narrowed.

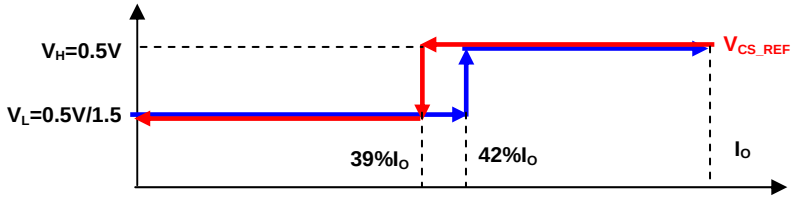

Figure 5. Hysteresis at Conversion Between Low I_{PK} and High I_{PK}

In order to avoid unstable operation, a hysteresis is added at the conversion between low I_{PK} and high I_{PK}. Considering the relationship between audio noise and flux density of transformer, deltaB≤2500 gauss is better for audio noise suppression.

The low limitation of maximum switching frequency is given by audio noise suppression. And the upper limit of the AP3765A can be up to 120kHz. But this is only the limit of the IC; the finally designed maximum switching frequency is determined by the tradeoff between the efficiency, mechanical dimensions and thermal performance.

2.3 Transformer and Power Devices Design

In the design of AP3765A, constant current control function will keep a fixed proportion between on-time t_{ONS} and off-time t_{OFFS} of rectifier D1 (in Figure 1) by discharging or charging a capacitor embedded in the IC. The fixed proportion is

$$\frac{t_{ONS}}{t_{SW}} = \frac{1}{2} \tag{10}$$

It is assumed

$$k = \frac{2 \cdot t_{SW}}{t_{ONS}} = 4 \tag{11}$$

Then the output constant-current value I_O is

$$I_O = \frac{1}{k} \cdot I_{PKS} = \frac{1}{k} \cdot N_{PS} \cdot \eta_i \cdot I_{PK} \tag{12}$$

2.3.1 Calculate Turn Ratio of Transformer (N_{PS})

The turn ratio of transformer should be designed first, which ensures the power converter operating in DCM within the whole conditions,

$$t_{SW} \geq t_{ONP} + t_{ONS} \tag{13}$$

As we know, if equation (13) is met at minimum input voltage and full load, it can ensure that the power converter operates in DCM in all conditions.

For the primary side current,

$$t_{ONP} = I_{pk} \cdot \frac{L_p}{V_{indc}} \tag{14}$$

Where
LP is the inductance of primary winding.
V_{indc} is the rectified DC voltage of input.
When V_{indc} is the minimum value, the maximum t_{ONP} can be obtained. So,

$$t_{ONP\_MAX} = I_{pk} \cdot \frac{L_p}{V_{indc\_min}} \tag{15}$$

For the secondary side current, L_S is the inductance of secondary winding, V_d is the forward voltage of secondary diode.

There is an oscillating signal on FB waveform after secondary Schottky diode current decrease to zero, which is caused by primary inductance and equivalent output capacitance of primary switch. Then some margin is added to t_{ONS} as

$$t_{ONS} = I_{pks} \cdot \frac{L_S}{V_S} \cdot 1.1 \tag{16}$$

$$V_S = V_O + V_d \tag{17}$$

From formula (4) and formula (16), we can get

$$Vs \cdot Io = \frac{1}{2} \cdot Ls \cdot Ipks^2 \cdot fsw = \frac{1}{2} \cdot \frac{Lp}{N_{PS}^2} \cdot (Ipk \cdot N_{PS} \cdot \eta i)^2 \cdot fsw = \frac{1}{2} \cdot Lp \cdot Ipk^2 \cdot fsw \cdot \eta i^2 \tag{18}$$

Then,

$$t_{SW} = \frac{L_p \cdot I_{pk}^2 \cdot \eta_i^2}{2 \cdot V_S \cdot I_O} \tag{19}$$

t_{ONP} , t_{ONS} and t_{SW} in (13) are replaced with (15), (16) and (19), then

$$\frac{L_p \cdot I_{pk}^2 \cdot \eta_i^2}{2 \cdot V_S \cdot I_O} \geq I_{pks} \cdot \frac{L_s}{V_s} \cdot 1.1 + I_{pk} \cdot \frac{L_p}{V_{indc\_min}} \tag{20}$$

Relationship between inductance of primary side and secondary side is,

$$L_s = \frac{L_p}{N_{PS}^2} \tag{21}$$

At full load, the system will work in the boundary of CC regulation. I_O can be given by formula (12)，the following can be obtained,

$$N_{PS} \leq N_{PS\_MAX} = \frac{V_{indc\_min} \cdot \eta_i}{V_S} \cdot (\frac{k}{2} - 1.1) \tag{22}$$

Then designed turns ratio N_{PS} should be no more than N_{PS_MAX} defined in formula (22).

2.3.2 Check Stress Voltage of Primary Side Switch and Reverse Voltage of Secondary Diode

If N_{PS} is fixed by customer according to design step 2.3.1, real stress voltage of primary side switch and reverse voltage of secondary diode can be calculated.

The maximum stress voltage of primary side switch is,

$$V_{ds\_switch} = V_{dc\_spike} + V_{indc\_max} + \frac{V_S \cdot N_P}{N_S} \quad (23)$$

Be careful that the value of V_{dc_spike} is determined by the snubber circuit design.

Maximum reverse voltage of secondary side ,

$$V_{dr} = V_S + \frac{V_{indc\_max} \cdot N_S}{N_P} \quad (24)$$

For Flyback converter design, higher turns ratio N_{PS} brings higher stress voltage of primary side switch, higher transforming efficiency, and the lower reverse voltage of secondary diode. Finally, in design of turns ratio N_{PS}, formula (22), (23) and (24) should be totally considered.

2.3.3 Calculate the Peak Current of Primary Side and Current Sensed Resistor (I_{PK} & R_{CS})

I_{PK} can be calculated by the output current.

$$I_{pk} = \frac{k \cdot I_O}{N_{PS} \cdot \eta_i} \quad (25)$$

In AP3765A, 0.5V is an internal reference voltage. If the sensed voltage V_{CS_REF} reaches 0.5V, the power switch will shut down and t_{ONP} will be ended.

So R_{CS} can be obtained by formula (9) and selected with a real value from the standard resistor series. We recommended using 1% tolerance resistors for R_{CS}. After R_{CS} is selected, I_{PK} should be modified based on the selected R_{CS}.

2.3.4 Calculate the Inductance of Primary Side---L_P

The primary side inductance L_P is relative with the stored energy. L_P should be big enough to store enough energy, so that P_{O_MAX} can be obtained from this system.

According to formula (18), the output power can be given by,

$$P_S = V_S \cdot I_O = \frac{1}{2} \cdot L_p \cdot I_{pk}^2 \cdot f_{SW} \cdot \eta_i^2 \quad (26)$$

Where, f_{SW} was set by the user based on definite requirement. Then, L_P can be gotten by,

$$L_P = \frac{2 \cdot P_S}{I_{PK}^2 \cdot f_{SW}} \cdot \frac{1}{\eta_i^2} \quad (27)$$

2.3.5 Calculate the Turns of Primary, Secondary and Auxiliary (N_P, N_S, N_A)

The turns of primary winding,

$$N_p = \frac{L_P \cdot I_{PK}}{Ae \cdot \Delta B} \geq \frac{L_P \cdot I_{PK}}{Ae \cdot B\max} \quad (28)$$

As N_{PS} and N_P are fixed, we can get N_S by

$$N_S = \frac{N_P}{N_{PS}} \quad (29)$$

Turns of auxiliary winding is,

$$N_A = \frac{N_S \cdot V_A}{V_S} \quad (30)$$

2.3.6 Check the Maximum Duty Cycle of Primary Side

After turn ratio of primary side and secondary side is designed, the maximum duty cycle of primary side at low line voltage can be calculated again.

Considering the Volt-second balance between magnetizing and de-magnetizing, the formula of duty cycle is

$$D_{max} = \frac{(V_O + V_d) \cdot N_{PS}}{V_{indc} \cdot \eta_i} \cdot \frac{t_{ons}}{t_{sw}} \quad (31)$$

2.3.7 Check Reverse Voltage of Auxiliary Diode

If N_P and N_A is fixed according to design step 2.3.5, real reverse voltage of auxiliary diode can be calculated by formula (32).

$$V_{dar} = V_A + \frac{V_{indc\_max} \cdot N_A}{N_P} \quad (32)$$

2.4 Feedback Resistors Design

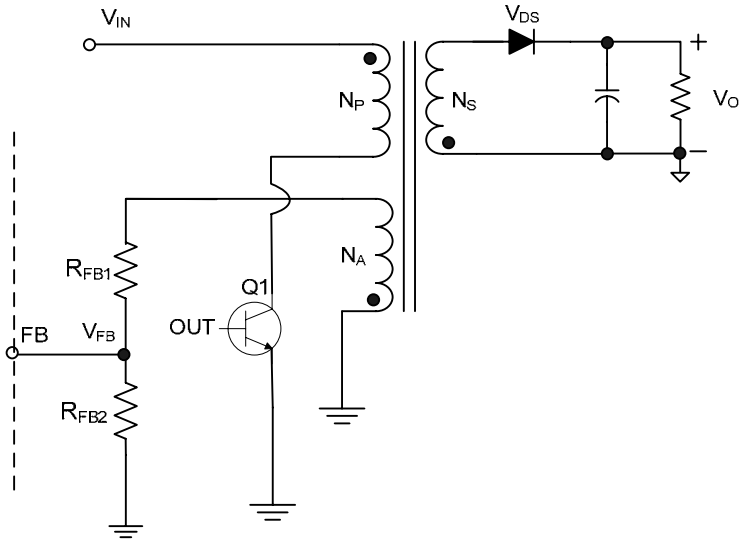

Figure 6. Feedback Resistors Circuit

From above Figure 6,

$$V_o = V_{FB} \cdot \frac{(R_{FB1} + R_{FB2})}{R_{FB2}} \cdot \frac{N_S}{N_A} - V_D \quad (33)$$

$$\frac{R_{FB1}}{R_{FB2}} = \frac{V_o + V_D}{N_S \cdot V_{FB}} \cdot N_A - 1 \quad (34)$$

Through adjusting R_{FB1} and R_{FB2}, a suitable output voltage can be achieved. The recommended values of R_{FB1} and R_{FB2} are within 5kΩ to 100kΩ.

2.5 Line Compensation Design

The internal line compensation function in AP3765A is shown in Figure 7. S1 is closed when the primary switch is "ON". The line voltage can be detected from the FB pin. The detected voltage internally compensates the peak current. So the line compensation is determined by R_{LINE}. In different applications, the value of R_{LINE} is different.

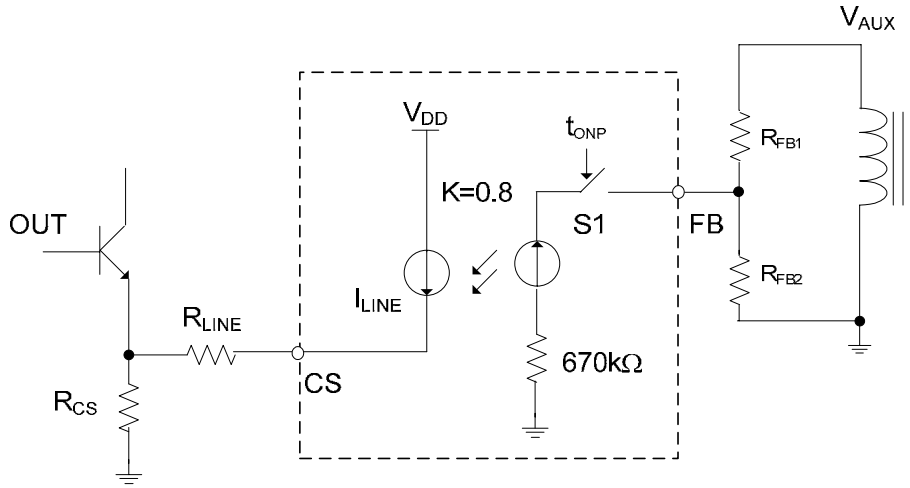

Figure 7. Line Compensation Circuit

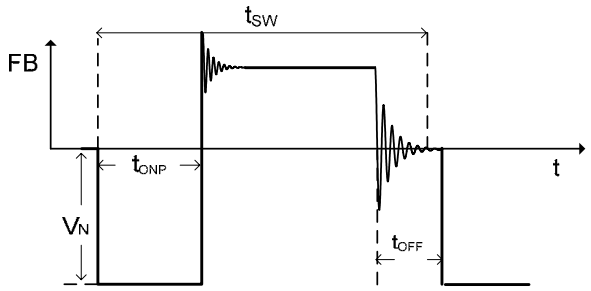

Figure 8. Waveform of FB Pin

The negative voltage V_N of FB pin (in Figure 8) is linear to line voltage. The AP3765A samples V_N to realize the line compensation.

$$V_N = V_{indc} \cdot \frac{N_A}{N_P} \cdot \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \tag{35}$$

The compensated voltage of line compensation (V_{CS_LINE}) can be calculated by the following formula,

$$V_{CS\_LINE} = V_N \cdot \frac{1}{670k} \cdot 0.8 \cdot R_{LINE} \tag{36}$$

This is designed to compensate the additional voltage of V_{CS} introduced by t_{delay}, which is the delay time of internal drivers of IC and primary side switch.

$$V_{delta} = V_{indc} \cdot \frac{t_{delay}}{L_P} \cdot R_{cs} \tag{37}$$

Then R_{LINE} can be adjusted to achieve excellent line regulation of output current.

$$R_{LINE} = \left(\frac{t_{delay}}{Lp} \cdot R_{cs}\right) / \left(\frac{N_A}{N_P} \cdot \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \cdot \frac{0.8}{670k}\right) \tag{38}$$

Design Example (for 5V/1.2A application):

Specification:
Input voltage: $85V_{AC}$ to $265V_{AC}$
Output voltage @ cable: V_{O_CABLE}=5V
Output current: I_O=1.2A
Output voltage @ PCB: V_O=5.13V, (AWG22 Cable, Length of cable=100cm)

Other setting by users:
Switching frequency: f_{SW}=65kHz
Forward voltage of secondary diode: V_d=0.4V
Forward voltage of auxiliary diode: V_{da}=1.1V
V_{CC} voltage: V_{CC}=14V
Core_type: RM5 (Ae=23.7mm^2), Bmax<3000GS
V_{dc_spike}=50V (with snubber circuit)

Design Steps:

1) Calculate turn ratio of transformer (N_{PS})

$$N_{PS} \le N_{PS\_MAX} = \frac{V_{indc\_min} \cdot \eta_i}{V_S} \cdot \left(\frac{k}{2} - 1.1\right) = 15.8 \tag{39}$$

$$V_{indc\_min} = V_{inac\_min} \cdot \sqrt{2} - 40 \tag{40}$$

Considering some margin for Flyback PSR control, we choose N_{PS}=15.5.

2) Check stress voltage of primary side switch and reverse voltage of secondary diode

According to formulas (23) (24) and the selected N_{PS}, proper power devices could be chosen.

$$V_{ds\_switch} = V_{dc\_spike} + V_{indc\_max} + \frac{V_S \cdot N_P}{N_S} = 510V < 700V \tag{41}$$

$$V_{dr} = V_S + \frac{V_{indc\_max} \cdot N_S}{N_P} = 29V < 40V \tag{42}$$

3) Calculate the peak current of primary side and current sense resistor (I_{PK} & R_{CS})

$$I_{pk} = \frac{I_{pks}}{N_{PS} \cdot \eta_i} = \frac{k \cdot I_O}{N_{PS} \cdot \eta_i} = 330mA \tag{43}$$

$$R_{CS}=\frac{V_{CS}}{I_{pk}}=1.5\,\Omega \quad (44)$$

4) Calculate the inductance of primary side---L_P

$$L_P=\frac{2\cdot V_S\cdot I_O}{I_{PK}^2\cdot f_{SW}\cdot \eta_i^2}=1.9mH \quad (45)$$

5) Calculate the turns of primary, secondary and auxiliary (N_P, N_S, N_A)

$$N_p=\frac{L_P\cdot I_{PK}}{Ae\cdot \Delta B}\geq \frac{L_P\cdot I_{PK}}{Ae\cdot B\max}=89.8\,T \quad (46)$$

We choose N_P=93T

$$N_S=\frac{N_P}{N_{PS}}=6\,T \quad (47)$$

$$N_A=\frac{N_S\cdot V_A}{V_S}=16\,T \quad (48)$$

6) Check the maximum duty cycle of primary side

The maximum duty cycle of primary side is calculated as following:

$$D=\frac{(V_O+V_d)\cdot N_{PS}\cdot 0.4}{V_{indc}\cdot \eta_i}=0.49 \quad (49)$$

7) Check reverse voltage of auxiliary diode

$$V_{dar}=V_A+\frac{V_{indc\_max}\cdot N_A}{N_P}=79V \quad (50)$$

8) Feedback Resistors

$$\frac{R_{FB1}}{R_{FB2}}=\frac{V_o+V_D}{N_S\cdot V_{FB}}\cdot N_A-1=2.56 \quad (51)$$

R_{FB1}=24.9kΩ, R_{FB2}=9.85kΩ

9) Line Compensation Resistors

$$R_{LINE}=(\frac{t_{delay}}{Lp}\cdot R_{cs})/(\frac{N_A}{N_P}\cdot\frac{R_{FB2}}{R_{FB1}+R_{FB2}}\cdot\frac{0.8}{670k})=3.4k\,\Omega \quad (52)$$

Where V_{O_NL}=5V. Therefore, the output voltage at cable terminal at full load is a little higher than the voltage at no load.

Design Results Summary:

1.Maximum peak current of primary side and R_{CS}			
I_{PK}	330	mA	Peak current of primary side
R_{CS}	1.5	Ω	Current sensed resistor
2.Transformer			
L_P	1.90	mH	Inductance of primary side
N_{PS}	15.5	Turn ratio of primary and secondary	
N_P	93	T	Turns of primary side
N_S	6	T	Turns of secondary side
N_A	16	T	Turns of auxiliary side
D_{MAX}	0.49		Maximum duty cycle of primary side at V_{INDC}=80V
3. Primary power switch and diode			
V_{ds_switch}	510	V	Voltage stress of primary power switch
V_{dr}	29	V	Maximum reverse voltage of secondary diode
V_{dar}	79	V	Maximum reverse voltage of auxiliary diode
4. Voltage feedback resistors			
R_{FB1}	24.9k	Ω	Feedback resistor at upside from auxiliary side to FB pin
R_{FB2}	9.85k	Ω	Feedback resistor at downside from FB pin to GND
5. Line compensation resistor			
R_{LINE}	3.4k	Ω	Line compensation resistor

3. Summary

In order to get good performance of AP3765A, it is important to correctly design standby power, switching frequency, transformer parameters, feedback resistance and line compensation resistance. This application note only gives a preliminary design guideline about these aspects and considers ideal conditions, so some parameters need to be adjusted slightly on the basis of the calculated results.

4. Application of AP3765A with AP4340

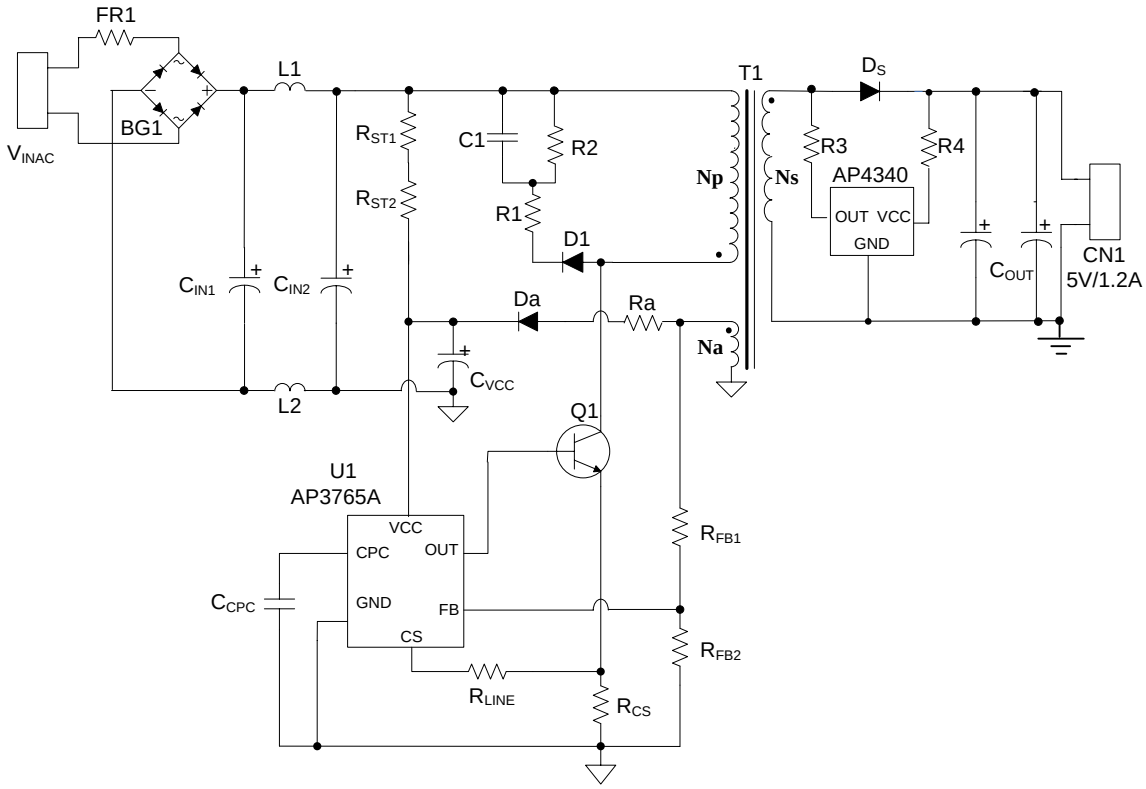

Figure 9. Typical Application Circuit of AP3765A with AP4340

In Primary Side Regulation of AP3765A application, if AP4340 is used at secondary side as the output voltage regulator, excellent dynamic response and low standby power can be achieved. When detecting the output voltage lower than a certain level, the AP4340 outputs periodical signals which will be coupled to auxiliary side and detected by AP3765A. By fast response and cooperation, AP4340 and AP3765A can effectively improve the transient performance for Primary Side Regulation power system. Besides, dummy load is not needed at secondary side and as a result standby power will be decreased. For more detailed operating principles, please refer to Application Note of AP4340 (Application Note 1078_BCD).