# AN1162

# DGD2005 Application Information

The DGD2005, High-side/Low-side gate driver is used to optimally drive the gate of MOSFETs or IGBTs. Below (Figure 1) is an example application using DGD2005 with MOSFETs to make three half-bridge circuits used to drive a three phase motor. Typical motor applications are AC Induction motors, PMSMs, and BLDC motors. DGD2005 can also be used in power supplies. In this document, the important parameters needed to design in the DGD2005 are discussed. Main sections are bootstrap resistor, diode, and capacitor selection, gate driver component selection, decoupling capacitor discussion, and PCB layout suggestions.

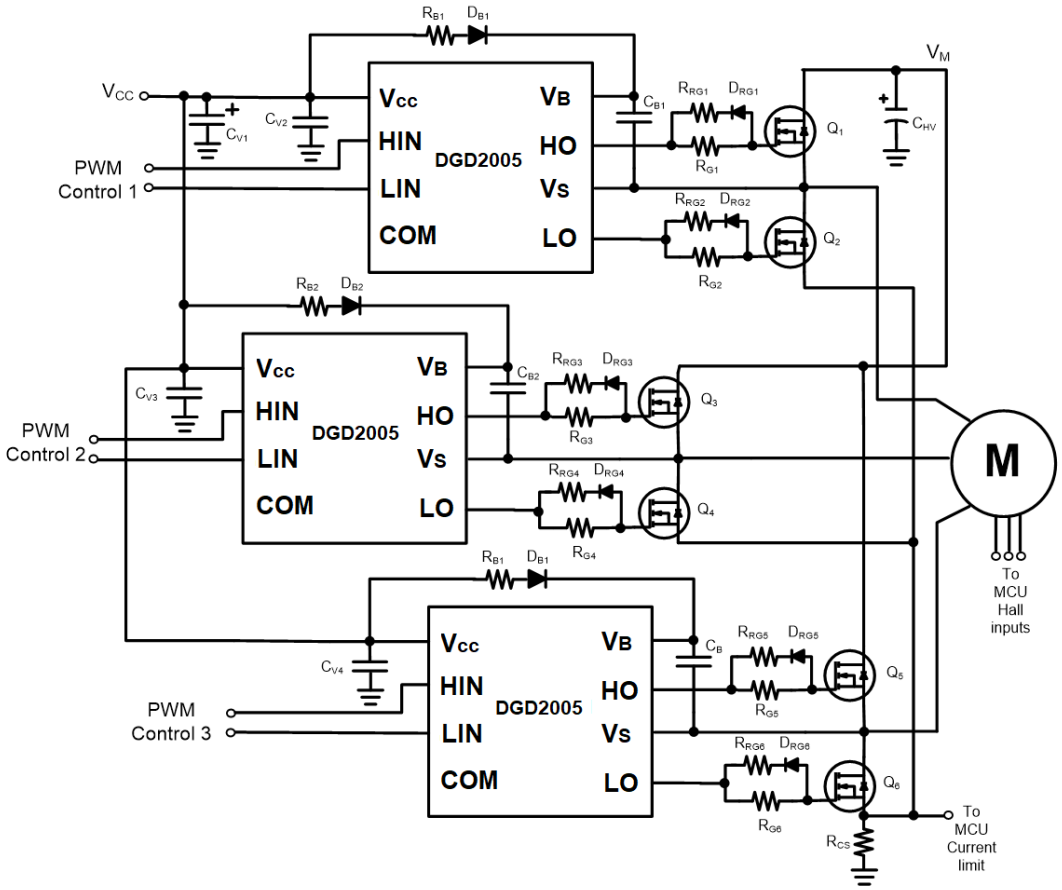


Figure 1. Three Phase Motor Driver application example of DGD2005

## Bootstrap Component Selection

### Bootstrap Resistor

Considering Figure 1, when the low-side MOSFET (Q2, Q4, or Q6) turns on, Vs pulls to GND and the bootstrap capacitor ($C_{B1}$, $C_{B2}$, or $C_{B3}$) is charged. When the high-side MOSFET (Q1, Q3, or Q5) is turned on, $V_S$ swings above Vcc and the charge on the bootstrap capacitor ($C_B$) provides current to drive the IC high-side gate driver. The first charge of $C_B$ from Vcc through the bootstrap resistor ($R_{BS1}$, $R_{BS2}$, or $R_{BS3}$) and bootstrap diode ($D_{BS1}$, $D_{BS2}$, or $D_{BS3}$) occurs when power is first applied and the low-side turns on the first time. At this time the charge current is the largest as typically $C_B$ is not discharged fully at each cycle during normal operation.

A bootstrap resistor ($R_{BS}$) is included in the bootstrap circuit to limit the inrush current that charges $C_B$ when Vs pulls below Vcc; this inrush current is largest with the first charge. Limiting inrush current is desirable to limit noise spike on Vs and COM, potentially causing shoot-through. The amplitude and length of time of the inrush current is determined mostly by the component value of $R_{BS}$ and $C_{BS}$ as well as Vcc level. The aim in resistor selection for the application is to slow down the inrush current but have minimal effect on the RC time constant of charging $C_{BS}$.

Typically, values for $R_{BS}$ are 3Ω to 10Ω, enough to dampen the inrush current but have little effect on the $V_{BS}$ turn on. Figures 2-5 illustrate the effect of different $R_{BS}$ values.

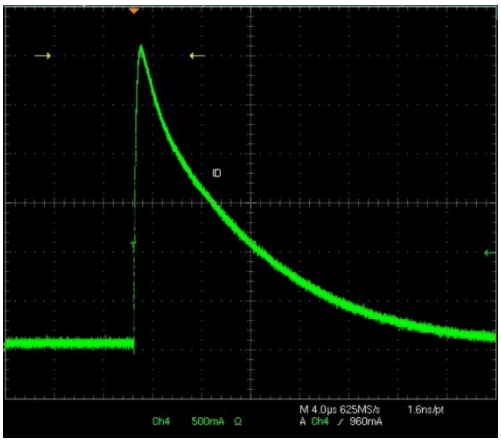


Figure 2. Bootstrap Peak inrush current ≈3A with RBS=3Ω, CBS=2.2µF

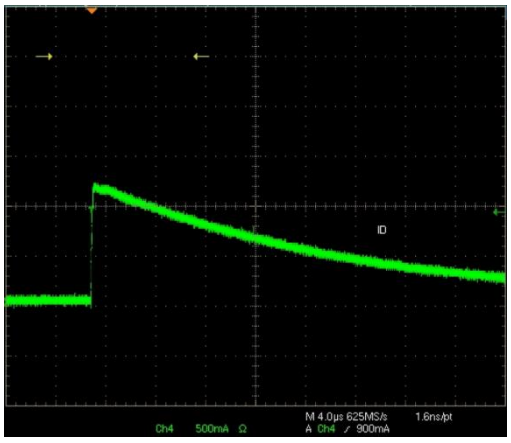


Figure 3. Bootstrap Peak inrush current ≈1.2A with RBS=10Ω, CBS=2.2µF

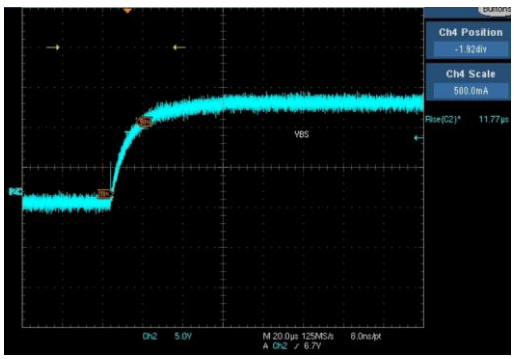


Figure 4. VBS Rise Time (11.8µs) with RBS=3Ω, CBS=2.2µF

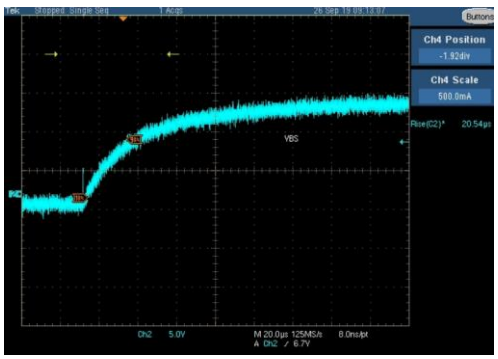


Figure 5. VBS Rise Time (20.5µs) with RBS=10Ω, CBS=2.2µF

**Bootstrap Diode**

The chosen bootstrap diode ($D_{BS}$) should be rated higher than the maximum rail voltage since the diode must be able to block the full rail voltage and any spikes seen at the $V_S$ node. The diode's current rating is simply the product of total charge (QT) required by the HVIC (High Voltage Integrated Circuit) and the switching frequency. An ultrafast recovery diode is recommended to minimize any delay of charging the $C_{BS}$ cap. A 1A ultrafast recovery diode is typical for DGD2005 applications.

**Bootstrap Capacitor**

The initial step in determining the value of the bootstrap capacitor is to determine the minimum voltage drop ($\Delta V_{BS}$) that can be guaranteed when the high-side device is turned on. In other words, the minimum gate-source voltage ($V_{GS\_min}$) must be greater than the UVLO of the high-side circuit, specifically $V_{BSUV-}$ level. Therefore, if $V_{GS\_min}$ is the minimum gate-source voltage such that:

$V_{GS\_min} > V_{BSUV-}$

Then:

$\Delta V_{BS} = Vcc - V_f - V_{GS\_min} - V_X$

Where:
- Vcc is the supply voltage to the DGD2005
- $V_f$ is the voltage drop across the bootstrap diode ($D_{BS}$)
- $V_X$ is the voltage drop across the MOSFET

$V_X$ is calculated as the current seen across low-side MOSFET multiplied by its $R_{DS\_ON}$ and is simply $V_{CE\_ON}$ at the specific output current if an IGBT were used instead.

In addition to the voltage drops across these components, other factors that cause $V_{BS}$ to drop are leakages, charge required to turn on the power devices, and duration of the high-side on time. The total charge (QT) required by the gate driver then equals:

$Q_T = Q_G + Q_{LS} + [I_{LK\_N}] * T_{H\_ON}$

Where:

$Q_G$ = gate charge of power device
$Q_{LS}$ = level shift charge required per cycle
$T_{H\_ON}$ = high-side on time
$I_{LK\_N}$ = sum of all leakages that include:
- $I_{GSS}/I_{GES}$: Gate-source leakage of the power device
- $I_{LK\_DB}$: Bootstrap diode leakage
- $I_{LK\_IC}$: Offset supply leakage of HVIC
- $I_{Q\_BS}$: Quiescent current for high-side supply
- $I_{LK\_CB}$: Bootstrap capacitor leakage

Bootstrap capacitor leakage ($I_{LK\_CBS}$) only applies to electrolytic types. Therefore, it is best not to use an electrolytic capacitor. Thus, bootstrap capacitor leakages will not be included in the calculations.

$Q_{LS}$ is not listed in the datasheet; depending on the process technology, it could range anywhere from 3-20nC for 500V to 1200V process respectively. Assuming a value of 10nC for the 600V process should be sufficient with added margin.

From the basic equation, then the minimum bootstrap capacitor is calculated as:

$C_{B\_min} \geq Q_T / \Delta V_{BS}$

Example using MOSFET, DMNH6021SK3Q

HVIC=DGD2005

Vcc = 12V
$Q_G$ = 20nC
$I_{GSS}$ = 100nA
$T_{H\_ON}$ = 10µs
$R_{DSON}$ = 25mΩ max, 125˚C
Iout = 5A
$I_{Q\_BS}$ = 130µA
$I_{LK\_IC}$ = 50µA
$Q_{LS}$ = 10nC
$V_F$ = 1.0V
$I_{LK\_DB}$ = 100µA
$V_{GSmin}$ = 10.0V

From equations:

$\Delta V_{BS}$ = 12V- 1.0V-10V-(0.125V) = 0.875V

$Q_T = Q_G + Q_{LS} + (I_{LK\_N} * T_{H\_ON})$ where $I_{LK\_N} * T_{H\_ON}$ = 2.8nC

= 20nC + 10nC + 2.8nC

= 32.8nC

Thus $C_{BS}$ min = 32.8nC/0.875V = 37nF.

The bootstrap capacitor calculated in the above example is the minimal value required to supply the needed charge. It is recommended that a margin of 2-3 times the calculated value be used. Utilizing values lower than this could result in over charging of the bootstrap capacitor especially during –VS transients.

Typically for motor driver applications $C_{BS}$ = 1µF to 10µF are used. It is recommended to use low ESR ceramic capacitors as close to the $V_B$ and $V_S$ pin as possible (see PCB layout suggestions section).

## Gate Resistor Component Selection

The most crucial time in the gate drive is the turn on and turn off of the MOSFET, and performing this function quickly, but with minimal noise and ringing is key. Too fast a rise/fall time can cause unnecessary ringing and poor EMI, and too slow a rise/fall time will increase switching losses in the MOSFET.

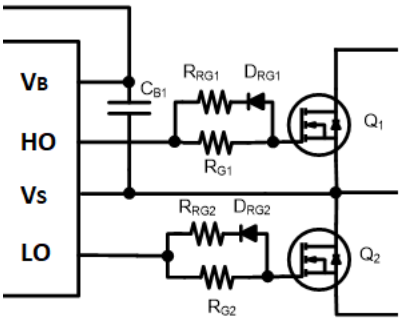


Figure 6. Gate Drive High-Side and Low-Side Components for DGD2005

Considering the gate driver components for DGD2005 in Figure 6, with the careful selection of $R_{Gn}$ and $R_{RGn}$, it is possible to selectively control the rise time and fall time of the gate drive to the MOSFET Qn. For turn on, all current will go from the IC through $R_{G1}$ and charge the MOSFET gate capacitance, hence increasing or decreasing $R_{Gn}$ will increase or decrease rise time in the application. With the addition of $D_{RGn}$, the fall time can be separately controlled as the turn off current flows from the MOSFET gate capacitor, through $R_{RGn}$ and $D_{RGn}$ to the driver in the IC to VS for high-side and COM for low-side. So, increasing or decreasing $R_{RGn}$ will increase or decrease the fall time. Sometimes finer control is not needed and only $R_{G1}$ and $R_{G2}$ are used.

Increasing turn on and turn off has the effect of limiting ringing and noise due to parasitic inductances, hence with a noisy environment, it may be necessary to increase the gate resistors. Gate component selection is a compromise of faster rise time with more ringing, and a poorer EMI but better efficiency, and a slower rise time with better EMI, better noise performance but poorer efficiency. The exact value depends on the parameters of the application and system requirements. Generally, for motors the switching speed is slower, and the application has more inherent noise, higher values are recommended, for example $R_G$ = 20Ω - 100Ω.

To have equal switching times for high-side and low-side, it is recommended that the gate driver components for high-side and low-side are mirrored. For example $R_{RG1} = R_{RG2}$, $D_{RG1} = D_{RG2}$ and $R_{G1} = R_{G2}$.

## Decoupling Capacitor Selection

For optimal operation, Vcc decoupling is crucial for all gate driver ICs. With poor decoupling, larger Vcc transients will occur at the IC when switching, and for greater and longer Vcc drops the IC can go into UVLO.

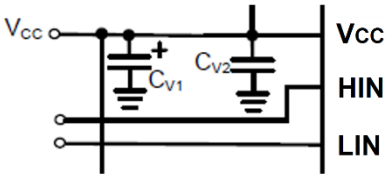


Figure 7. Suggested Vcc decoupling

As shown in Figure 7, two decoupling capacitors are recommended $C_{V1}$ and $C_{V2}$. $C_{V1}$ can be a larger electrolytic, for example 47µF (50V), and is used to dampen low frequency drains on supply: $C_{V1}$ does not need to be right next to the IC, but $C_{V2}$ is used to decouple faster edge changes to Vcc, and should be a low ESR ceramic capacitor placed close to the Vcc pin. This component provides stability when Vcc is quickly pulled down with load from the IC. Typical values for $C_{V2}$ are 0.1µF to 1µF.

For applications with multiple gate driver ICs (for example BLDC motor drive with 3 x gate drivers as shown in Figure 1), one larger electrolytic ($C_{V1}$) can be used and the three low ESR ceramic caps ($C_{V2}$, $C_{V3}$, $C_{V4}$) should be used close to the Vcc pin (see Layout section also).

## Input Resistors

The DGD2005 PWM inputs, HIN and LIN, are very high impedance inputs with a pull-down resistor on both inputs to COM (see Figure. 8). The pull-down resistor on HIN and LIN has a value of approximately 1MΩ.

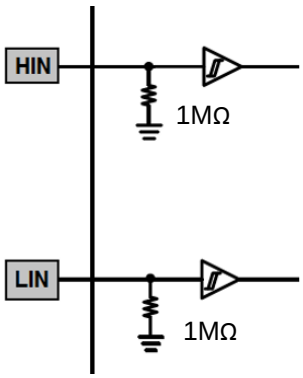


Figure 8. Input Logic for DGD2005

## Matching Gate Driver with MOSFET or IGBT

### IC drive current and MOSFET/IGBT gate charge

Gate Driver ICs are defined by their output drive current, its ability to source current to the gate of the MOSFET/IGBT at turn on and to sink current from the gate of the MOSFET/IGBT at turn off. For the DGD2005, the drive current is $I_{O+}$=290mA typical and $I_{O-}$=600mA typical.

For a given MOSFET/IGBT, with the known drive current of the DGD2005, you can calculate how long it will take to turn on/off the MOSFET/IGBT with the equation:

t = Qg/I

Qg = total charge of the MOSFET/IGBT as provided by the datasheet
I = sink/source capability of the gate driver IC
t = calculated rise/fall time with the given charge and drive current

For example with the Diodes' DGTD65T15H2TF, 650V IGBT, Qg = 61nC; and with the DGD2005 $I_{O+}$=290mA and $I_{O-}$=600mA, the tr = 210ns and tf = 102ns. These are estimates as the total charge given in the datasheet may not be the same conditions in the application. Also, an addition of a gate resistor will increase the tr and tf.

### Unexpected shoot-through with $dV_{DS}/d_t$

Unwanted MOSFET turn-on, caused by $C_{GD}$ x $dV_{DS}/d_t$ (see Figure 9) is often the cause of unexplained shoot through in the half-bridge circuit. Depending on the ratio of $C_{GS}$/ $C_{GD}$ , when the $dV_{DS}/d_t$ across low-side MOSFET (Q2) occurs (i.e when high-side MOSFET turns on), there can be a voltage applied to the gate of the Q2 MOSFET, turning on Q2 and causing shoot through. In effect a gate bouncing occurs causing a ringing on the VS line and the power ground.

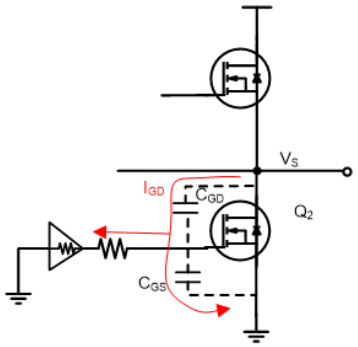


Figure 9. Unexpected shoot through with $dV_{DS}/d_t$

Considering Figure 9,

$I_{GD} = C_{GD}$ x $dV_{DS}/d_t$

$I_{GD}$ will flow towards the resistive load (and small inductance due to parasitics) of the gate driver and the $C_{GS}$ of the MOSFET. Hence this unwanted condition may be minimized by looking at the Ciss/Cres in the MOSFET datasheet (Ciss/Cres gives an indication of $C_{GS}/C_{GD}$); having a Ciss/Cres as large as possible will minimize this phenomenon. Also an external capacitor can be added to the gate-source of the MOSFET (for example 1nF) which will increase $C_{GS}/C_{GD}$.

## Minimum Pulse Requirement

The DGD2005 has RC filters on the input lines to be more resilient in noisy environments. With a rising edge at the input to the gate driver, followed by the propagation delay of the IC, delay from gate resistor, and rise time of the MOSFET, the half-bridge will then turn on producing bus voltage at the output. This MOSFET turn on produces significant system noise. For optimal operation, it is suggested to provide a minimum pulse width at the input to the IC from the MCU to ensure the turn off occurs after this event. As a rule of thumb, this minimum pulse should be 2 x propagation delay for high-side/low-side gate drivers; hence for the DGD2005, the minimum pulse recommended at the logic inputs is 440ns.

During typical operation, the DGD2005 will respond to an input greater than 50ns (approximate value from the RC input filter response). Hence for an input pulse greater than 50ns approximately the IC will follow the pulse as expected; and for an input pulse less than 50ns, there will be no response from the IC.

## PCB layout suggestions

Layout plays an important role in minimizing unwanted noise coupling, unpredicted glitches, and abnormal operation which can arise from a poor layout of the associated components. Figure 10 shows a schematic with parasitic inductances in the high-current path ($L_{P1}$, $L_{P2}$, $L_{P3}$, $L_{P4}$), which would be caused by inductance in the metal of the trace. Considering Figure 10, the length of the tracks in red should be minimized, and the bootstrap capacitor ($C_B$) and the decoupling capacitor ($C_D$) should be placed as close to the IC as possible in addition to using low ESR ceramic capacitors. And finally, the gate resistors ($R_{GH}$ and $R_{GL}$) and the sense resistor ($R_S$) should be surface mount devices. These suggestions will reduce the parasitics due to the PCB traces.

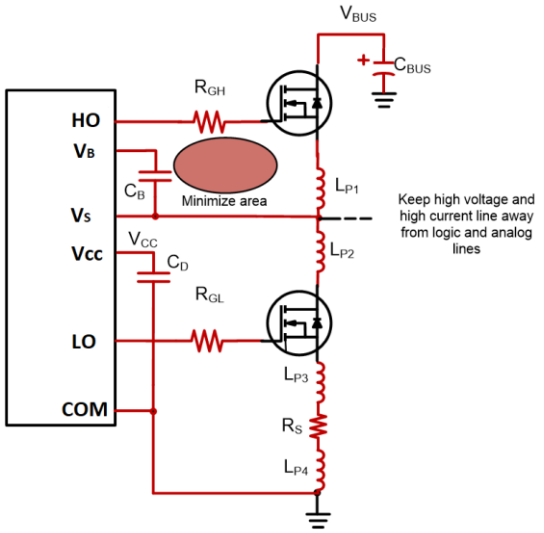


Figure 10. Layout suggestions for DGD2005 in a half-bridge, lines in red should be as short as possible.

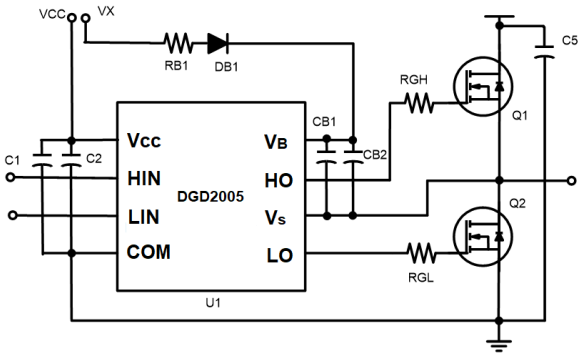


Figure 11. Schematic for layout example in Figure 12.

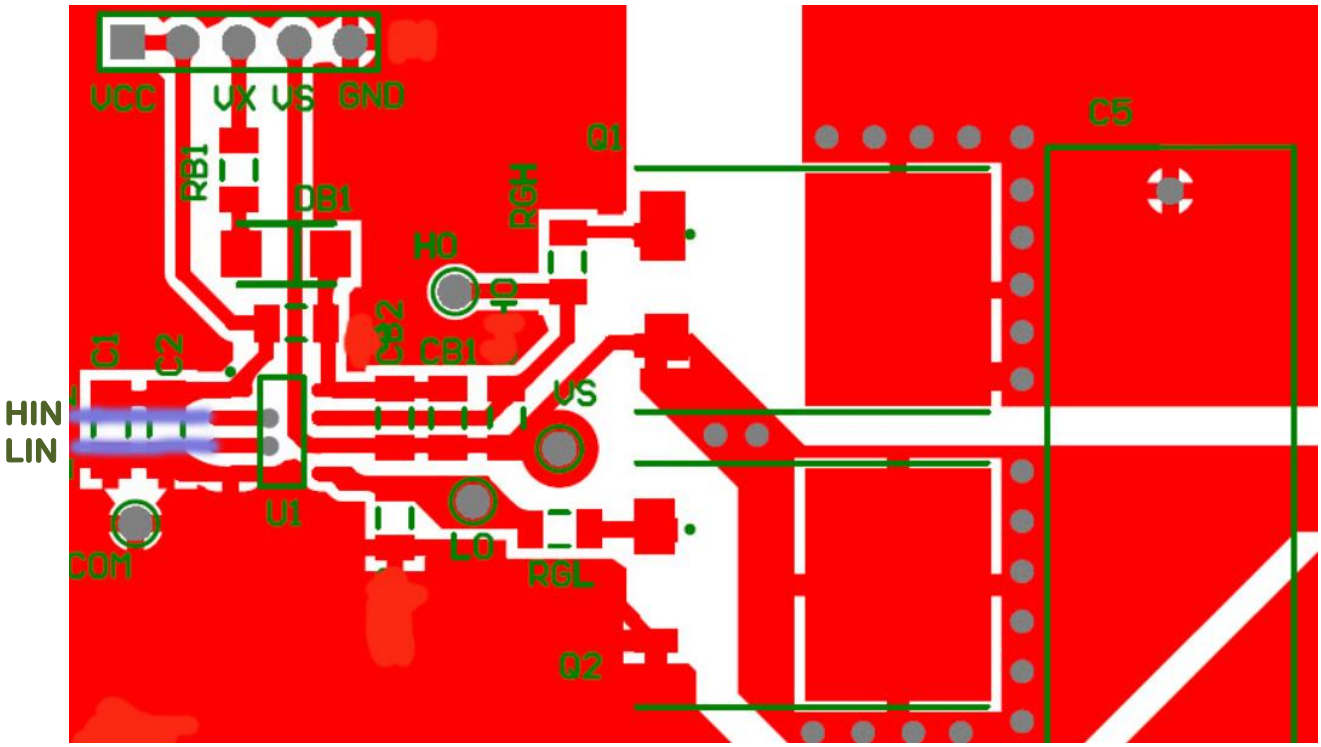


Fig 12. Layout of the schematic shown in Figure 11, DGD2005 in SOIC8.
All routing and components on top except for HIN and LIN from input

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