DIODES INCORPORATED

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Application Note for DPS1133

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Introduction

The DPS1133 is a unidirectional power switch for USB power delivery with protections for overvoltage, overcurrent, output short circuit, reversed voltage, reversed current, and overtemperature conditions. It can support up 84W of output power with user programmable capability. This document is written for engineers using DPS1133 in the USB power delivery circuit to obtain setup information. To simplify the task, this paper will go directly to the basic configuration for PDS1133 to operate and then to a specific example to demonstrate how to select components to achieve design targets.

Designing with DPS1133

1. Capacitance required for IN and OUT ports, C_{IN} and C_{OUT} The DPS1133 is rated for 24V on the input port and 3.5A continuous load on the output port. In order to support the rated power, 10uF capacitance on the input and output ports is recommended.

2. Define the operating voltage range, VLIM
The DPS1133 has an operating voltage from 4.5V to 24V. The operating voltage is set by the resistance between the VLIM and GND pins, RVLIM. The larger the RVLIM, the higher the operating voltage it can support. RVLIM can be chosen according to:

$$R_{VLIM} = [1.1 \text{ x Vin}] / 0.1\text{mA}$$
and
$$51\text{K}\Omega \le \text{RVLIM} \le 270\text{K}\Omega$$

When the DPS1133 carries a load, large voltage spikes will be imposed on top of the set input voltage when the load is being removed. If no or not enough voltage margin is applied, the voltage on the input port will go beyond the overvoltage threshold V_{OVPTH}, cause device shutdown and then turn back on due to the load drop out, resulting in an unstable system. To eliminate this problem, a 5 ~ 20% voltage margin is recommended. In this R_{VLIM} calculation, a 10% of margin, [1.1 x Vin] is being applied.

Once R_{VLIM} is chosen, the overvoltage threshold V_{OVPTH} is automatically set by design, which is

$$V_{OVPTH} = [1.1 \text{ x Vin}] + 0.5\text{V}$$

For an example, for a 12V input application, with 10% input voltage margin,

$$R_{VLIM} = [1.1 \text{ x } 12\text{V}] / 0.1\text{mA} = 132 \text{ K}\Omega$$

With R_{VLIM} = 132 KΩ, the voltage spike on the input port can swing up to Vin = 1.1 x 12V = 13.2V without triggering the overvoltage threshold V_{OVPTH}, and from the equation above,

$$V_{OVPTH} = [1.1 \text{ x } 12] + 0.5\text{V} = 13.7\text{V}$$

3. Device enable, EN
For the DPS1133 to work, the EN pin must pull to a logic high voltage. Tie the EN pin to a 2V DC supply enables the device output. If the voltage at the input port is within operating range, the output will ramp up to the desired voltage.

4. Current limit and over current setting, ILIM
The resistor between the ILIM and GND pins, RILIM, sets the device's current limit and will clamp the output current to this limit even when the load is demanding for more power.

The output current limit can be set according to the following:

$$RILIM = 100 / IILIM,$$

Where:

- I_{ILIM} is in ampere
- R_{ILIM} is in KΩ
- $27K\Omega \leq R_{ILIM} \leq 200K\Omega$

For an example, for a 2A current limit application,

$$R_{ILIM} = 100 / 2 = 50\ K\Omega$$

When the output current is founded to be larger than the programmed ILIM level (2A in this case) for more than 2us, the device goes to protection mode by clamping the output current to the programmed 2A and the output voltage will drop down significantly, to a level around or less than 25% of the input voltage.

For applications require continuous current from the output, a 10 ~ 20% margin should apply. To apply this margin, follow

$$R_{ILIM} = 100 / [I_{ILIM} \times 1.2]$$

From the above example, if a maximum 2A of continues current is required, we apply a 20% margin, and R_{ILIM} can be calculated by following

$$R_{ILIM} = 100 / [I_{ILIM} \times 1.2] = 100 / [2 \times 1.2] = 41.7\ K\Omega$$

5. Short circuit protection setting, ILIM
In the event of output short circuit, the output current will rise rapidly. When this current exceeds the fast-trip threshold $I_{FASTRIP}$, the device will be turned off immediately to protect the device from being damaged.

The $I_{FASTRIP}$ is also set by the ILIM current, I_{ILIM},

$$I_{FASTRIP} = 1.125 \times I_{ILIM} + 1.8$$

Where I_{ILIM} is in ampere.

For ILIM at 2A, $I_{FASTRIP}$ is calculated to: $I_{FASTRIP} = 1.125 \times 2 + 1.8 = 4.05A$

Another method of protection is through voltage trip. When the device is under heavy load condition, the output voltage will rapidly drop below 25% of the input voltage, with its output current limit to I_{ILIM} at the meantime. When the heavy load condition is removed, the device will resume normal operation.

6. Output current monitoring, IMON
Output current monitoring is through the resistor between the IMON and GND pins, R_{IMON}. To prevent noise from entering into the IMON pin, a 100pF capacitor is placed across the IMON and GND pins. R_{IMON} should be chosen such that the voltage across the IMON pin, V_{IMON} is below 4.5V. By design, a 10uA current on IMON pin will be generated for every 1A load at the output, therefore, output current sensing can be obtained from the voltage drop at the IMON pin, V_{IMON}:

$$V_{IMON} = (10uA/A) \times I_{OUT} \times R_{IMON}, \text{ where } R_{IMON} \text{ is in } K\Omega$$

$$\text{and } V_{IMON} < 4.5V$$

For an example, if a 2A load is presented on the output, with R_{IMON} = 100 KΩ, V_{IMON} will be 2V. The calculation is as following:

$$V_{IMON} = (10uA/A) \times (2A) \times (100\ K\Omega) = 2V$$

7. Output ramp time control, DV/DT
The capacitor placed between the DV/DT and GND pins sets the output voltage ramp rate at the device turn on. This ramp time is determined by the capacitance from the DV/DT pin to ground, CDV/DT:

$$C_{DV/DT} = t_{DV/DT} / [8.3 \times 10\text{-}2 \times V_{IN}]$$

Where $t_{DV/DT}$ is the total ramp time in ms

and the unit of V_{IN} is volt, $C_{DV/DT}$ is nF.

For an example, if the output ramp time from 0V to 12V is specified to be 1ms, the required capacitance $C_{DV/DT}$ is calculated to be:

$$C_{DV/DT} = t_{DV/DT} / [8.3 \times 10\text{-}2 \times V_{IN}] = 1000ms / [8.3 \times 10\text{-}2 \times 12V] = 1nF$$

Please refer to the DPS1133 datasheet for more information on output ramp control

8. Fast role swap control, FRS
To enable fast role swap, a positive pulse with 2V of amplitude is applied to the FRS pin. FRS is taken action after the FRS transition low for a certain time. Please refer to Figure 1 and 2 for details on the FRS timing requirements. When FRS function is not used, simply leave the FRS pin open or tie it to ground.

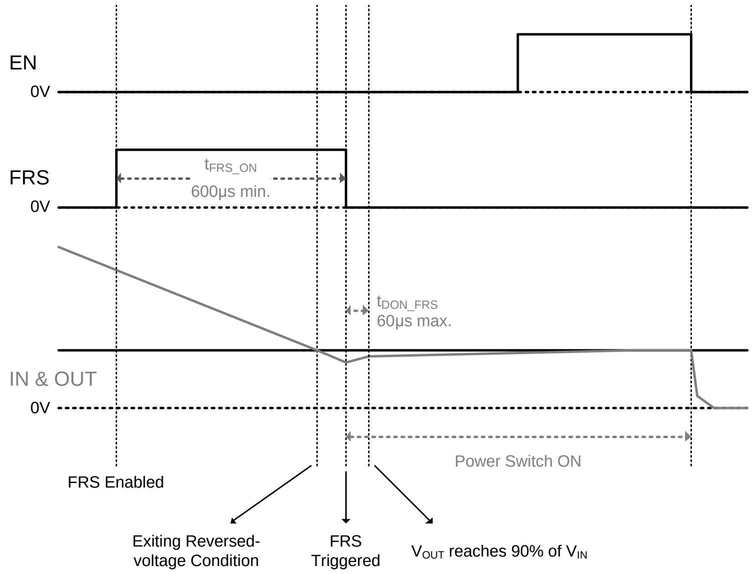

Figure 1. FRS Control Sequence for Fast Role Swap
Power Switch ON at Falling Edge of FRS Signal after Exiting RVP Condition

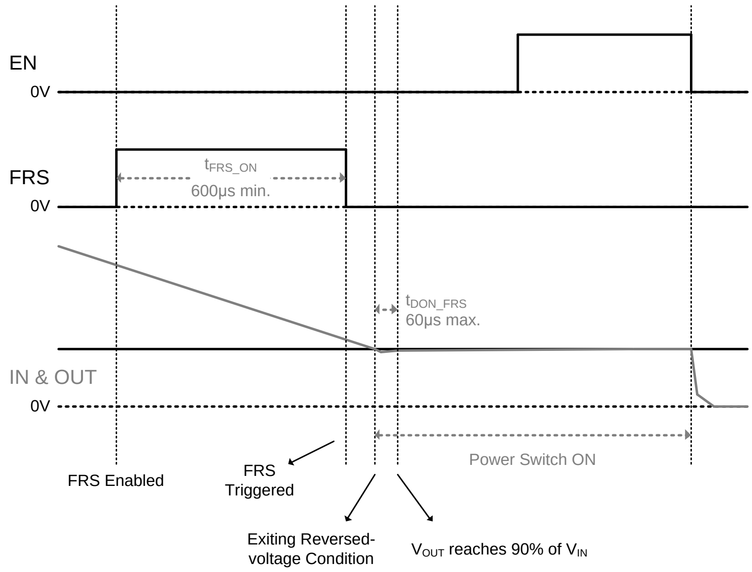

Figure 2. FRS Control Sequence for Fast Role Swap
Power Switch ON When Exiting RVP Condition after FRS is Triggered (Falling Edge)

9. Discharge function, DISC1 and DISC2
   To discharge the input and output port, a positive voltage must be applied to the DISC1 and DISC2 pins respectively. A 2V voltage is sufficient to discharge the ports.

10. Regulated voltage, VREG
    The internal regulator voltage can be monitored via the VREG pin. For smooth regulator voltage, a 0.1µF capacitor should be placed from the VREG pin to GND. The nominal VREG voltage is 5V.

11. Fault status reporting, FAULTB
    In the events of the input overvoltage, overcurrent, reversed voltage, reversed current, short-circuit, ILIM short to ground and over temperature conditions, the device will generate a fault signal by pulling the FAULTB voltage, V_{FAULTB} low. V_{FAULTB} will remain low until all of the above conditions have cleared. A pull up resistor, R_{PU} from FAULTB to a supply voltage of 5V will satisfy the fault reporting needs. To filter out the noise, a 0.1µF capacitor is placed from the FAULTB pin to ground. The R_{PU} resistor should not be too large, especially when quick FAULBT response time is required. Generally a 10 KΩ R_{PU} or smaller is recommended.

    A typical application circuit below demonstrates the general settings for the DPS1133 device circuit.

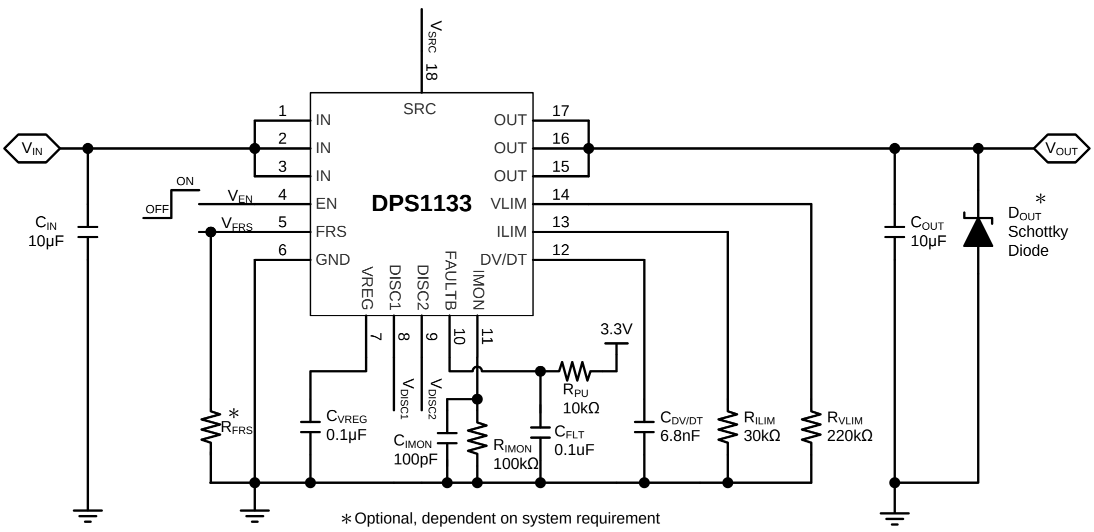

Figure 3. Typical application circuit for DPS1133