Advanced Low Voltage CMOS with Bus Hold (ALVCH) 3.3V Logic

Introduction

Pericom's new Advanced Low Voltage CMOS with bus hold (ALVCH) logic was especially designed for fast 3.5 ns propagation delays and low noise while providing a "last state" hold feature. This note includes the major advantages of this new product line.

Circuit Operation

Figure 1 shows the output stage of the ALVCH which includes a proprietary active pull-down circuit (and R2) that reduces ground bounce and undershoot. An output is sensed for a below ground undershoot level in a negative feedback circuit. The pull-down predriver, controlled by the edge rate controller, then reduces the preamp output drive, thus increasing the NMOS transistor channel resistance. Also, R1 is in series with the active pull-up to reduce overshoot.

Figure 2 shows a cross section of the ALVCH chip. The inherent diodes D1, D2, and D3 can cause problems in some applications if not for proper chip design methods. R1, R2, and the edge control circuit slow the output rise and fall times. Slowing the edges reduces overshoot and undershoot.

Inherent diode D2 is shorted and the substrate diode D3 is always back-biased. D1 is the only forward biased inherent diode when driving a 5V bus (and this can be alleviated with the I/O Tolerant part). So, there is never a clamp action that could damage the part.

The Advanced Low Voltage CMOS family with bus hold, known as ALVCH, has a hold feature that retains the last state at the input.

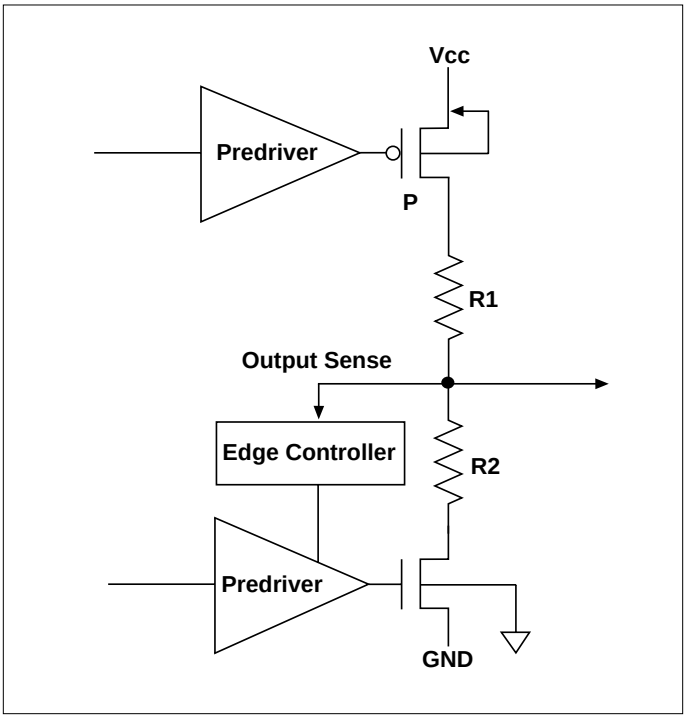

Figure 1. ALVCH Output Circuit

Bus Hold

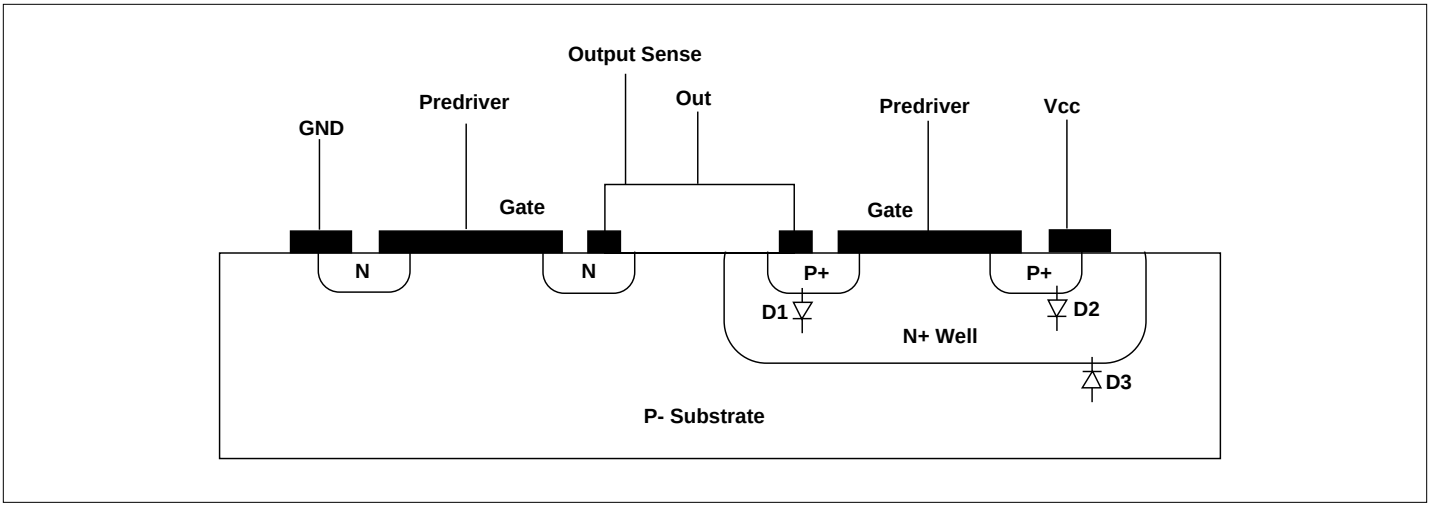

Figure 2. ALVCH Cross Section—Inherent Diode Locations

This option means that floating inputs do not need pull-up or pull-down resistors. Un-terminated floating inputs could cause the buffer to oscillate and destroy itself. Notice that the ALVCH series is not 5V I/O Tolerant. The bus hold circuit is shown in Figure 3. Inverters basically loop on a logic "1" or "0" so a logic low or high results in the same level out. R1 sets hold current to about 100µA.

Propagation Delay — Speed vs. Power

ALVC and ALVCH families are very fast logic devices that exhibit delays to 3.5ns with 50pF loads. This line of product was designed with a proprietary 0.5m CMOS process. Because of this process the power consumption is minimal while maintaining fast prop delays.

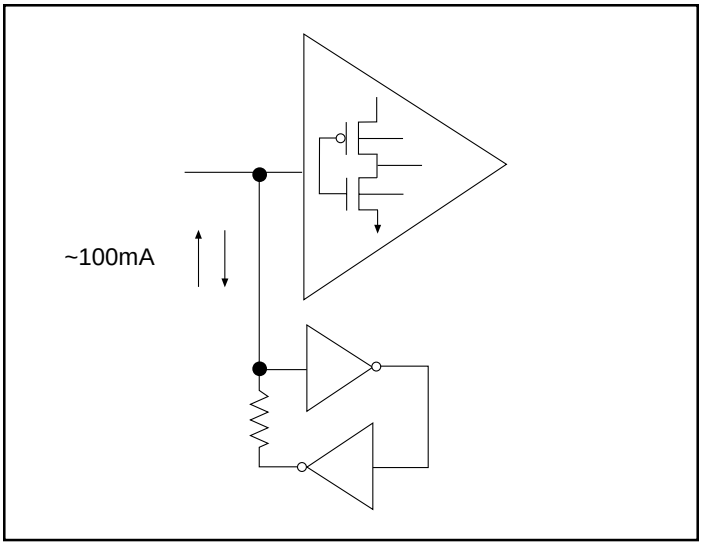

Figure 3. Bus Hold Circuit

Noise Application Information

Not only do these families have low power and small delays, but they also have low noise. Typically, the ground bounce is <0.4V with 50pF loading. Overshoot and undershoot is <0.3V. This makes these parts ideal for buffering 3.3V DRAM that are not tolerant to 5V. The reason for this low noise is the proprietary edge control in the pull-down and series resistors in the pull-up and pull-down circuits. These parts have slow edges. Usually they match up very well with 60Ω to 80Ω traces up to 10 inches long. Because of the minimal noise, these devices are ideal for 3.3V memory.