Interfacing PECL to LVDS

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PECL (Positive/Pseudo Emitter Coupled Logic) drivers and receivers are widely employed for high-speed backplanes and point-to-point serial connections. Today's electronic systems continue the advance to higher clock speeds operating from a single 3.3V supply. A PECL driver's differential output voltage swing of 800mV to 1.0V in combination with its large 2.0V offset brings out problems with system power and EMI generation. Newer system designs are therefore migrating to an alternative differential technology such as LVDS (Low Voltage Differential Signaling).

LVDS drivers and receivers provide a system design with the following benefits:

- Low voltage swing signals (300mV - 400mV) provide a higher operating frequency, reduced transient switching noise (lower EMI), and lower power dissipation.
- Simple terminated transmission line (single 100-Ohm resistor) eliminates signal reflection, provide higher bandwidth, improved noise margins, and higher DC drive capability for heavily loaded signal nets.
- Single-ended or differential receiver configurations allow multiple loads and point-to-point interconnect operation up to 200 MHz

Interface Circuit

This application note illustrates the simple resistor network required for interfacing a PECL driver and an LVDS receiver. Both PECL and LVDS buffers implement differential low-voltage signaling techniques, but with different swing and offset voltage levels. A PECL driver's differential output signal is more positive than is expected by the input circuit of an LVDS receiver. Implementing pulldown resistors in a Thevenin parallel termination resistor divider network will properly bias the PECL DC voltage level to within range of the LVDS receiver.

Parameter	PECL	LVPECL	LVDS
V_{CC}	5.0V	3.3V	3.3V
V_{OH}	4.0V	2.5V	1.4V
V_{OL}	3.2V	1.5V	1.0V
V_{PP}	800-1000mV	800-1000mV	250-400mV
V_{OS}	2.0V	2.0V	1.2V

Signal Voltage Comparisons

(continued)

The Thevenin parallel resistor network should be placed near the LVDS receiver to minimize signal reflections, (see Figure 1). The parallel equivalent impedance of the resistor network is calculated to match the circuit line's characteristic impedance (Z).

$R1 \parallel (R2 + R3) = Z$

The DC voltage level at point A should be V_{CC} - 2.0V while point B is biased to a level within the LVDS common mode input range.

Point A: $[(R2 + R3) / (R1 + R2 + R3)] = 2.0V / V_{CC}$

Point B: $R3 / (R1 + R2 + R3) = V_{IL} / V_{CC}$

Where V_{IL} is 1.2V (LVDS input common mode voltage)

The AC voltage swing at the LVDS receiver's point B is calculated from a simple voltage divider network:

$V_{BAC} = [R3 / (R2 + R3)] * V_{AAC}$

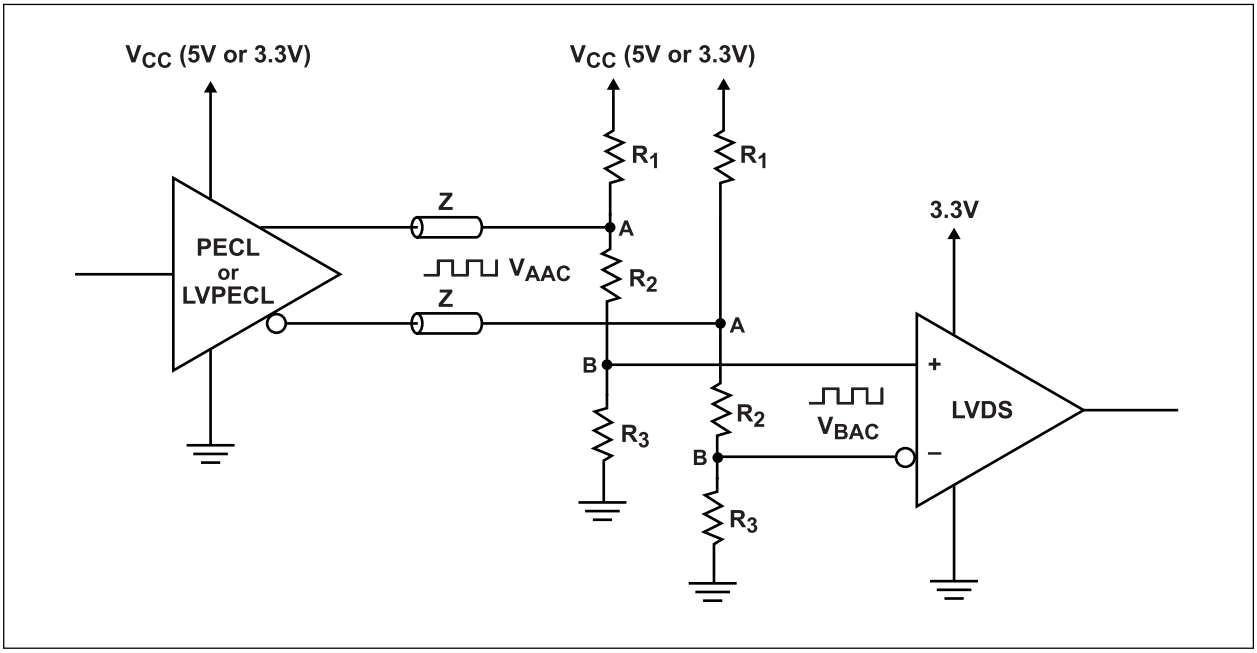

Figure1. Resistor Network Interface