APPLICATION NOTE 1126
1.5A, 1.4MHZ HIGH EFFICIENCY SYNCHRONOUS DC-DC BUCK CONVERTER

Introduction

The AP3418 is a 1.4MHz fixed frequency, current mode, PWM synchronous buck (step-down) DC-DC converter, capable of driving a 1.5A load with high efficiency, excellent line and load regulation. The device integrates synchronous P-channel and N-channel power MOSFET switches with low on-resistance. It is ideal for powering portable equipment that runs from a single Li-ion battery.

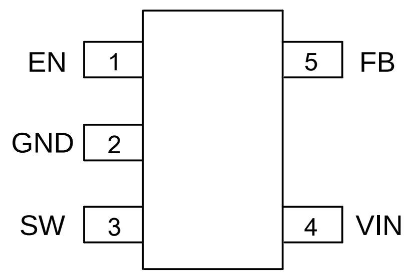
A standard series of inductors are available from several different manufacturers optimized for use with the AP3418. This feature greatly simplifies the design of switch-mode power supplies.

The AP3418 is available in SOT25 package.

Function Block Diagram

The pin configuration and the representative block diagram of the AP3418 are respectively shown in Figure1 and Figure 2.

(Top View)



SOT25

Figure 1. Pin Configuration of AP3418

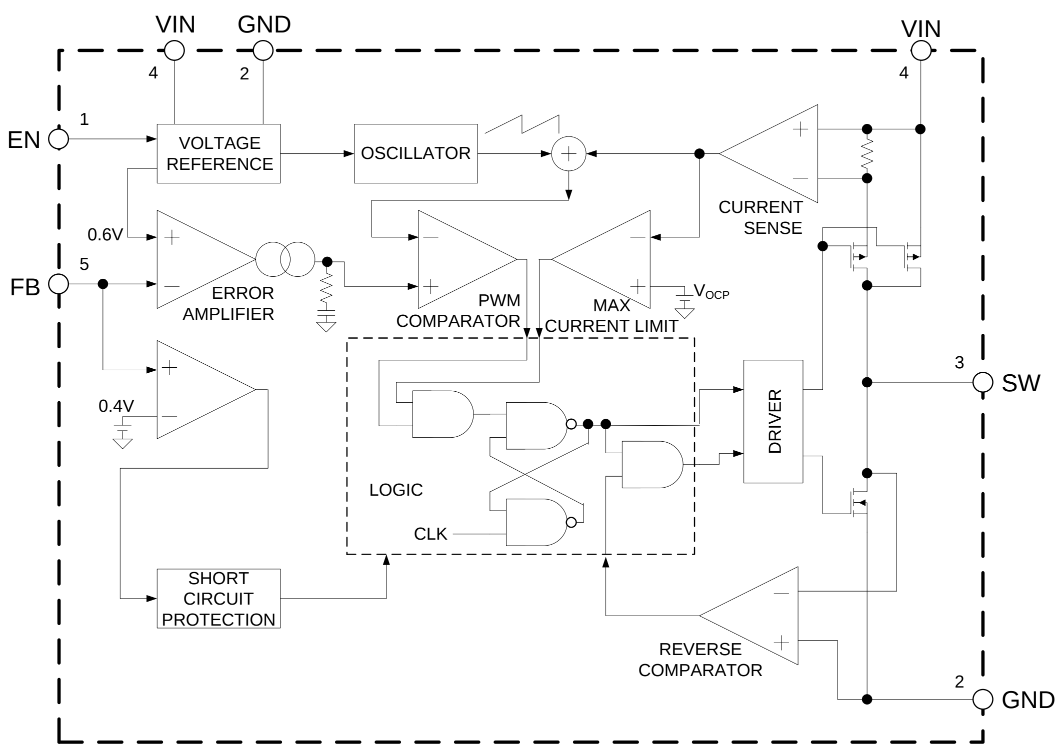


Figure 2. Functional Block Diagram of AP3418

EVB Schematic

A general AP3418 application circuit is shown in Figure 3. External component selection is driven by the load requirement, and begins with the selection of the inductor L1. Once L1 is chosen, C_{IN} and C_{OUT} can be selected.

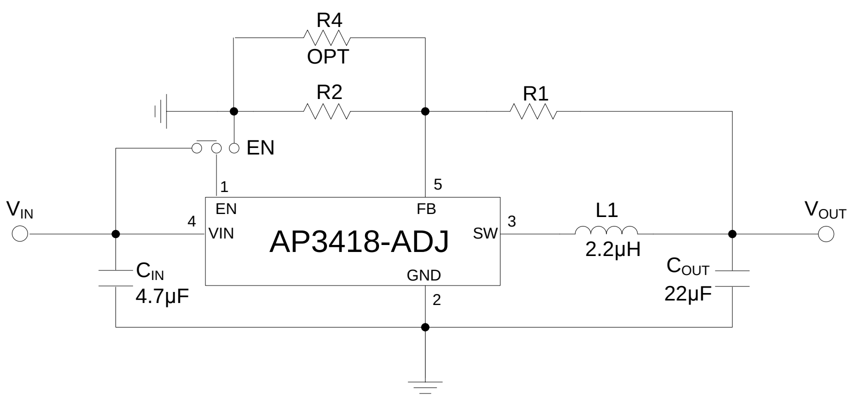


Figure 3. Schematic of AP3418

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L1 (µH)
3.3	135	30	2.2
2.5	95	30	2.2
1.8	60	30	2.2
1.2	30	30	2.2

Application Notes

Inductor Selection

Although the inductor does not influence the operating frequency, the inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L decreases with higher inductance and increases with higher V_{IN} or V_{OUT}.

$$\Delta I_L = \frac{V_{OUT}}{f_{osc} \times L1} \times (1 - \frac{V_{OUT}}{V_{IN}})$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple, greater core losses, and lower output current capability. ΔI_L typical value is 20% to 40% of output current.

Another important parameter for the inductor is the current rating. Exceeding an inductor's maximum current rating may cause the inductor to saturate and overheat. If inductor value has been selected, the peak inductor current can be calculated as the following:

$$I_{PEAK} = I_{OUT} + V_{OUT} \times \frac{V_{IN} - V_{OUT}}{2 \times f_{OSC} \times V_{IN} \times L1}$$

It should be ensured that the current rating of the selected inductor is 1.5 times of the I_{PEAK}.

Input Capacitor Selection

Because the buck converter has a pulsating input current, a low ESR input capacitor is required. This results in the best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. Also the input capacitor must be sufficiently large to stabilize the input voltage during heavy load transients. Ceramic capacitors show a good performance because of the low ESR value, and they are less sensitive against voltage transients and spikes. Place the input capacitor as close as possible to the input pin of the device for best performance. The typical value is about 4.7µF. The X5R or X7R ceramic capacitors have the best temperature and voltage characteristics, which is good for input capacitor.

Application Notes (Cont.)

Output Capacitor Selection

The output capacitor is the most critical component of a switching regulator, it is used for output filtering and keeping the loop stable. The selection of C_{OUT} is driven by the required ESR to minimize voltage ripple and load step transients. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is determined by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{8 \times f_{OSC} \times C_{OUT}} \right)$$

The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Once the ESR requirements for C_{OUT} have been met, the RMS current rating generally far exceeds the $I_{RIPPLE\ (P-P)}$ requirement, except for an all ceramic solution. In most applications, a 22µF ceramic capacitor is usually enough for these conditions.

Feedback Divider Resistors

The AP3418 develops a 0.6V reference voltage between the feedback pin, FB, and the signal ground as shown in Figure 3. The output voltage is set by a resistive divider according to the following formula:

$$V_{OUT} = 0.6 \times \left(1 + \frac{R1}{R2}\right)$$

Layout Consideration

PCB layout is very important to the performance of the AP3418. The loop which switching current flows through should be kept as short as possible. The external components (especially C_{IN}) should be placed as close to the IC as possible.

Try to route the feedback trace as far from the inductor and noisy power traces as possible. You would also like the feedback trace to be as direct as possible and somewhat thick. These two sometimes involve a trade-off, but keeping it away from inductor and other noise sources is the more critical of the two. Locate the feedback divider resistor network near the feedback pin with short leads.

Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. These copper areas should be connected to one of the input supplies: VIN or GND.

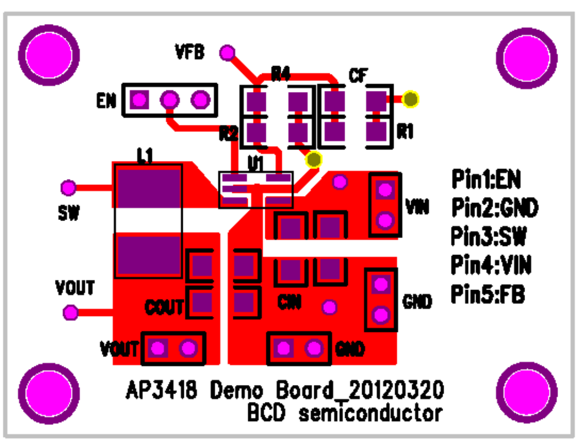


Figure 4. Top Layer

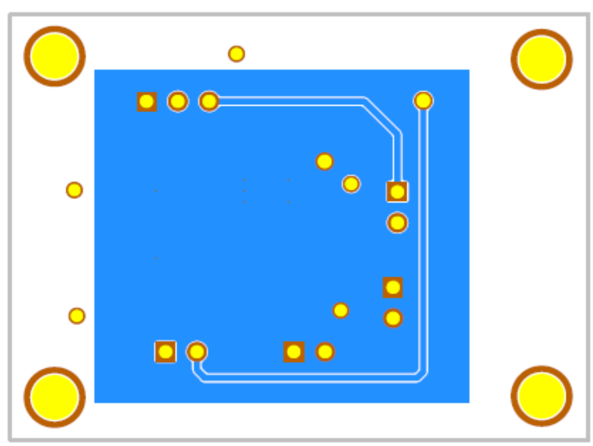


Figure 5. Bottom Layer

Bill of Materials (BOM)

Location	Quantity	Specification	Size
C_{IN}	1	4.7µF	C1206
C_{OUT}	1	22µF	C1206
R1	1	30kΩ (1%)	R1206
R2	1	30kΩ (1%)	R1206
L1	1	2.2µH	4.0(mm) x 4.0(mm)
U1	1	AP3418	SOT25

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