High Voltage Green Mode PWM Controller AP3105NA/NV/NL/NR

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1. Introduction

The AP3105NX is a low start-up current, current mode PWM controller with green-mode power-saving operation. Different from AP3103, AP3105NX's PWM switching frequency at normal operation is fixed at 65kHz dithering with a narrow range. The difference between AP3103 and AP3105NX is shown in Table 1. The dithering of frequency will improve EMI feature. When the load decreases, the frequency will reduce and when at a very low load, the IC will enter the "burst mode" to minimize switching loss. A minimum 20kHz frequency switching is to avoid the audible noise as well as to reduce the standby loss. A so-called VCC Maintain Mode is applied under light load to realize a stable output and to reduce the loss on the start-up resistor. The standby power of the system using AP3105NX can be reduced to 60mW at 230V input.

	AP3103	AP3105NX
Frequency	Adjustable	Fixed at 65kHz
V_{FB} Resistor	4.5kΩ	10kΩ
Standby Performance	Better	Best
External Protection	NA	By "CTRL" pin
VCC OVP	Auto-recoverable	Latch /Auto-recoverable
OLP & FOCP	Auto-recoverable	Latch /Auto-recoverable

Table 1. The Difference between AP3103/AP3105NX

The AP3105NX integrates a lot of functions such as the Lead Edge Blanking (LEB) of the current sensing, internal slope compensation and several protection features which include cycle-by-cycle current limit (OCP), fast OCP (FOCP), VCC over voltage protection, OTP, OLP protection. The "CTRL" pin is designed for customers to add external protection functions such as OVP and OTP.

The AP3105NX is specially designed for off-line AC-DC power supply, such as LCD monitors, notebook adapters and battery charger applications. It can offer the designers a cost-effective solution while keeping versatile protection features. The IC uses the SOT-23-6 package type to realize its compact size.

This application note includes detailed explanation of the IC's major functions, some considerations about the PCB layout, and methods for reducing the standby power loss, and finally presents a demo design of a 12V 2A adaptor.

2. Function Description

2.1 CTRL Pin

For some applications, the system requires external programmable protection function. The CTRL pin has two kinds of modes to trigger the protection: high level trigger and low level trigger. The low threshold voltage is 0.5V and high threshold voltage is 2.5V. When the CTRL pin voltage is lower than 0.5V or higher than 2.5V, latch or auto-restart protection will be triggered (different versions of AP3105NX offer different protection combinations, which are shown in Table 2).

Version	VCC OVP	OLP& FOCP	CTRL (Low)	CTRL (High)
AP3105NA	Auto-recoverable	Auto-recoverable	Latch	Auto-recoverable
AP3105NV	Latch	Auto-recoverable	Latch	Latch
AP3105NL	Latch	Latch	Latch	Latch
AP3105NR	Auto-recoverable	Auto-recoverable	Auto-recoverable	Latch

Table 2. Version Classification of AP3105NX

CTRL pin voltage maintains 1.6V if the pin is floating, so leave CTRL pin open if the designer does not need this function. Once the latch protection is triggered, the bulk capacitor will provide the energy to the IC through start-up resistor to ensure the IC disable the output signal (latch mode). This mode will not be released until the AC input is shut off. Therefore, the de-latch time is mainly depending on the value of HV startup bulk capacitor. If the system needs a short de-latch time, it is better for the startup resistor to take power from the point before the rectifier bridge. Typical application of CTRL pin is shown in Figure 1.

Note:
1. The sink current to the CTRL pin should be lower

than 5mA by selecting a proper pull up resistor.

2. If the designer needs to apply a bypass capacitor on CTRL pin, the capacitor should not be more than 1nF.

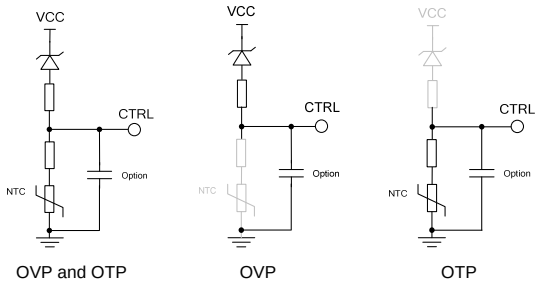


Figure 1. CTRL Pin Application

2.2 Difference of AP3105&AP3105NX

Table 3 shows the difference between AP3105&AP3105NX.

	AP3105	AP3105NX
OLP Delay Time	48ms@start-up 32ms@normal operating	100ms@start-up 64ms@normal operating
V_{CS} Adjustable @ start-up	NA	Adjustable

Table 3. AP3105 vs. AP3105NX

2.3 Longer OLP Delay Time for Capacitive Load

A capacitive load needs more power to be charged at start-up time. One solution is to enlarge the OCP point and keep the same start-up time, otherwise it will trigger OLP protection mode. Another solution is to extend the OCP delay time, which can simplify the transformer design since it is no need to rise the OCP point. Thus AP3105NX makes the OLP delay time longer to 100ms at start-up state and 64ms at operating mode. If FB pin's value is over 4V for 64ms at operating state or for 100ms at start-up, IC will enter OLP mode to limit the input power. Figure 2 and Figure 3 show the startup state with different OLP delay time under capacitive load. A shorter delay time may trigger OLP under capacitive load while a longer OLP delay time resulting start-up succeed.

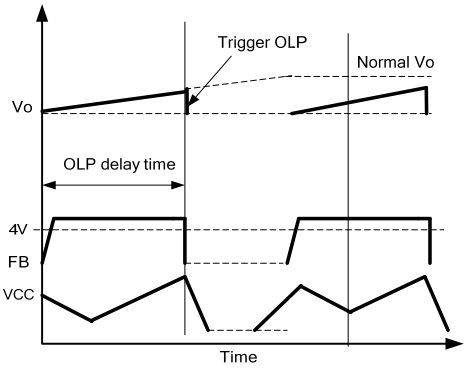


Figure 2. Shorter OLP Delay Time

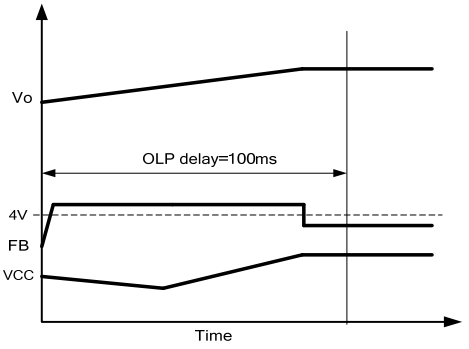


Figure 3. Longer OLP Delay Time

2.4 Adjusting the Primary Peak Current at Start-up

AP3105NX makes the primary peak current adjustable to limit the V_{DS} crossing MOSFET at start-up. An 85μA DC current source is added on SENSE pin, generating a DC voltage difference between SENSE pin and V_{CS}, which makes the V_{CS} equal to 0.95V to 85μA*R_F (as shown in Figure 5). As a result, MOSFET's peak current is limited at start up time, resulting a lower V_{DS} crossing MOSFET. This current source will be taken off after 37ms and not be effective under normal operating mode (as shown in Figure 4). R_F cannot be too large that makes the peak current too small and leads start-up fail at low line input. A proper value of R_F is 680Ω to 2.5kΩ.

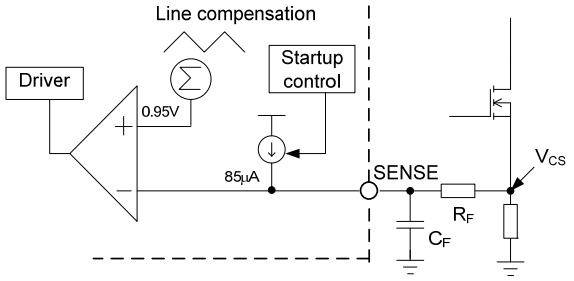


Figure 4. Current Source at SENSE Pin

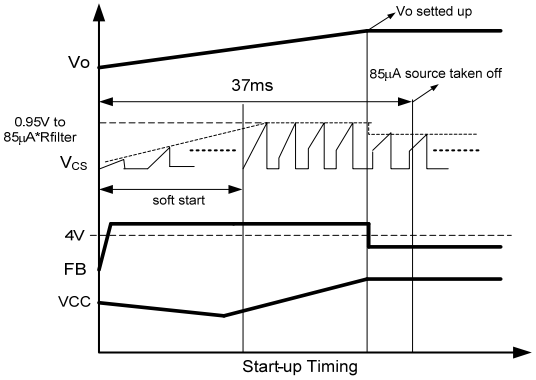


Figure 5. Start-up Timing of AP3105NX

2.5 Fast OCP Function

When the load is short-circuited, the power converter can be protected by OLP protection. But if the output filter inductor and the secondary Schottky are short-circuited, the transformer will be immediately saturated resulting in the breakdown of the MOSFET due to high voltage stress. The AP3105NX bears built-in fast OCP function to alleviate the saturation of the transformer and reduce the voltage stress of MOSFET. The FOCP position and FOCP waveform are shown in Figure 7 and Figure 8. When the secondary Schottky and the output filter inductor is short-circuited, the power converter can trigger latch or auto-restart immediately within several switching cycles with fast OCP. The FOCP threshold on SENSE pin is 1.8V.

In some applications, high spike voltage appears on the rise edge of the SENSE pin waveform due to a large transformer primary winding's parasitic capacitor or an irrational PCB layout , which may exceed the 1.8V threshold and trigger FOCP protection by error (as shown in Figure 6). To avoid this result, a RC filter is added on SENSE pin. The recommended resistor value of filter is over 680Ω when the capacitor is 220pF.

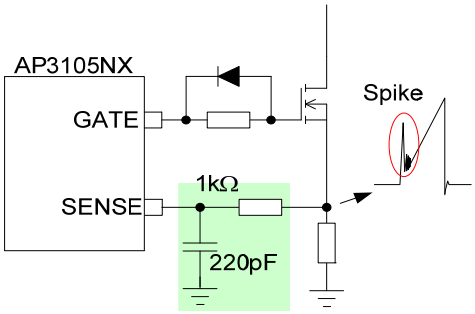


Figure 6. Sense Pin RC Filter

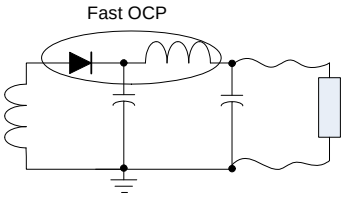


Figure 7. FOCP Position

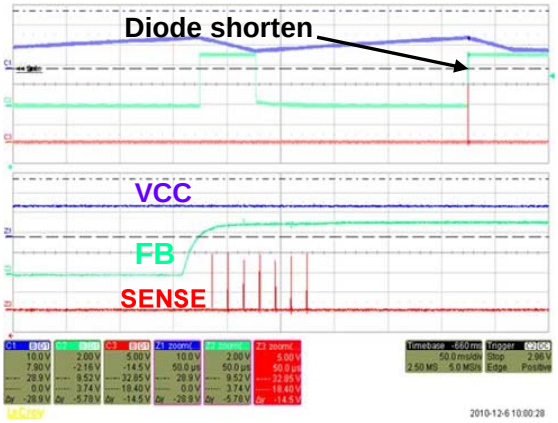


Figure 8. FOCP Waveform

2.6 VCC Maintain Mode

Under load transient condition(heavy load to light load), V_{FB} will drop to lower than 1.4V, thus the PWM drive signal will be stopped, and there is no more energy transferred due to no switching. Therefore, the IC supply voltage (VCC) may drop to the UVLO (off) threshold and the system may enter the unexpected restart mode (as shown in Figure 9).

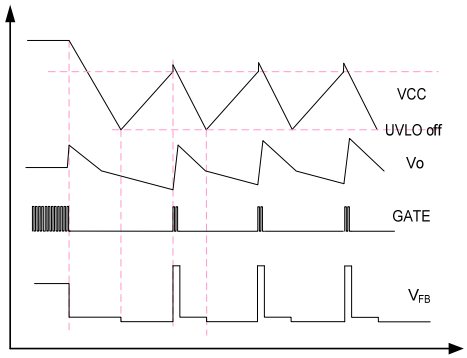


Figure 9. Load Transient without VCC Maintain

To avoid this situation, the AP3105NX holds a so-called VCC maintain mode which can supply energy to VCC when VCC decreases to a setting threshold (10.1V), the VCC maintain comparator will

output a driver signal to make the system switch and provide a proper energy to VCC pin. When VCC increases to 10.6V, the gate signal will be stopped (as shown in Figure 10).

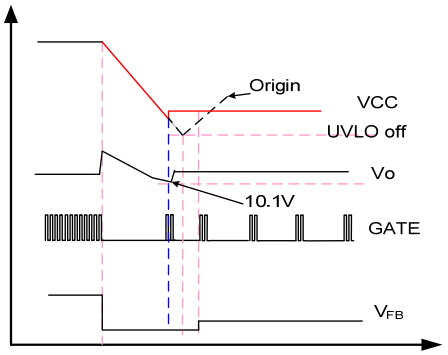


Figure 10. Load Transient with VCC Maintain

The VCC maintain function will benefit dynamic transition (full load to light load). It can simplify system loop design. Also this mode is designed for reducing startup resistor loss and it will achieve a better standby performance with low value VCC capacitor and larger startup resistor.

To avoid the "VCC maintain mode" triggering in normal operating condition, it is suggested to design the VCC value higher than VCC maintain threshold under minimum load condition(usually at no load). The unexpected processing of VCC maintain mode under no load is shown in Figure 11.

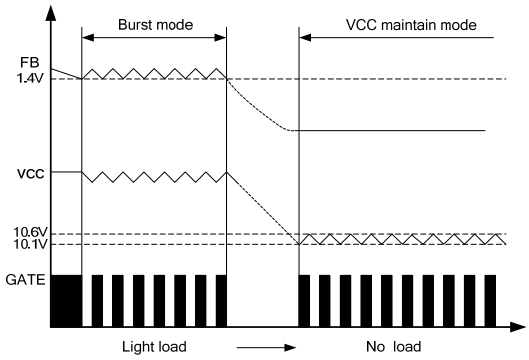


Figure 11. VCC Maintain Mode Triggered @No Load

2.7 Surge Immunity Enhanced Solutions

In some applications, a strict surge test specification is required. For instance, common mode surge is over 6kV.

When a large surge voltage is added across the primary and secondary sides of the system, the general Ground may be raised higher, thus a current will be thrown out from some pins and damage the internal circuit.

If CTRL pin is not floating, R2 is recommended 100kΩ to 200kΩ for eliminating the abnormal current. Also R1 is suggested 300Ω at least and over 1kΩ if it is needed to pass 6kV CM spec.

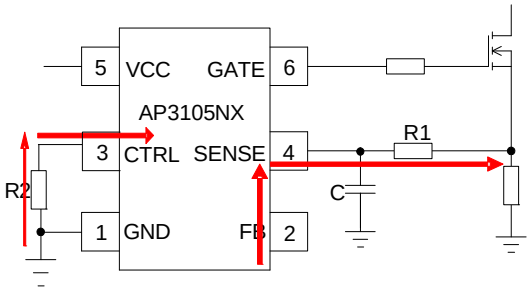
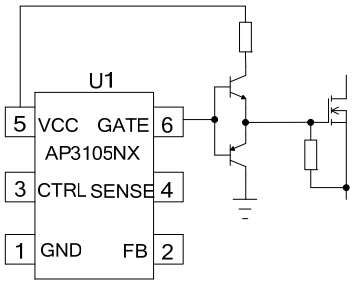


Figure 12. Surge Immunity Circuits

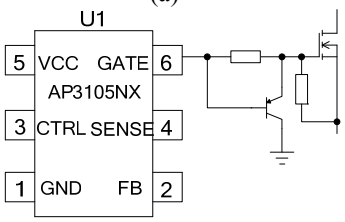
2.8 MOSFET Driver Circuit

A MOSFET consists of many small MOSFET cells. For these cells have different distances from the GATE pin, insufficiency turn on/off speed will cause partial over-heating of the MOSFET and lower efficiency.

For system which is over 36W, driver circuit with a push-pull as shown in Figure 13 (a) is recommended or at least using Figure 13 (b) with a single pull-down transistor. Figure 13 (c) can be applied in system that is less than 36W.



(a)



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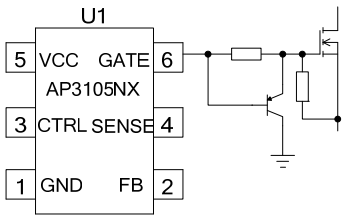


(c)

Figure 13. Driver Circuit

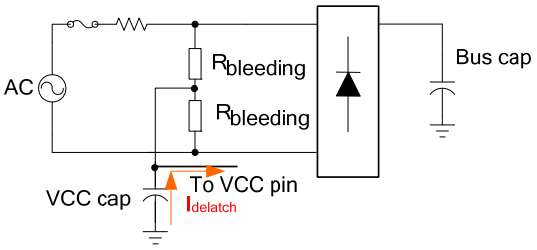
2.9 Start-up Circuit

A usual applied start-up circuit takes start-up current from Bus cap (as shown in Figure 14 (b)), but the de-latch time of some protection mode when AC turns off will be long for the Bus cap still charges the VCC cap.

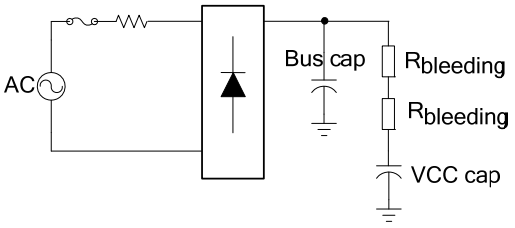
Another start up circuit (as shown in Figure 14 (a)) is connected ahead of bridge rectifier. It could reset latch mode protection quickly for VCC cap have a single larger discharge current. The de-latch time is equal to:

$$t_{delatch} = \frac{C_{VCC} \times \Delta v}{I_{delatch}} = \frac{C_{VCC} \times 3.3V}{13.6\mu A}$$

C_{VCC} is the VCC cap's value, $I_{delatch}$ is the current that the IC consumed under protection mode. Δv is the error of UVLO threshold and de-latch threshold. Thus, a shorter de-latch time needs a smaller VCC cap value.



(a)



(b)

Figure 14. Start-up Circuit

3. Standby Power Loss Reduction

Some methods are recommended here for reducing the standby power loss.

3.1 X-capacitor and X-resistor

A good quality X-capacitor will be helpful to save the standby power, and a low value X-cap could also decrease the X-cap loss. According to IEC 60950, for the X-cap exceeding 0.1μF, the voltage will be decayed to 37% of its original value during an interval equal to one constant, and after calculating, the RC value is determined by the formula "R× C<1".

Therefore, for a low value X-cap, a higher value X-resistor could be used, and the losses on X-resistor will be reduced.

3.2 Current Sampling Resistor

The value of current sampling resistor could affect the standby power. A lower value CS resistor is good for low standby power. But it also has effects on the OLP result: a lower value CS resistor will make a larger OLP point.

3.3 "SENSE" Pin RC Value

The value of "SENSE" pin RC could also affect the standby power. A larger value of RC can make the I_{PEAK} sense signal and the voltage on "FB" pin smaller. A smaller voltage on "FB" pin will result in a lower operating frequency. It is good for achieving low standby power, but it will also make the OLP point larger.

3.4 The Output Voltage Dividing Resistor

The value of output voltage dividing resistor should be as high as possible, but the maximum value of the resistor connected to GND (R17 in Figure 18) should not exceed 15KΩ.

3.5 Primary RCD Clamp Circuit

To get a better standby power, the RCD clamp circuit could be replaced by a Transient Voltage Suppressor (TVS) and a diode (Figure 15). The advantage of the TVS clamp is that it only conducts when necessary and it is independent of the switching frequency.

Compared to a RCD clamp, it reduces no-load power but increases costs and EMI. Besides, a lower value of RC is contributed to standby power, while the voltage stress on MOSFET should be in the spec.

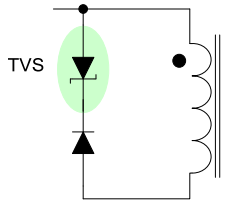


Figure 15. Clamp Circuit with TVS

4. SENSE Pin RC Filter Chosen Principle

Table 4 shows the effects with different RC value on SENSE pin. A proper value of R_F is 680Ω to 2.5KΩ while the C_F value is 33pF to 330pF. Figure 16 shows the results of OCP line regulation with different RC value.

	Standby Loss	OCP Line Regulation	FOCP Trigger	V_{DS} & I_{PEAK} @startup
Larger R*C	less	worse	Not easily	
Lower R*C	larger	better	More easily	
Larger R_F				lower
Lower R_F				higher

Table 4. Affects of RC Value

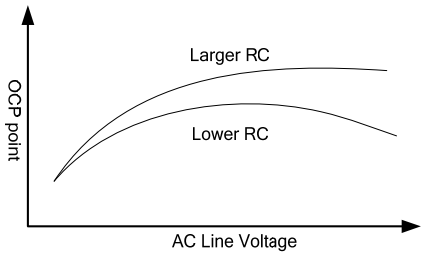


Figure 16. OCP Regulation with Difference

5. PCB Layout Consideration

5.1 High Frequency Loop Consideration

As shown in Figure 17, there are four major high frequency current loops:

1. The current path from bulk capacitor, transformer, MOSFET, R_{CS} returning to bulk capacitor

2. The path from GATE pin, MOSFET, R_{CS} returning to the ground of IC

3. The RCD clamp circuit is a high frequency loop

4. Transformer, rectifier diode, and output capacitor is also a high frequency current loop

The loops must be as short as possible to decrease the radiate area for a better EMI, and if the MOSFET and Schottky diode have heat sink, the heat sink should be connected to their ground separately.

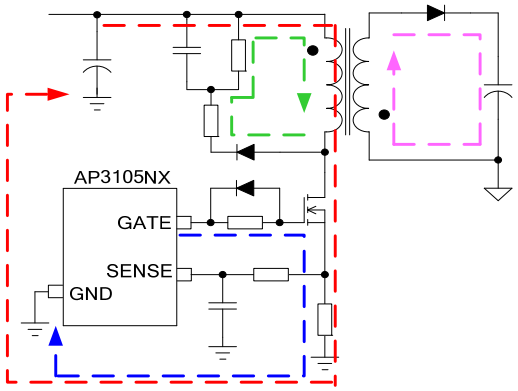


Figure 17. High Current Loop

In addition, the IC should not be placed in the loop of switching power trace, and in some applications, the power ground could be crossed over by the control signal (low current and low voltage), but the switching power trace with pulsating high voltage should not be crossed over.

5.2 ESD Consideration

Electro-Static Discharge (ESD) is an important testing item for switching power supply. The system's ability for bearing the test could be improved by designing a path to release the electric charge to the ground.

As shown in Figure 18, the red line represents the proposed path to release the charge. The copper tips for discharging should be placed between primary side and secondary side, but the distance between two copper tips should be consistent with the requirement of the safety specification.

The input common mode filter and differential mode filter will affect the effect of transient discharging, so the copper tips should be added and their distance should be as short as possible. Another way is placing a resistor paralleled with the inductor to replace the copper tip and the resistor's value is about 1kΩ to 5kΩ. A smaller resistor is helpful to ESD but has bad effects on lighting surge.

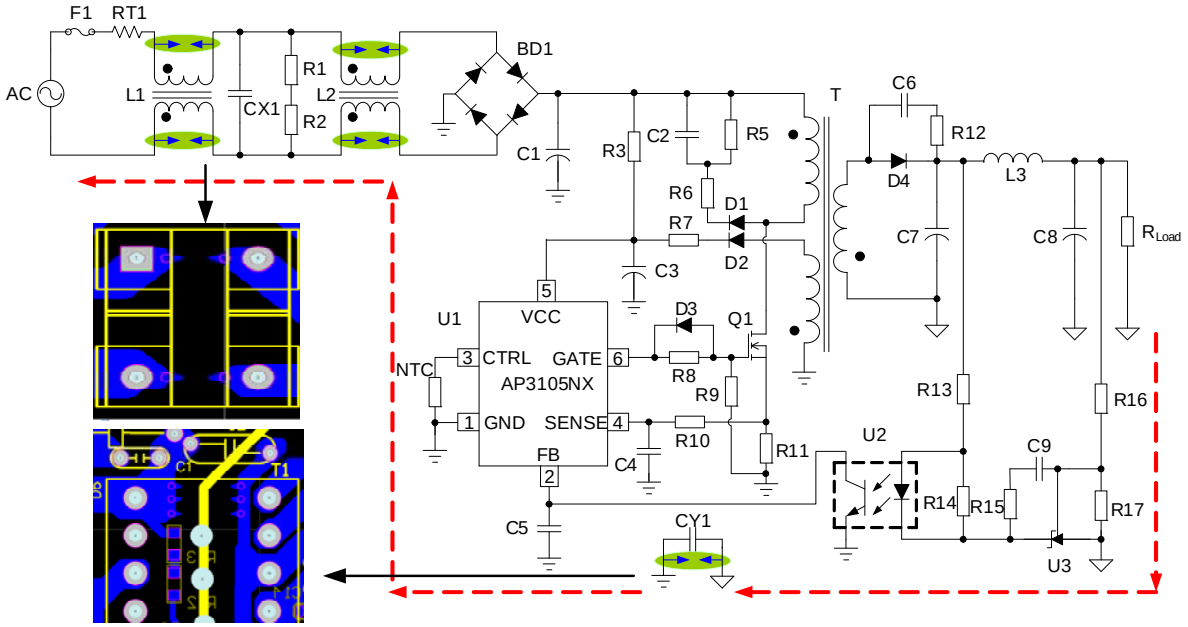


Figure 18. The Path of Release Charge of ESD

5.3 Layout Consideration for Surge Test

Figure 19 shows a circuit example which is under lightning surge test. The surge signal crosses between input line cable and secondary earth ground. Possible surge current paths I1, I2 and I3 are shown in the diagram.

I2 is the current which passes through YCAP, and I3 is the current which passes through transformer from secondary GND to primary Aux winding GND. I2 and I3 may interfere IC GND if YCAP GND and AUX GND have a common trace with IC GND on the layout. I1 is the current which passes through transformer from secondary GND to primary bulk CAP. I1 normally will not influence IC because there is a large resistor between IC pin and bulk CAP terminal.

A proper "Ground" layout is a so-called "Star" connection which is highly recommended for primary GND layout. As shown in Figure 19, the GND of MOSFET, Auxiliary winding GND, YCAP GND and control IC GND are separated, and finally connected together on bulk capacitor ground. The width of these grounds should be kept as large as possible.

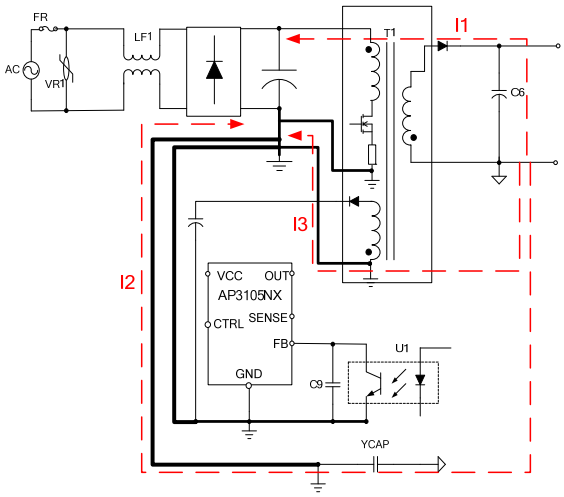


Figure 19. Ground Layout for Surge Test Immunity

6. Demo Design of 12V 2A Adaptor

12V 2A DEMO using flyback topology is designed, and the system specification is shown as follows:

- Output voltage and current: 12V/2A
- Input voltage range: 90Vac to 265Vac

Table 5 shows the demo board components list. Figure 20 shows the application circuit schematic.

Item	Type	Item	Type	Item	Type
C2	102/1KV, ceramic	D10	VF30100S, TO220	R_{S1}, R_{S2}	1.6Ω, 1206
C3	17μF/400V, AL CAP	R1	9.1R, 1206	L4	220μH, 0510
C4	3.3μF, AL CAP	R2	SHORT	U1	817C
C5	680nF, 0603, ceramic	R4	1K, 0603	U2	AP3105NA, BCD
C6	1000μF/16V, KZJ	R5	0.022R, 0805	U3	AP4320, BCD
C7	17μF/400V, AL CAP	R7	10Ω, 0805	T1	PQ20, 1600μH
C9, C13	2.2nF, 0805, ceramic	R9	10K, 0603	Q1	11N60, TO220, INFINEON
C10	1nF, 0603, ceramic	R10, R14	5.6K, 0603	LF1	60μH, MOROTA
C11	33pF, 0603, ceramic	R11	200K, 1206	FR	1A/250V
C12	YCAP, 102	R12	8.2K, 0603	VR1	VARISTOR, 10K621
C20	2.2μF, 0603, ceramic	R13	2.4K//18K, 0603	BRIDGE1	KBP206
D1, D5	FR107, 0805	R15	220Ω, 0603		
D2	1N4148, 0805	R18, R21	2.5M, 1206		

Table 5. BOM of Demo Board (12V/2A)

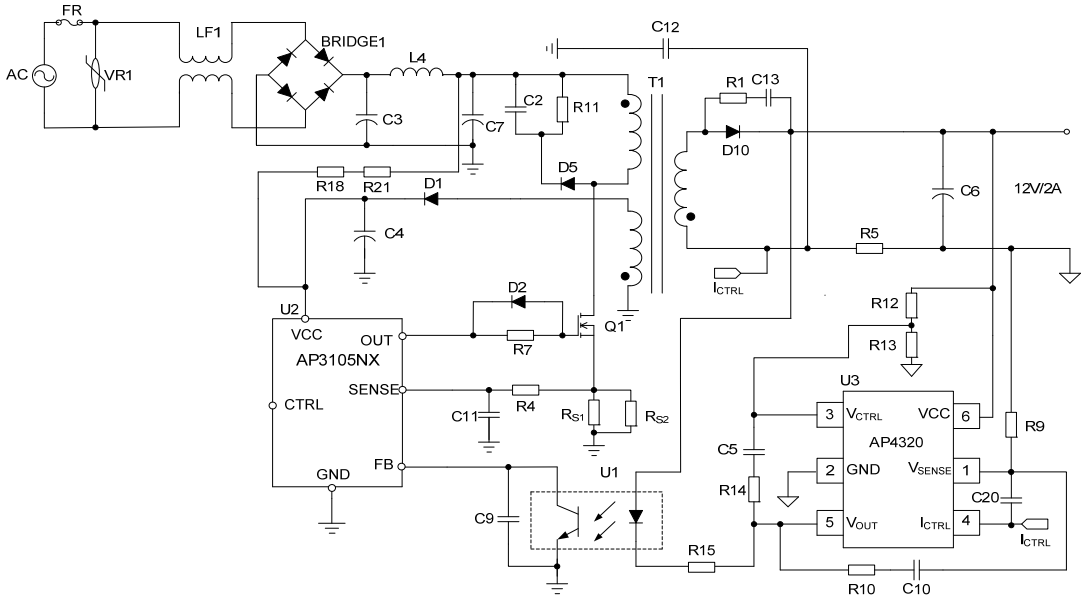


Figure 20. Application Circuit Schematic

Table 6 shows the standby loss test result and Table 7 shows the efficiency test result with no output cable.

V_{IN}	115V/50Hz	150V/50Hz	230V/50Hz	264V/50Hz
P_{STB}	42mW	46mW	63mW	83mW

Table 6. Standby Loss Test Result

	0.5A	1A	1.5A	2A	AV
$115V_{IN}$	88.6%	88.7%	88.9%	88.3%	88.6%
$230VI_N$	87.2%	88%	88.6%	88.2%	88%

Table 7. Efficiency with PCB Terminal