

## Application Notes for AP3772 System Solution

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### 1. Introduction

The AP3772 uses Pulse Frequency Modulation (PFM) method to realize Discontinuous Conduction Mode (DCM) operation for Flyback power supplies. The operating principle of PFM is different with Pulse Width Modulation (PWM), so the design of transformer is also different.

The AP3772 can provide accurate constant voltage (CV), constant current (CC) regulation with Primary Side Regulation (PSR) structure. It uses internal line compensation and cable compensation to reduce the

number of external system components. Fixed cable compensation is used in different IC versions to adapt the different voltage drop on output cable and good CV regulation is achieved. Besides, audio noise is reduced by the creative audio suppression technique.

The AP3772 is designed for driving bipolar transistor in Flyback converter, with more driving current of about 40mA. With system parameters properly designed, AP3772 can achieve standby power less than 150mW.

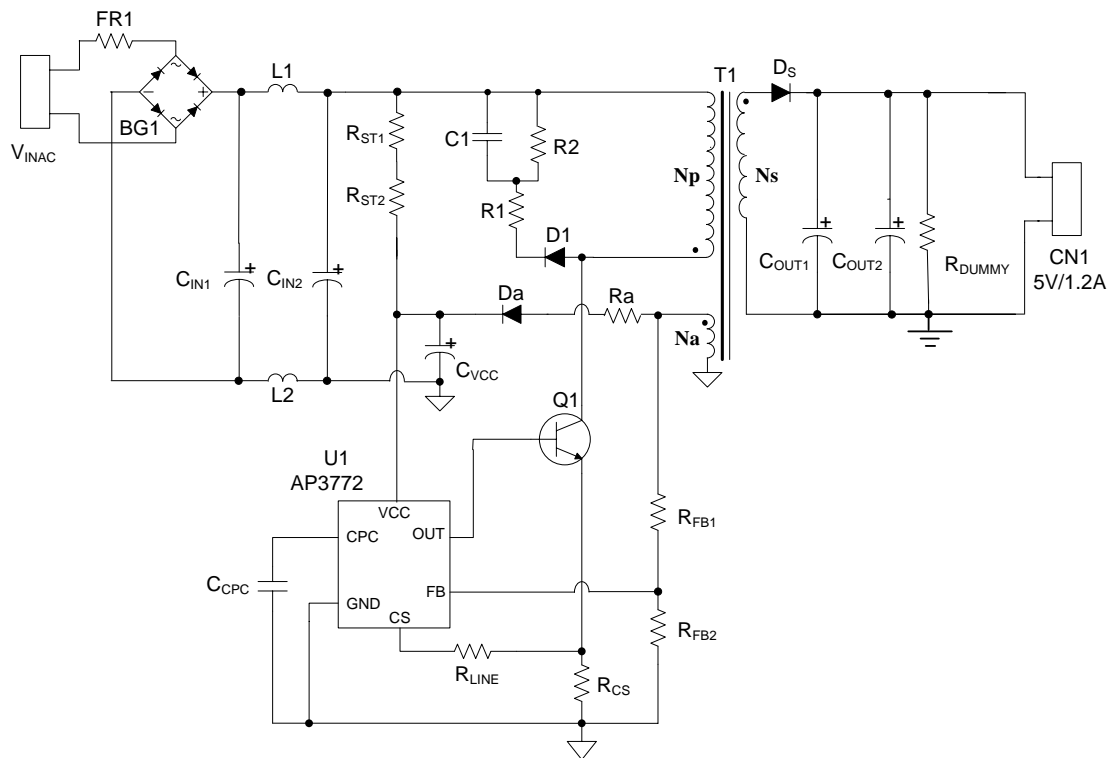


Figure 1. Typical Application Circuit of AP3772

Figure 1 is the typical application circuit of AP3772, which is a conventional Flyback converter with a 3-winding transformer---primary winding ( $N_p$ ), secondary winding ( $N_s$ ) and auxiliary winding ( $N_a$ ). The auxiliary winding is used for providing  $V_{CC}$  supply voltage for IC and sensing the output voltage feedback signal to FB pin.

Figure 2 shows the typical waveforms which demonstrate the basic operating principle of AP3772 application. And

the parameters are defined as following.

$V_{dri}$ ---The driving signal of primary power switch

$I_p$ ---The primary side current

$I_s$  ---The secondary side current

$I_{PK}$ ---Peak value of primary side current

$I_{PKS}$ ---Peak value of secondary side current

$V_{SEC}$ ---The transient voltage at secondary winding

$V_s$ ---The stable voltage at secondary winding when

rectification diode is in conducting status, which equals the sum of output voltage  $V_{OUT}$  and the forward voltage drop of diode

$V_{AUX}$ ---The transient voltage at auxiliary winding

$V_A$ --- The stable voltage at auxiliary winding when rectification diode is in conducting status, which equals the sum of voltage  $V_{CC}$  and the forward voltage drop of auxiliary diode

$t_{SW}$ ---The period of switching frequency

$t_{ONP}$  ---The conduction time when primary side switch is "ON"

$t_{ONS}$  ---The conduction time when secondary side diode is "ON"

$t_{OFF}$  ---The dead time when neither primary side switch nor secondary side diode is "ON"

$t_{OFFS}$  --- The time when secondary side diode is "OFF"

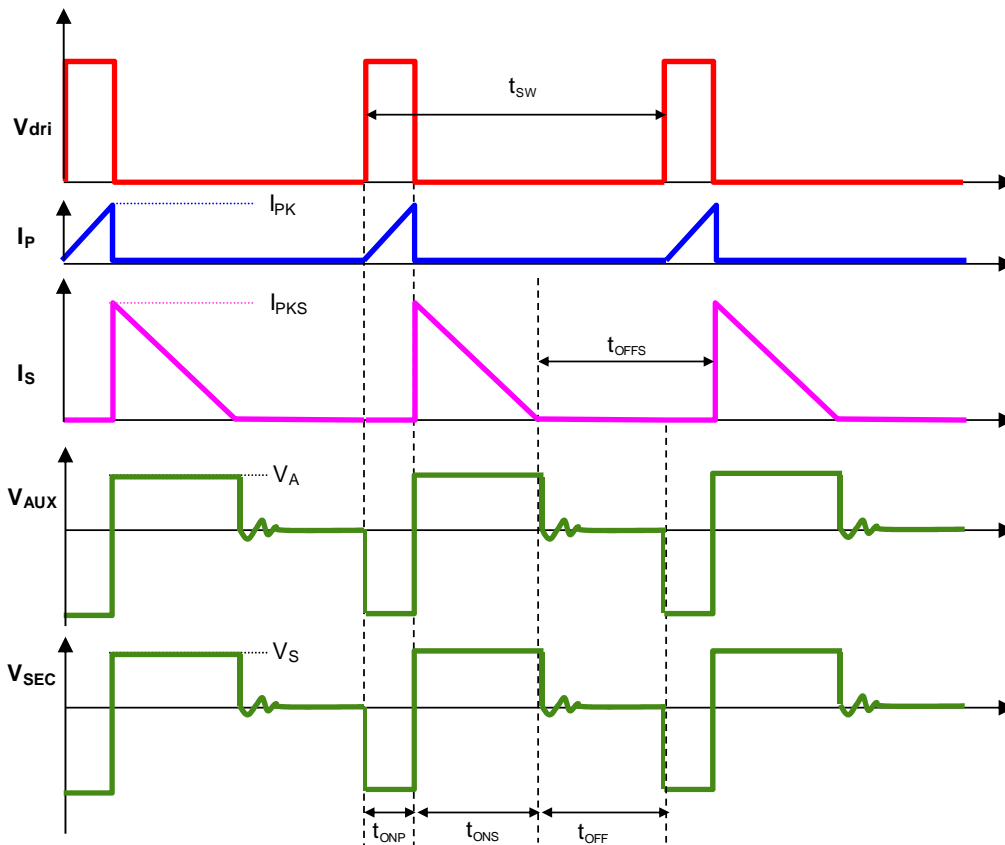


Figure 2. Operation Waveforms of Flyback PSR Control System

## 2. Guideline of System Design

1. Low Standby Power Design
2. Switching Frequency Design
3. Transformer and Power Devices Design
4. Feedback Resistors Design
5. Line Compensation Design
6. Cable Compensation Design

### 2.1 Low Standby Power Design

In order to achieve low standby power, AP3772 decreases the minimum operating voltage. And the startup resistors  $R_{ST1}+R_{ST2}$  should be high enough to further lower the power loss. However, there is a tradeoff between low standby power  $P_{ST}$  and small startup time  $t_{START}$ , which is

$$t_{START} = (R_{ST1} + R_{ST2}) \cdot C_{VCC} \cdot V_{TH\_ST} / V_{INDC\_MIN} \quad (1)$$

Where  $V_{TH\_ST}$  is the Startup Threshold of  $V_{CC}$ , and  $V_{INDC\_MIN}$  is the rectified DC voltage from the lowest AC input.

Besides, the selection of dummy load resistor is a tradeoff between standby power and I-V curve. The recommended value of dummy load resistor  $R_{DUMMY}$  is 4.7k $\Omega$  to 10k $\Omega$  for an application with 5V output voltage.

### 2.2 Switching Frequency Design

As we know, in DCM Flyback converter, the stored energy of primary side will be transferred to secondary side at the time when the primary switch is turned off. And assume the current transfer efficiency from primary to secondary is  $\eta_i$ , then

$$I_{pks} = I_{pk} \cdot N_{PS} \cdot \eta_i \quad (2)$$

Here,  $N_{PS}$  is the turn ratio of primary winding to secondary winding.

It is obvious in Figure 2 that the output current “ $I_O$ ” is the average current of secondary side “ $I_S$ ”,

$$I_O = \frac{1}{2} I_{pks} \cdot \frac{t_{ONS}}{t_{SW}} \quad (3)$$

Then,

$$I_O = \frac{1}{2} I_{pk} \cdot N_{PS} \cdot \eta_i \cdot \frac{t_{ONS}}{t_{SW}} \quad (4)$$

Always voltage of CPC pin ( $V_{CPC}$ ) is determined by,

$$V_{cpc} = V_{DD} \cdot \frac{t_{ONS}}{t_{SW}} \quad (5)$$

Here  $V_{DD}$  is a constant voltage generated by IC. Then,

$$\frac{V_{cpc}}{I_O} = \frac{2 \cdot V_{DD}}{N_{PS} \cdot \eta_i \cdot I_{PK}} \quad (6)$$

If  $\eta_T$  is efficiency of power transmission from transformer primary to the output, then

$$P_O = V_O \cdot I_O = \frac{1}{2} \cdot L_P \cdot I_{pk}^2 \cdot f_{SW} \cdot \eta_T \quad (7)$$

Where,  $f_{SW}$  is the switching frequency. So,

$$\frac{f_{SW}}{I_O} = \frac{2 \cdot V_O}{L_P \cdot I_{pk}^2 \cdot \eta_T} \quad (8)$$

When voltage at the sense resistor reaches the reference voltage set by AP3772, the switch will be turned off and primary current reaches its maximum value,

$$I_{PK} = \frac{V_{cs\_ref}}{R_{cs}} \quad (9)$$

When the constant reference  $V_{CS\_REF}$  is used, the peak current  $I_{PK}$  is constant. From formula (6) and (8), it is obvious that  $V_{CPC}$  and  $f_{SW}$  increases linearly with the output current  $I_O$ .

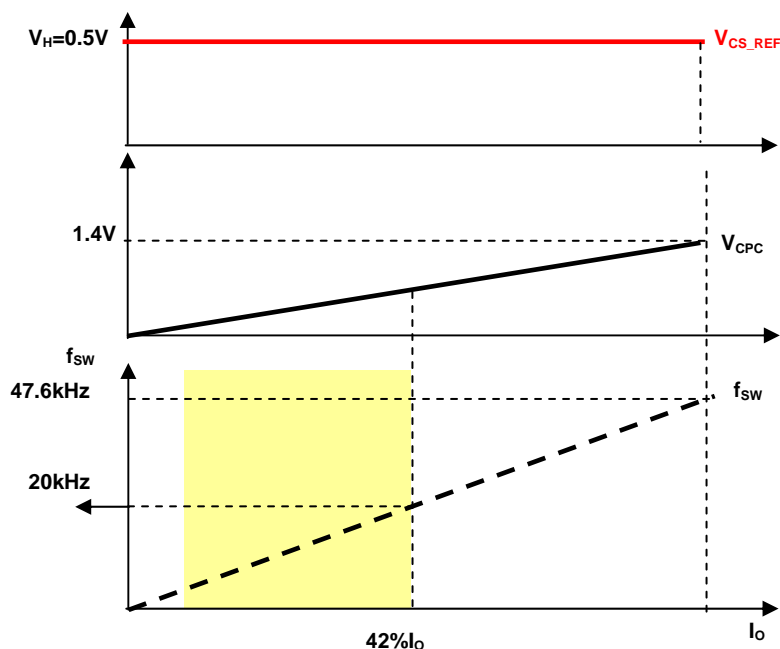


Figure 3. Relationship Between  $V_{CPC}$ ,  $f_{SW}$  and  $I_O$  at Constant Peak Current Mode

In AP3772, in order to realize audio noise suppression, two-segmented of current reference voltage  $V_{CS\_REF}$  is used. The reference is about 0.5V when  $I_O \geq 42\% * I_{O\_MAX}$  and is

decreased to 0.5V/1.5 when  $I_O < 42\% * I_{O\_MAX}$ , as follows in Figure 4.

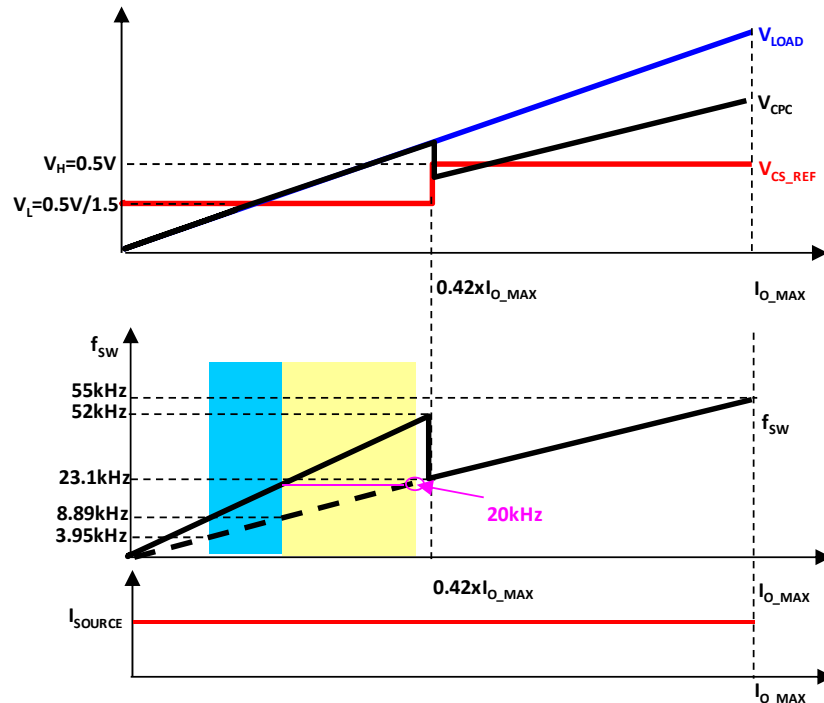


Figure 4. Relationship Between  $V_{CPC}$ ,  $f_{SW}$  and  $I_O$  at Variable Peak Current Mode

Then from formula (6) and (8), we can see the  $V_{CPC}$  and  $f_{SW}$  both has a leap at about 42% of maximum load. At the leap point, if the peak current is decreased by 1.5 times, the voltage of CPC pin at low  $I_{PK}$  will be increased to 1.5 times,

and the switching frequency  $f_{SW}$  at low  $I_{PK}$  will be increased to  $1.5^2$  times. So the load range in audio is largely narrowed.

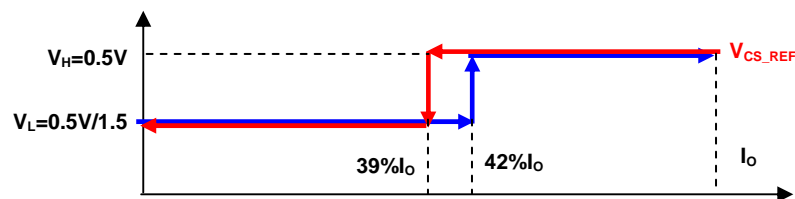


Figure 5. Hysteresis at Conversion Between Low  $I_{PK}$  and High  $I_{PK}$

In order to avoid unstable operation, a hysteresis is added at the conversion between low  $I_{PK}$  and high  $I_{PK}$ . Considering the relationship between audio noise and flux density of transformer,  $\Delta B \leq 2500$  gauss is better for audio noise suppression.

the AP3772 can be up to 120kHz. But this is only the limit of the IC; the finally designed maximum switching frequency is determined by the tradeoff between the efficiency, mechanical dimensions and thermal performance.

The low limitation of maximum switching frequency is given by audio noise suppression. And the upper limit of

## 2.3 Transformer and Power Devices Design

In the design of AP3772, constant current control function will keep a fixed proportion between on-time  $t_{ONS}$  and off-time  $t_{OFFS}$  of rectifier D1 (in Figure 1) by discharging or charging a capacitor embedded in the IC. The fixed proportion is

$$\frac{t_{ONS}}{t_{SW}} = \frac{1}{2} \quad (10)$$

It is assumed

$$k = \frac{2 \cdot t_{SW}}{t_{ONS}} = 4 \quad (11)$$

Then the output constant-current value  $I_O$  is

$$I_O = \frac{1}{k} \cdot I_{PKS} = \frac{1}{k} \cdot N_{PS} \cdot \eta_i \cdot I_{PK} \quad (12)$$

### 2.3.1 Calculate Turn Ratio of Transformer ( $N_{PS}$ )

The turn ratio of transformer should be designed first, which ensures the power converter operating in DCM within the whole conditions,

$$t_{SW} \geq t_{ONP} + t_{ONS} \quad (13)$$

As we know, if equation (13) is met at minimum input voltage and full load, it can ensure that the power converter operates in DCM in all conditions.

For the primary side current,

$$t_{ONP} = I_{pk} \cdot \frac{L_p}{V_{indc}} \quad (14)$$

Where

$L_p$  is the inductance of primary winding.

$V_{indc}$  is the rectified DC voltage of input.

When  $V_{indc}$  is the minimum value, the maximum  $t_{ONP}$  can be obtained. So,

$$t_{ONP\_MAX} = I_{pk} \cdot \frac{L_p}{V_{indc\_min}} \quad (15)$$

For the secondary side current,  $L_s$  is the inductance of secondary winding,  $V_d$  is the forward voltage of secondary diode.

There is an oscillating signal on FB waveform after secondary Schottky diode current decrease to zero, which is caused by primary inductance and equivalent output capacitance of primary switch. Then some margin is added to  $t_{ONS}$  as

$$t_{ONS} = I_{pks} \cdot \frac{L_s}{V_s} \cdot 1.1 \quad (16)$$

$$V_s = V_o + V_d \quad (17)$$

From formula (4) and formula (16), we can get

$$V_s \cdot I_o = \frac{1}{2} \cdot L_s \cdot I_{pks}^2 \cdot f_{sw} = \frac{1}{2} \cdot \frac{L_p}{N_{PS}^2} \cdot (I_{pk} \cdot N_{PS} \cdot \eta_i)^2 \cdot f_{sw} = \frac{1}{2} \cdot L_p \cdot I_{pk}^2 \cdot f_{sw} \cdot \eta_i^2 \quad (18)$$

Then,

$$t_{SW} = \frac{L_p \cdot I_{pk}^2 \cdot \eta_i^2}{2 \cdot V_s \cdot I_o} \quad (19)$$

$t_{ONP}$ ,  $t_{ONS}$  and  $t_{SW}$  in (13) are replaced with (15), (16) and (19), then

$$\frac{L_p \cdot I_{pk}^2 \cdot \eta_i^2}{2 \cdot V_s \cdot I_o} \geq I_{pks} \cdot \frac{L_s}{V_s} \cdot 1.1 + I_{pk} \cdot \frac{L_p}{V_{indc\_min}} \quad (20)$$

Relationship between inductance of primary side and secondary side is,

$$L_s = \frac{L_p}{N_{PS}^2} \quad (21)$$

At full load, the system will work in the boundary of CC regulation.  $I_o$  can be given by formula (12), the following can be obtained,

$$N_{PS} \leq N_{PS\_MAX} = \frac{V_{indc\_min} \cdot \eta_i}{V_s} \cdot \left( \frac{k}{2} - 1.1 \right) \quad (22)$$

Then designed turns ratio  $N_{PS}$  should be no more than  $N_{PS\_MAX}$  defined in formula (22).

### 2.3.2 Check Stress Voltage of Primary Side Switch and Reverse Voltage of Secondary Diode

If  $N_{PS}$  is fixed by customer according to design step 2.3.1, real stress voltage of primary side switch and reverse voltage of secondary diode can be calculated.

The maximum stress voltage of primary side switch is,

$$V_{ds\_switch} = V_{dc\_spike} + V_{indc\_max} + \frac{V_S \cdot N_P}{N_S} \quad (23)$$

Be careful that the value of  $V_{dc\_spike}$  is determined by the snubber circuit design.

Maximum reverse voltage of secondary side,

$$V_{dr} = V_S + \frac{V_{indc\_max} \cdot N_S}{N_P} \quad (24)$$

For Flyback converter design, higher turns ratio  $N_{PS}$  brings higher stress voltage of primary side switch, higher transforming efficiency, and the lower reverse voltage of secondary diode. Finally, in design of turns ratio  $N_{PS}$ , formula (22), (23) and (24) should be totally considered.

### 2.3.3 Calculate the Peak Current of Primary Side and Current Sensed Resistor ( $I_{PK}$ & $R_{CS}$ )

$I_{PK}$  can be calculated by the output current.

$$I_{pk} = \frac{k \cdot I_O}{N_{PS} \cdot \eta_i} \quad (25)$$

In AP3772, 0.5V is an internal reference voltage. If the sensed voltage  $V_{CS\_REF}$  reaches 0.5V, the power switch will shut down and  $t_{ONP}$  will be ended.

So  $R_{CS}$  can be obtained by formula (9) and selected with a real value from the standard resistor series. We recommended using 1% tolerance resistors for  $R_{CS}$ . After  $R_{CS}$  is selected,  $I_{PK}$  should be modified based on the selected  $R_{CS}$ .

### 2.3.4 Calculate the Inductance of Primary Side--- $L_P$

The primary side inductance  $L_P$  is relative with the stored energy.  $L_P$  should be big enough to store enough energy, so that  $P_{O\_MAX}$  can be obtained from this system.

According to formula (18), the output power can be given by,

$$P_S = V_S \cdot I_O = \frac{1}{2} \cdot L_P \cdot I_{pk}^2 \cdot f_{SW} \cdot \eta_i^2 \quad (26)$$

Where,  $f_{SW}$  was set by the user based on definite requirement. Then,  $L_P$  can be gotten by,

$$L_P = \frac{2 \cdot P_S}{I_{PK}^2 \cdot f_{SW}} \cdot \frac{1}{\eta_i^2} \quad (27)$$

### 2.3.5 Calculate the Turns of Primary, Secondary and Auxiliary ( $N_P$ , $N_S$ , $N_A$ )

The turns of primary winding,

$$N_P = \frac{L_P \cdot I_{PK}}{Ae \cdot \Delta B} \geq \frac{L_P \cdot I_{PK}}{Ae \cdot B_{max}} \quad (28)$$

As  $N_{PS}$  and  $N_P$  are fixed, we can get  $N_S$  by

$$N_S = \frac{N_P}{N_{PS}} \quad (29)$$

Turns of auxiliary winding is,

$$N_A = \frac{N_S \cdot V_A}{V_S} \quad (30)$$

### 2.3.6 Check the Maximum Duty Cycle of Primary Side

After turn ratio of primary side and secondary side is designed, the maximum duty cycle of primary side at low line voltage can be calculated again.

Considering the Volt-second balance between magnetizing and de-magnetizing, the formula of duty cycle is

$$D_{max} = \frac{(V_O + V_d) \cdot N_{PS}}{V_{indc} \cdot \eta_i} \cdot \frac{t_{ons}}{t_{sw}} \quad (31)$$

### 2.3.7 Check Reverse Voltage of Auxiliary Diode

If  $N_P$  and  $N_A$  is fixed according to design step 2.3.5, real reverse voltage of auxiliary diode can be calculated by formula (32).

$$V_{dar} = V_A + \frac{V_{indc\_max} \cdot N_A}{N_P} \quad (32)$$

## 2.4 Feedback Resistors Design

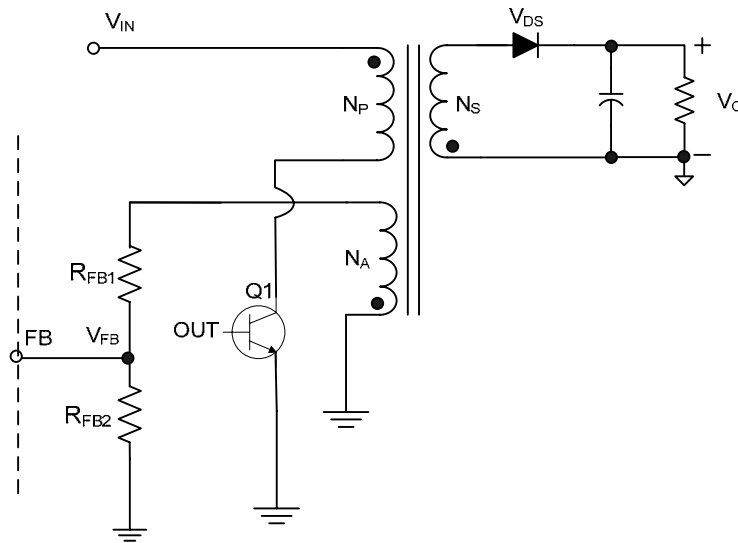


Figure 6. Feedback Resistors Circuit

From above Figure 6,

$$V_o = V_{FB} \cdot \frac{(R_{FB1} + R_{FB2})}{R_{FB2}} \cdot \frac{N_s}{N_a} - V_D \quad (33)$$

$$\frac{R_{FB1}}{R_{FB2}} = \frac{V_o + V_D}{N_s \cdot V_{FB}} \cdot N_a - 1 \quad (34)$$

Through adjusting  $R_{FB1}$  and  $R_{FB2}$ , a suitable output voltage can be achieved. The recommended values of  $R_{FB1}$  and

$R_{FB2}$  are within  $5k\Omega$  to  $100k\Omega$ .

## 2.5 Line Compensation Design

The internal line compensation function in AP3772 is shown in Figure 7. S1 is closed when the primary switch is “ON”. The line voltage can be detected from the FB pin. The detected voltage internally compensates the peak current. So the line compensation is determined by  $R_{LINE}$ . In different applications, the value of  $R_{LINE}$  is different.

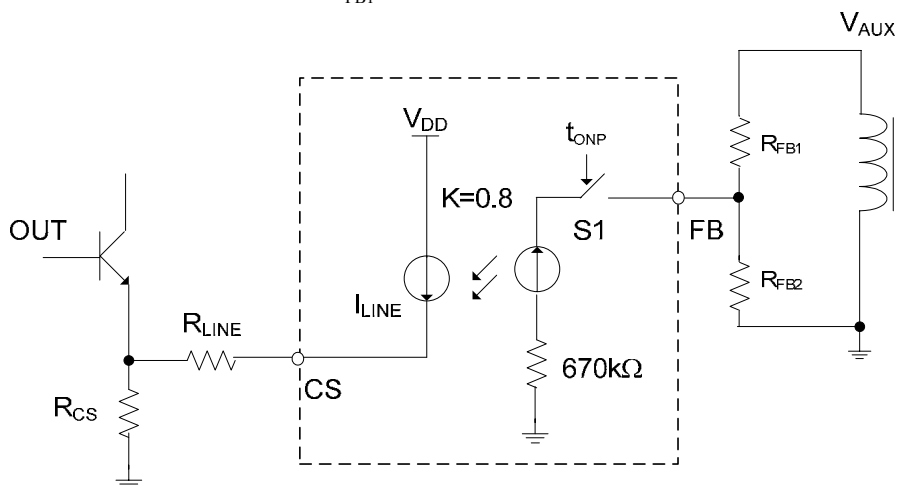


Figure 7. Line Compensation Circuit

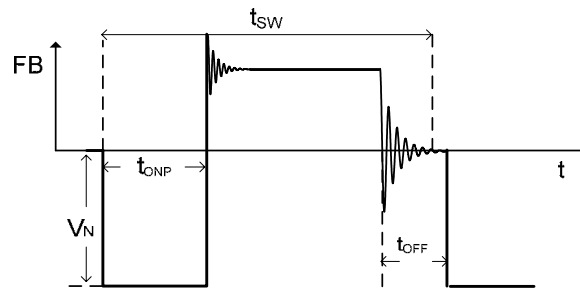


Figure 8. Waveform of FB Pin

The negative voltage  $V_N$  of FB pin (in Figure 8) is linear to line voltage. The AP3772 samples  $V_N$  to realize the line compensation.

$$V_N = V_{indc} \cdot \frac{N_A}{N_P} \cdot \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \quad (35)$$

The compensated voltage of line compensation ( $V_{CS\_LINE}$ ) can be calculated by the following formula,

$$V_{CS\_LINE} = V_N \cdot \frac{1}{670k} \cdot 0.8 \cdot R_{LINE} \quad (36)$$

This is designed to compensate the additional voltage of  $V_{CS}$  introduced by  $t_{delay}$ , which is the delay time of internal drivers of IC and primary side switch.

$$V_{delta} = V_{indc} \cdot \frac{t_{delay}}{L_p} \cdot R_{cs} \quad (37)$$

Then  $R_{LINE}$  can be adjusted to achieve excellent line

regulation of output current.

$$R_{LINE} = \left( \frac{t_{delay}}{L_p} \cdot R_{cs} \right) / \left( \frac{N_A}{N_P} \cdot \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \cdot \frac{0.8}{670k} \right) \quad (38)$$

## 2.6 Cable Compensation Design

Three versions of IC are designed to meet different requirement for cable voltage compensation. As we know, an increase voltage at  $V_{FB}$  ( $\Delta V_{FB\_CABLE}$ ) will introduce an increase voltage at  $V_{OUT}$  ( $\Delta V_{OUT\_CABLE}$ ), which is a linear function of the output load ( $I_{OUT}$ ). Then in application of AP3772, CPC pin detects the load information and a corresponding delta voltage is added to  $V_{FB}$  to compensate the voltage drop at output cable.

As defined in datasheet below, for example, in AP3772A, there is a total voltage increase of 6% at  $V_{FB}$  when the output is at full load ( $I_{OUT\_MAX}$ ). And if the output is at 10%\* $I_{OUT\_MAX}$ , the increase voltage of  $V_{FB}$  is 0.6%. Proper version of IC can be chosen according to the resistance of the output cable.

CABLE COMPENSATION SECTION						
Cable Compensation Voltage	$\frac{\Delta V_{FB\_CABLE}}{V_{FB}} \%$	AP3772A	5	6	7	%
		AP3772B	2	3	4	%
		AP3772C		0		%

Assume

$$\Delta V_{FB} \% = \frac{\Delta V_{FB\_CABLE}}{V_{FB}} \quad (39)$$

Then from Figure 6,

$$\Delta V_{OUT\_CABLE} = \Delta V_{FB} \% \cdot V_{FB} \cdot \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \cdot \frac{N_S}{N_A} = I_{O\_MAX} \cdot R_{CABLE} \quad (40)$$

Then after  $\Delta V_{FB} \%$  is calculated, proper version of AP3772 can be chosen accordingly.

$$\Delta V_{FB} \% = I_{O\_MAX} \cdot R_{CABLE} / \left( V_{FB} \cdot \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \cdot \frac{N_S}{N_A} \right) \quad (41)$$

## Design Example (for 5V/1.2A application):

Specification:

Input voltage: 85V<sub>AC</sub> to 265V<sub>AC</sub>

Output voltage @ cable:  $V_{O\_CABLE}=5V$

Output current:  $I_O=1.2A$

Output voltage @ PCB:  $V_O=5.13V$ , (AWG22 Cable, Length of cable=100cm)



Other setting by users:

Switching frequency:  $f_{sw}=65\text{kHz}$

Forward voltage of secondary diode:  $V_d=0.4\text{V}$

Forward voltage of auxiliary diode:  $V_{da}=1.1\text{V}$

$V_{CC}$  voltage:  $V_{CC}=14\text{V}$

Core\_type: RM5 ( $A_e=23.7\text{mm}^2$ ),  $B_{max}<3000\text{GS}$

$V_{dc\_spike}=50\text{V}$  (with snubber circuit)

## Design Steps:

### 1) Calculate turn ratio of transformer ( $N_{PS}$ )

$$N_{PS} \leq N_{PS\_MAX} = \frac{V_{indc\_min} \cdot \eta_i}{V_S} \cdot \left(\frac{k}{2} - 1.1\right) = 15.8 \quad (42)$$

$$V_{indc\_min} = V_{inac\_min} \cdot \sqrt{2} - 40 \quad (43)$$

Considering some margin for Flyback PSR control, we choose  $N_{PS}=15.5$ .

### 2) Check stress voltage of primary side switch and reverse voltage of secondary diode

According to formulas (23) (24) and the selected  $N_{PS}$ , proper power devices could be chosen.

$$V_{ds\_switch} = V_{dc\_spike} + V_{indc\_max} + \frac{V_S \cdot N_p}{N_S} = 510\text{V} < 700\text{V} \quad (44)$$

$$V_{dr} = V_S + \frac{V_{indc\_max} \cdot N_S}{N_p} = 29\text{V} < 40\text{V} \quad (45)$$

### 3) Calculate the peak current of primary side and current sense resistor ( $I_{PK}$ & $R_{CS}$ )

$$I_{pk} = \frac{I_{pks}}{N_{PS} \cdot \eta_i} = \frac{k \cdot I_O}{N_{PS} \cdot \eta_i} = 330\text{mA} \quad (46)$$

$$R_{CS} = \frac{V_{CS}}{I_{pk}} = 1.5\ \Omega \quad (47)$$

### 4) Calculate the inductance of primary side--- $L_P$

$$L_P = \frac{2 \cdot V_S \cdot I_O}{I_{PK}^2 \cdot f_{SW} \cdot \eta_i^2} = 1.9\text{mH} \quad (48)$$

### 5) Calculate the turns of primary, secondary and auxiliary ( $N_p, N_S, N_A$ )

$$N_p = \frac{L_P \cdot I_{PK}}{A_e \cdot \Delta B} \geq \frac{L_P \cdot I_{PK}}{A_e \cdot B_{max}} = 89.8\text{ T} \quad (49)$$

We choose  $N_p=93\text{T}$

$$N_S = \frac{N_p}{N_{PS}} = 6\text{ T} \quad (50)$$

$$N_A = \frac{N_S \cdot V_A}{V_S} = 16\text{ T} \quad (51)$$

### 6) Check the maximum duty cycle of primary side

The maximum duty cycle of primary side is calculated as following,

$$D = \frac{(V_O + V_d) \cdot N_{PS} \cdot 0.4}{V_{indc} \cdot \eta_i} = 0.49 \quad (52)$$

### 7) Check reverse voltage of auxiliary diode

$$V_{dar} = V_A + \frac{V_{indc\_max} \cdot N_A}{N_p} = 79\text{V} \quad (53)$$

### 8) Feedback Resistors

$$\frac{R_{FB1}}{R_{FB2}} = \frac{V_O + V_D}{N_S \cdot V_{FB}} \cdot N_A - 1 = 2.56 \quad (54)$$

$$R_{FB1}=24.9\text{k}\Omega, R_{FB2}=9.85\text{k}\Omega$$

### 9) Line Compensation Resistors

$$R_{LINE} = \left(\frac{t_{delay}}{L_P} \cdot R_{cs}\right) / \left(\frac{N_A}{N_p} \cdot \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \cdot \frac{0.8}{670\text{k}}\right) = 3.4\text{k}\ \Omega \quad (55)$$

### 10) Cable Compensation Choice

$V_{FB}=4.04\text{V}$ , the same in three versions of AP3772. Then,

$$V_{FB}\% = I_{O\_MAX} \cdot R_{CABLE} / \left(V_{FB} \cdot \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \cdot \frac{N_S}{N_A}\right) = 2.4\% \quad (56)$$

According to datasheet information, AP3772B is a better choice.

$$V_{O\_FL} = V_{O\_NL} + (V_{FB}\% \cdot V_{FB} \cdot \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \cdot \frac{N_S}{N_A}) - I_{O\_MAX} \cdot R_{CABLE} = 5.03\text{V} \quad (57)$$

Where  $V_{O\_NL}=5\text{V}$ . Therefore, the output voltage at cable terminal at full load is a little higher than the voltage at no load.

## Design Results Summary:

1. Maximum peak current of primary side and $R_{CS}$			
$I_{PK}$	330	mA	Peak current of primary side
$R_{CS}$	1.5	$\Omega$	Current sensed resistor
2. Transformer			
$L_p$	1.90	mH	Inductance of primary side
$N_{PS=}$	15.5	Turn ratio of primary and secondary	
$N_p$	93	T	Turns of primary side
$N_s$	6	T	Turns of secondary side
$N_A$	16	T	Turns of auxiliary side
$D_{MAX}$	0.49		Maximum duty cycle of primary side at $V_{INDC}=80V$
3. Primary power switch and diode			
$V_{ds\_switch}$	510	V	Voltage stress of primary power switch
$V_{dr}$	29	V	Maximum reverse voltage of secondary diode
$V_{dar}$	79	V	Maximum reverse voltage of auxiliary diode
4. Voltage feedback resistors			
$R_{FB1}$	24.9k	$\Omega$	Feedback resistor at upside from auxiliary side to FB pin
$R_{FB2}$	9.85k	$\Omega$	Feedback resistor at downside from FB pin to GND
5. Line compensation resistor			
$R_{LINE}$	3.4k	$\Omega$	Line compensation resistor
6. Cable Compensation			
IC version	AP3772B		
$V_{O\_NL}$	5	V	Output cable voltage @ no load
$V_{O\_FL}$	5.03	V	Output cable voltage @ full load

### 3. Summary

In order to get good performance of AP3772, it is important to correctly design standby power, switching frequency, transformer parameters, feedback resistance and line compensation resistance. This application note only gives a

preliminary design guideline about these aspects and considers ideal conditions, so some parameters need to be adjusted slightly on the basis of the calculated results.

#### 4. Application of AP3772 with AP4340

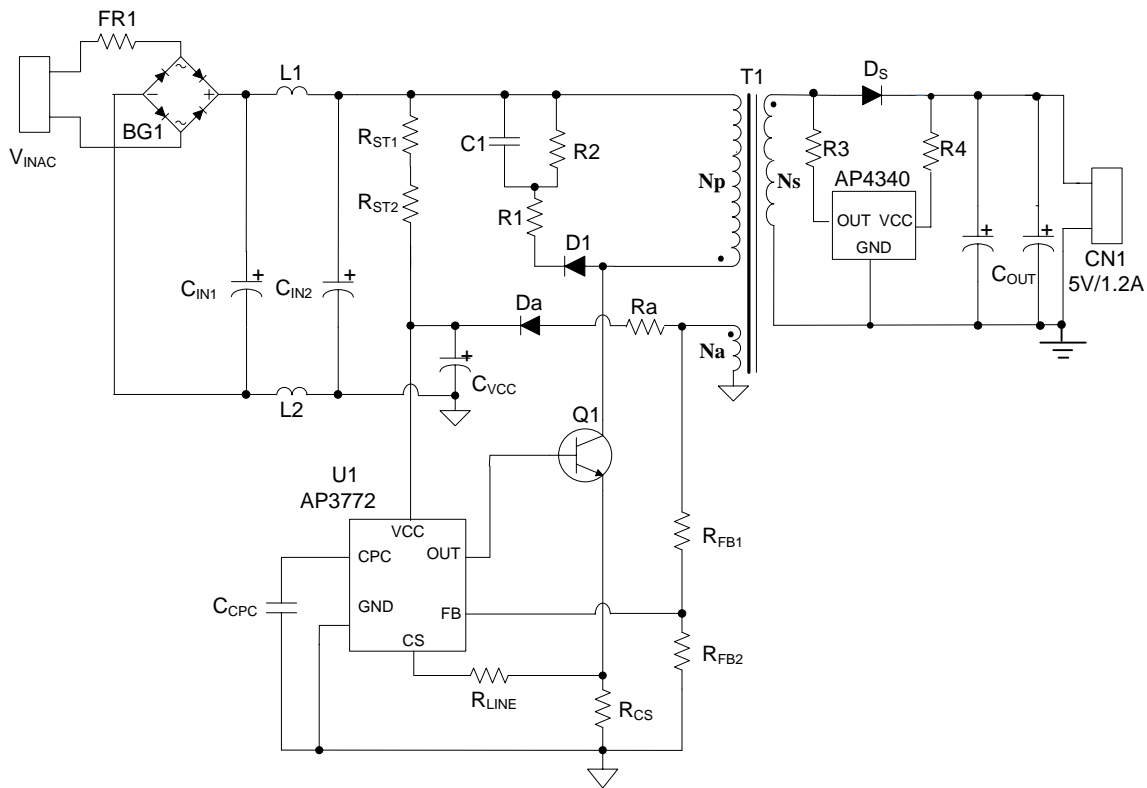


Figure 9. Typical Application Circuit of AP3772 with AP4340

In Primary Side Regulation of AP3772 application, if AP4340 is used at secondary side as the output voltage regulator, excellent dynamic response and low standby power can be achieved. When detecting the output voltage lower than a certain level, the AP4340 outputs periodical signals which will be coupled to auxiliary side and detected by AP3772. By fast response and cooperation, AP4340 and

AP3772 can effectively improve the transient performance for Primary Side Regulation power system. Besides, dummy load is not needed at secondary side and as a result standby power will be decreased. For more detailed operating principles, please refer to Application Note of AP4340 (Application Note 1078\_BCD).