Design and Application Notes for AP3107/H System Solution

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1. Introduction

The AP3107/H is a high voltage start-up, current mode PWM controller with green-mode power-saving operation.

The AP3107/H is specially designed for ultra low standby power performance. Different from AP3106, AP3107/H PWM switching frequency at normal operation is fixed at 65kHz/130kHz internally with a narrow range.

Table 1. The differences Between AP3107/H and AP3106

	AP3106	AP3107/H
Frequency	Adjustable	Fixed at 65kHz/130kHz
FB Resistor	18k	18k—Normal Mode 120k—Burst Mode
Standby Performance	Better	Best
Dynamic Performace	Good	A Little Bad
Application Area	Adapter	LCD Display/Standby Power

The AP3107/H integrates a lot of functions such as green mode, frequency dithering, VCC over voltage protection (VOVP) and line compensation. The green mode and burst mode functions with a low operating current could minimize the power consumed on light load, frequency dithering will help to achieve a good EMI result, VOVP protects the IC from being damaged when VCC voltage is too high in abnormal conditions, and line compensation enables a constant over load protection (OLP). Otherwise, over-temperature protection, soft-start function and brown-out function are also integrated in AP3107/H, and the brown-out range is embedded with a tight range of 70Vac to 80Vac.

The AP3107/H provides the users a high efficiency, low standby power, minimum external component counts and low cost solution for AC/DC power converters especially for LCD power. The standby power of system using AP3107/H could be less than 100mW, and the application note will show you how to design a SMPS using AP3107/H.

The AP3107/H is offered in SOIC-7 package to realize a compact size.

2. Peripheral Component

2.1 BNO Pin Resistor

The AP3107/H has the function of brown-out which can be realized by BNO pin, the brown-out voltage is adjusted by the resistor connected between BNO and GND, the formula of DC input voltage and BNO pin resistor is as the following：

$$V_{ON}(V) = 0.0001(V/k\Omega^2) \times R_{BNO}^2(k\Omega) - 0.1284(V/k\Omega) \times R_{BNO}(k\Omega) + 103.41(V)$$

$$V_{OFF}(V) = 0.0001(V/k\Omega^2) \times R_{BNO}^2(k\Omega) - 0.13(V/k\Omega) \times R_{BNO}(k\Omega) + 96.181(V)$$

Where：

V_{ON} means AP3107/H starts to work when the voltage on HV pin is higher than V_{ON}.

V_{OFF} means AP3107/H does not work when the voltage on HV pin is lower than V_{OFF}.

R_{BNO} is the resistor between BNO pin and GND.

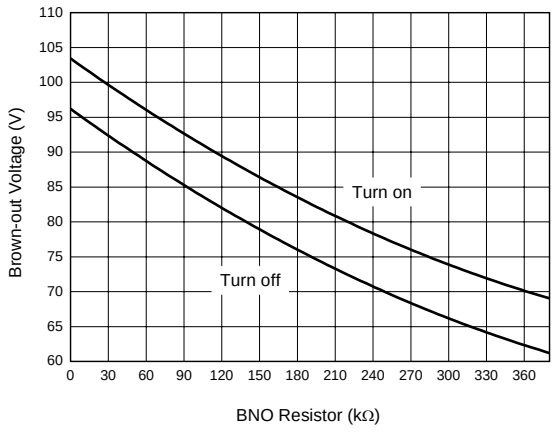

Figure 1. Brown-out Voltage vs. BNO Resistor

2.2 HV Protection Resistor

HV pin is connected to the high voltage line to start the IC, it can be connected to the line directly, but when the lightning surge test is done, the surge current may go through bulk capacitor positive, if

HV pin is connected to the line directly, the lighting noise will influence the IC by the PCB track, so one resistor 20kΩ to 50kΩ should be connected between high voltage line and HV pin.

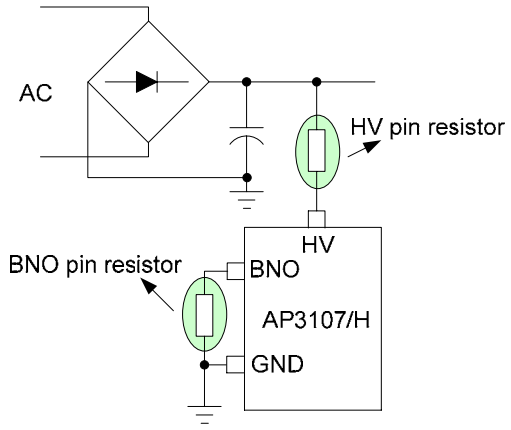

Figure 2. The Resistors of HV Pin and BNO Pin

2.3 SENSE Design for AP3106 and AP3107/H Series

2.3.1 The RC Filter Function

When switch is turned on, there will be a voltage spike (which is caused by parasitic capacitance of primary winding and secondary recovery current) on the current sensing resistor. To avoid false trigger by the voltage spike, there is 250ns LEB (Leading Edge Blanking) time for SENSE pin, but if the time of spike exceeds LEB time, the IC will be triggered falsely too, so the RC filter is necessary. Otherwise when the switch is shut down, there is a negative voltage on current sensing resistor, and the resistor could protect the IC from being damaged.

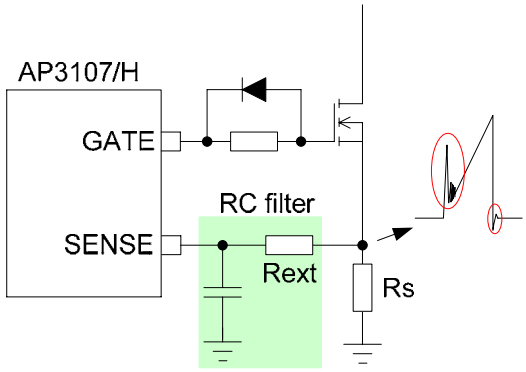

Figure 3. RC Filter for SENSE Pin

Though RC filter is helpful to the IC, it's time constant should be selected carefully, because it will affect the OCP result of system.

2.3.2 How to Get a Constant OLP

For a constant OLP from 90Vac to 264Vac, there is line compensation in AP3107/H and AP3106, the current limit point with line compensation is as below:

$$V_{cs} = \frac{136 * 10^6 (V * \Omega) - (Vin(V) - 107.7(V)) * (R_{ext}(\Omega) + 78850(\Omega))}{160 * 10^6 (\Omega)}$$

Where Rext is the resistor of RC filter for SENSE pin in Figure 3.

Figure 4 is the curve of SENSE pin voltage vs. line voltage when Rext=1k.

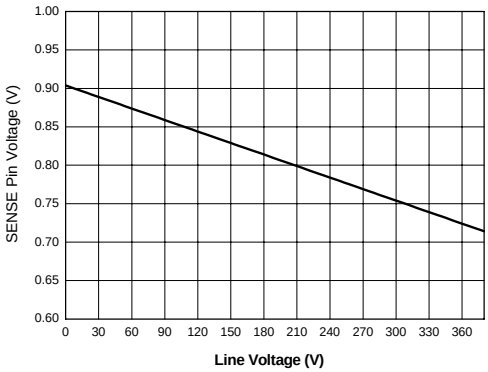

Figure 4. SENSE Pin Voltage vs. Line Voltage When Rext=1K

The formula of input power on OCP point is as the following:

For CCM,

$$Pin = Vo * (Ipeak + Itd - Icomp) * (1 - D) * Nt - \frac{N_t^2 * V_o^2 * (1 - D)^2}{L_m * fs}$$

For DCM,

$$Pin = \frac{1}{2}(Ipeak + Itd - Icomp)^2 * Lm * fs$$

Where
Ipeak is primary peak current which is V_{CS}/R_S;
Itd is the primary current caused by delay time (td) of IC and system which is V_{IN}*td/L_M;
Icomp is the current of line compensation on sensing resistor;
Nt is turn ratio;
L_M is primary inductor;
fs is switching frequency;
D is duty cycle.

By the formula, we can adjust some system parame-

ters to receive a better OLP result.

(1) Primary Inductance
Primary inductance will influence the working mode (CCM and DCM) of system on OLP point, and it will also decide the depth of CCM. DCM is better than CCM on contributing to constant OLP, and deeper CCM has a negative influence on constant OLP, so a lower value of primary inductance will be helpful to constant OLP.

(2) RC Filter for SENSE Pin
For RC filter, it should be adjusted on practical using, if the line compensation is too large on high line (OCP current on high line is lower than it on low line), increasing RC constant is helpful to constant OLP, if the line compensation is not enough on high line (OCP current on high line is lower than it on low line), decreasing RC constant is a good choice.

(3) Turn Ratio
If the line compensation is too large on high line, decreasing turn ratio is useful for constant OLP, if the line compensation is not enough on high line, increasing turn ratio is a good choice.

3. PCB Layout for AP310X Series

3.1 EMI Consideration

A proper PCB layout can abate unknown noise interference and EMI issue in the switching power supply. Shown as Figure 5, there are four main huge high frequency current loops:

1. The current path from bulk capacitor, transformer, MOSFET, R_{CS} returning to bulk capacitor, path A in Figure 5;
2. The path from GATE pin, MOSFET, R_{CS} returning to the ground of IC, path B in Figure 5;
3. The RCD clamp circuit is a high frequency loop, path C in Figure 5;
4. Transformer, rectifier diode, and output capacitor is also a high frequency current loop, path D in Figure 5.

They must be as short as possible to decrease the radiation area for a better EMI, and if the MOSFET and Schottky diode have heat sink, they should be connected to the ground separately.

Otherwise, the IC should not be placed in the loop of switching power trace, and control signal (low current and low voltage) should not be across switching power trace with pulsating high voltage, but power ground can be crossed.

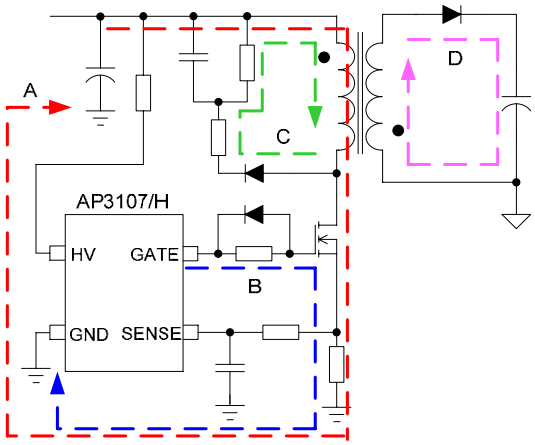

Figure 5. High Current Loop

3.2 ESD Design

Electro-static Discharge (ESD) is an important testing item for switching power supply, the ability of bearing for system could be improved by designing a path to release the electric charge to the ground.

As shown in Figure 6, the red line means the proposed path to release the charge. A copper tip for discharging can be placed between primary side and secondary side, but the distance between two tips should be consistent with the requirement of safety specification.

The inductor of common mode filter and differential mode filter will affect the effect of transient discharging, so there should be copper tip with them and the distance should be as short as possible. Another way is placing resistor paralleled with the inductor to replace the copper tip and the value is about 1kΩ to 5kΩ, a smaller resistor is helpful to ESD but has bad influence for lightning surge.

3.3 Common Mode Lightning Surge Design

In common mode lightning surge test, the IC pins may observe the noisy signal which is highly dependent on PCB design, so a good layout could improve the ability of enduring the surge test. “Star” connection is highly recommended for primary GND. As shown in Figure 7, the blue lines mean separated routines tied to GND which are connected together in bulk capacitor negative pin. The primary side of Y-cap can also be connected to the high voltage pin of transformer.

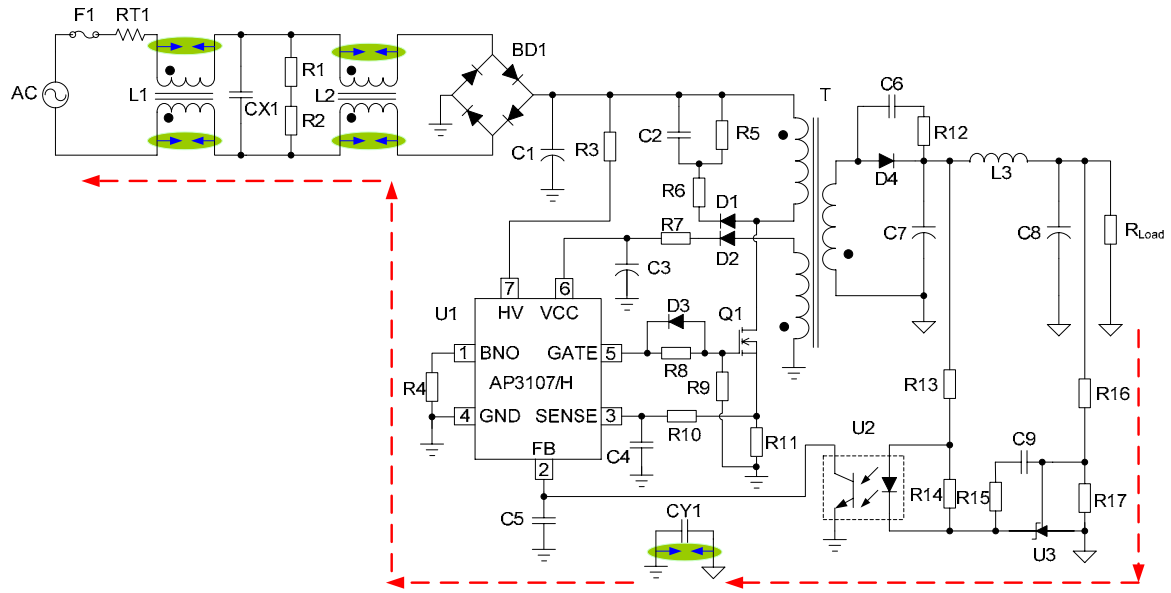

Figure 6. The Path to Release Charge of ESD

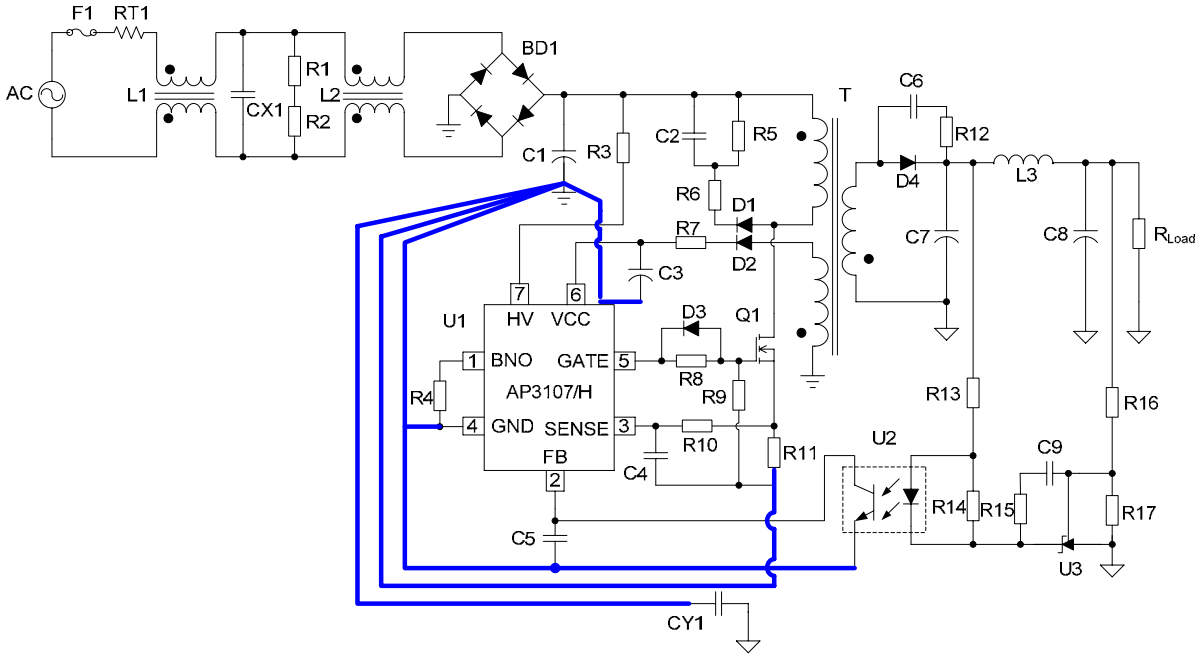

Figure 7. Star Connection of Primary GND

4. How to Design a Lower Standby Power with 3107/H

4.1 X-capacitor and X-resistor

A good quality X-capacitor will be helpful to save the standby power, using a low value X-cap can also decrease the X-cap losses, according to IEC 60950, for the X-cap exceeding 0.1μF, during an interval equal to one constant, the voltage will have decayed to 37% of its original value, and after calculating, the RC value is determined by R×C<1, so for a low value X-cap, a higher value X-resistor can be used, and the losses on X-resistor will be reduced.

4.2 Bulk Capacitor

A good quality bulk capacitor is contributed to low standby power, it can save 20mW to 30mW power relative to poor quality capacitor.

4.3 Opto-coupler Resistor

For a low standby power, small current mode technology is used under light load condition. If the system enters burst mode, the pulse of GATE pin is low and the persistent time is over one clock, IC will enter small current mode (the sourcing current of FB pin is about 50μA) to reduce the power consumption of AP3107/H, When system exits burst mode, the AP3107/H will operate at normal current mode. Otherwise, adjusting the opto-coupler resistor (R_{opt} in Figure 8) which parallels with the opto-coupler could affect the output voltage at small current mode. The current (I_{opt} in Figure 8) flows in the diode of opto-coupler is relative to the current of FB pin, so I_{opt} will be a small current. If the current flowing in R_{opt} and opto-coupler is not enough for shunt regulator, the output voltage at small current mode will be down from the center voltage a little, the higher value the R_{opt} is, the lower value the output voltage is, and the low output voltage will contribute to the low standby power. The value of R_{opt} can be calculated by following formula:

$$R_{opt} > \frac{V_{opt} \times K}{I_c \times K - I_{FB}}$$

Where:

V_{opt} is the drop voltage of diode in opto-coupler, the normal value is about 1V;

I_{FB} is sourcing current of FB pin at small current mode;

I_C is the minimum cathode current for regulation of shunt regulator;

K is the current transfer rate (CTR) of opto-coupler and the value is about 25% to 30% when there is 50μA current flowing in the transistor of opto-coupler.

When system exits the burst mode, the output voltage will go back to normal voltage.

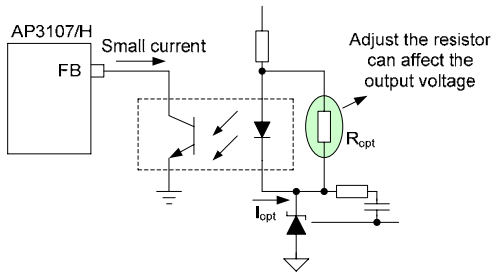

Figure 8. Resistor Paralleled with Opto-coupler

4.4 Current Sampling Resistor

The value of sampling resistor can affect the standby power, a lower value SENSE resistor is good for low standby power. But it is also relative to the OLP result, a lower value SENSE resistor will make a worse OLP result.

4.5 The Output Voltage Dividing Resistor

The value of output voltage dividing resistor should be as high as possible, but the maximum value of the resistor connected to GND (R17 in Figure 7) should not exceed 15kΩ.

4.6 RCD Clamp Circuit

For a better standby power, the RCD clamp circuit may be replaced by a Transient Voltage Suppressor (TVS) and a diode (Figure 9), the advantage of the TVS clamp is that it only conducts when it is really needed and is independent of the switching frequency. Compared to a RCD clamp, it reduces no-load power but increases costs and EMI. Otherwise, a lower value of RC is contributed to standby power, while the voltage stress on MOSFET should be within the spec.

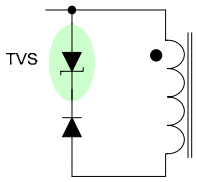

Figure 9. Clamp Circuit with TVS

4.7 RC Clamp on Schottky

A low value of RC which paralleled with Schottky is helpful to low standby power, the value should

be adjusted to make the voltage stress on Shottky not exceed the spec at turn-on.

5. LCD Monitor Demo Design and Test Result

A LCD monitor board using flyback topology is designed, the system specification is as below:

- Output voltage and current: 14V/2.5A, 5V/2.5A
- Input voltage range: 90Vac to 264Vac

Figure 10 shows the application schematic, and Table 2 is the test result of standby power. It shows the LCD monitor demo board components list. The standby power is less than 100mW in the whole input voltage range while the load are 5V/6mA and 14V/0A, the power is measured by a power meter Chroma 66202.

Table 2. Test Results of Standby Power (5V/6mA, 14V/0A)

Input Voltage	90Vac/60Hz	115Vac/60Hz	180Vac/50Hz	230Vac/50Hz	264Vac/50Hz
Input Power	0.057W	0.060W	0.049W	0.087W	0.095W

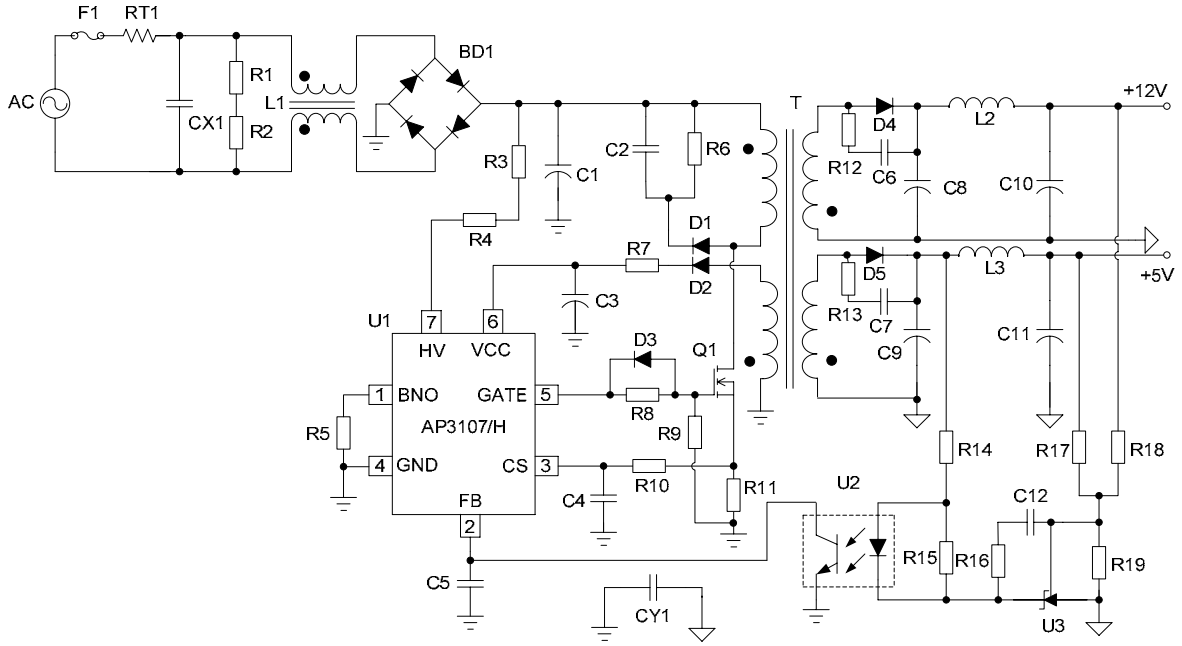

Figure 10. Application Circuit Schematic

Part	Value	Note	Part	Value	Note
BD1	GUB410		C4	10pF	0805C
F1	1A/250V		C5	6.8nF	0805C
RT1	5D-9		C6，C7	1nF/1kV	0805C
R1, R2	2MΩ	1206R	C8	680μF/16V	Electrolytic
R3, R4	20kΩ	1206R	C9	680μF/10V	Electrolytic
R5	100kΩ	0805R	C10	470μF/16V	Electrolytic
R6	100kΩ	Axial-1W	C11	470μF/10V	Electrolytic
R7	2.2Ω	1206R	C12	22nF	0805C

Part	Value	Note	Part	Value	Note
R8	10Ω	0805R	CX1	0.22μF	X-cap
R9	100kΩ	0805R	CY1	1nF	X-cap
R10	1kΩ	0805R	L1	30mH	0.8A
R11	0.39Ω	Axial-1/2W	L2	2.2μH	
R12	10Ω	1206R	L3	2.2μH	
R13	20Ω	1206R	D1	FR107	DO-41
R14	150Ω	0805R	D2	1N4007	DO-41
R15	7.5kΩ	0805R	D3	1N4148	1206
R16	20kΩ	0805R	D4	MBR10150	BCD Semi
R17	18kΩ	0805R	D5	MBR10100	BCD Semi
R18	180kΩ	0805R	U1	AP3107/H	SOIC-7
R19	12kΩ	0805R	U2	PC817C	Sharp
C1	100μF/400V	Electrolytic	U3	AZ431	BCD Semi
C2	2.2nF/1kV	Ceramic	Q1	STP6NK60Z	TO-220
C3	47μF/50V	Electrolytic	T1	ER28	