# AN1179

# DGD05473 DGD0507A Application Note

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The DGD05473 and DGD0507A High Frequency, High-Side, Low-Side Gate Drivers in DFN3030-10 are used to optimally drive the gate of MOSFETs. The DGD05473/07A has an integrated bootstrap diode for ease of design and reduced BOM. Below (Figure 1) is an example application using the DGD05473 with MOSFETs in a wireless charger transmitter. In this discussion, the important parameters needed to design in the DGD05473/07A are discussed; main sections are bootstrap capacitor selection, Gate Driver component selection, decoupling capacitor discussion and PCB layout suggestions.

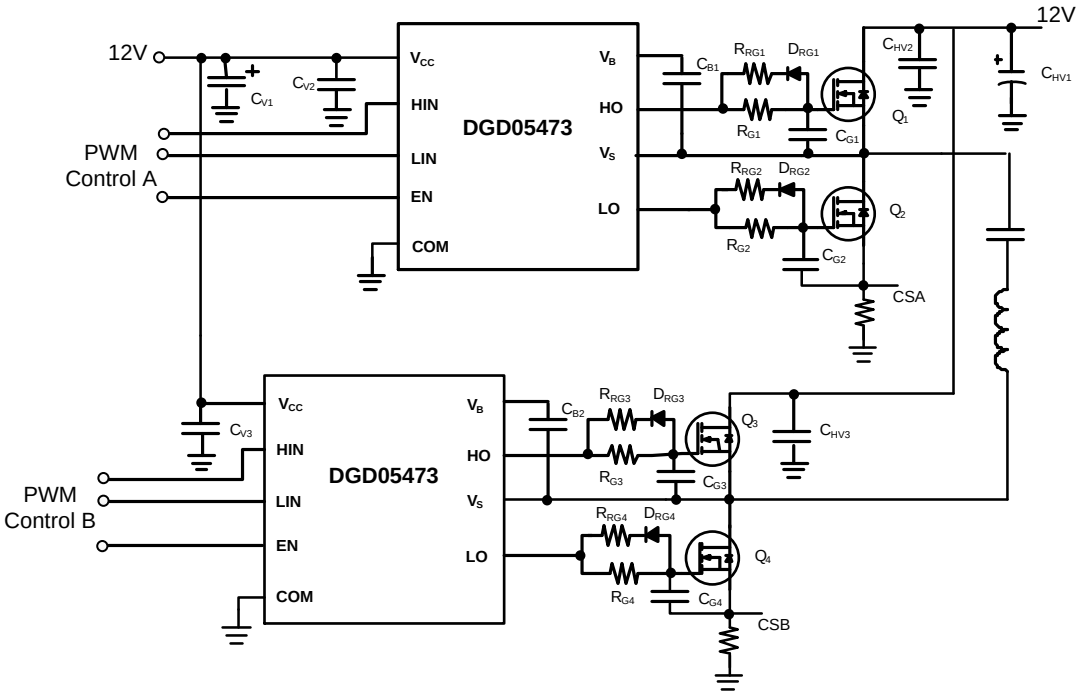


**Figure 1. Wireless charger transmitter example application using the DGD05473**

## Bootstrap Component Selection

Considering Figure 1, when the Low-Side MOSFET (Q2 or Q4) turns on, $V_S$ pulls to GND and the bootstrap capacitor ($C_{B1}$ and $C_{B2}$) is charged. When the High-Side MOSFET (Q1 or Q3) is turned on, $V_S$ swings above $V_{CC}$ and the charge on the bootstrap capacitor ($C_B$) provides current to supply the IC High-Side Gate Driver. The charge on $C_B$ is provided by $V_{CC}$ through the integrated bootstrap diode and bootstrap resistor and often the first charge of $C_B$ at power up will be the largest current through the bootstrap circuit as typically $C_B$ is not fully discharged at each cycle during normal operation.

### Bootstrap Capacitor Discussion

The initial step in determining the value of the bootstrap capacitor ($C_B$) is to determine the maximum voltage drop ($\Delta V_{BS}$) that can be guaranteed when the High-Side device is turned on. In other words, $V_{BSmin}$ must be greater than the UVLO of the High-Side circuit, specifically $V_{BSUV-}$ level. Therefore, if $V_{BSmin}$ is the minimum $V_{BS}$ such that:

$V_{BSmin} > V_{BSUV-}$

Then:

$\Delta V_{BS} = V_{CC} - V_F - V_{BSmin} - V_X$

Where:

- $V_{CC}$ is the supply voltage to the DGD05473
- $V_F$ is the voltage drop across the internal bootstrap diode ($D_{BS}$)
- $V_X$ is the voltage drop across the MOSFET

$V_X$ is calculated as the current seen across Low-Side MOSFET multiplied by its $R_{DS(ON)}$.

In addition to the voltage drops across these components, other factors that cause $V_{BS}$ to drop are leakages, charge required to turn on the power devices and duration of the High-Side on time. The total charge ($Q_T$) required by the Gate Driver then equals:

$Q_T = Q_G + Q_{LS} + [I_{LK\_N}] * T_{HON}$

Where:

$Q_G$ = gate charge of power device
$Q_{LS}$ = level shift charge required per cycle
$T_{HON}$ = High-Side on time
$I_{LK\_N}$ = sum of all leakages that include:

- $I_{GSS}/I_{GES}$: Gate-source leakage of the power device
- $I_{LK\_DB}$: Bootstrap diode leakage
- $I_{LK\_IC}$: Offset supply leakage of HVIC
- $I_{QBS}$: Quiescent current for High-Side supply
- $I_{LK\_CB}$: Bootstrap capacitor leakage

Bootstrap capacitor leakage ($I_{LK\_CB}$) only applies to electrolytic types. Therefore, it is best not to use an electrolytic capacitor. Thus, bootstrap capacitor leakages will not be included in the calculations.

$Q_{LS}$ is not listed in the datasheet; for the lower voltage process technology a $Q_{LS}$ of 5nC will be a good approximation and provide a sufficient margin.

From the basic equation, then the minimum bootstrap capacitor is calculated as:

$$C_{Bmin} \geq Q_T / \Delta V_{BS\_max}$$

**Example using MOSFET**

The follow example uses a power MOSFET as the switching device with the following and desired parameters:

- Power device = DMN6017SK3
- Gate Driver = DGD05473
- $V_{CC}$ = 12V
- $Q_G$ = 26nC
- $I_{GSS}$ = 100nA
- $T_{HON}$ = 5µs
- $R_{DS(ON)}$ = 25mΩ, 125°C
- $I_{OUT}$ = 10A
- $I_{QBS}$ = 100µA
- $I_{LK\_IC}$ = 1µA
- $Q_{LS}$ = 5nC

- $V_F$ = 1.0V
- $I_{LK\_DB}$ = 1µA
- $V_{GSmin}$ = 3.3V

From equations above:

$\Delta V_{BS\_max}$ = 12V- 1.0V-3.3V-0.25V = 7.45V

$Q_T = Q_G + Q_{LS} + [I_{LK\_N}]*T_{HON;}$ where $I_{LK\_N} * T_{HON}$ = 0.5nC

Thus $Q_T$ = 26nC + 5nC +0.5nC = 31.5nC

Therefore $C_{Bmin}$ = 31.5nC / 7.45V= 4.2nF

The bootstrap capacitor calculated in the above solution is the minimal value required to supply the needed charge. It is recommended that a margin of 2-3 times the calculated value be used, minimally. Utilizing values lower than this could result in over charging of the bootstrap capacitor especially during $-V_S$ transients. Typically for high-speed applications like power supplies, $C_B$ = 0.1µF to 1µF are used; and for low-speed applications like motor drives, $C_B$ = 1.0µF to 2.2µF are used. It is recommended to use low ESR ceramic capacitors as close to the $V_B$ and $V_S$ pin as possible (see PCB layout suggestions section).

## Integrated Bootstrap Diode

The DGD05473/07A has an integrated bootstrap diode to minimize the system BOM and to ease system design. From a DC perspective, the data below from the datasheet shows the performance of the integrated bootstrap diode:

| | | | | | | |
|---|---|---|---|---|---|---|
| Forward Voltage of Bootstrap Diode | $V_{F1}$ | — | 0.67 | — | V | $I_F$ = 100µA |
| Forward Voltage of Bootstrap Diode | $V_{F2}$ | — | 1.2 | — | V | $I_F$ = 100mA |

The current through the integrated bootstrap diode is typically the largest during the first charge of $C_B$. And the current waveform, as well as the time to charge $C_B$ is determined by the size of the $C_B$, see below Figure 2 and Figure 3.

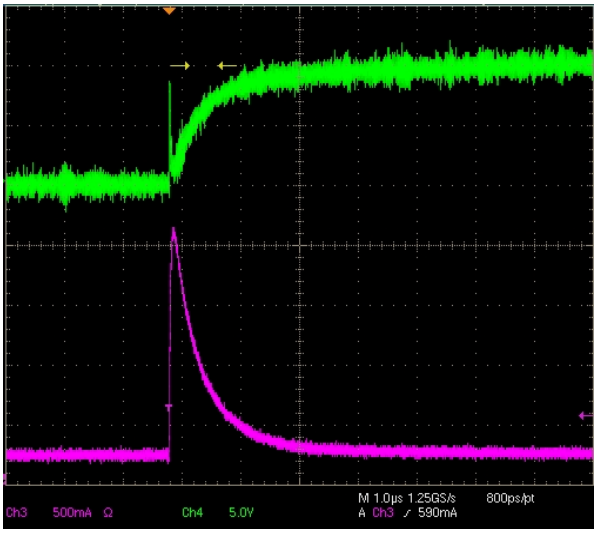


**Figure 2. Bootstrap inrush current (Ch3) and $V_{BS}$ (Ch4) with $C_B$ = 0.1µF**

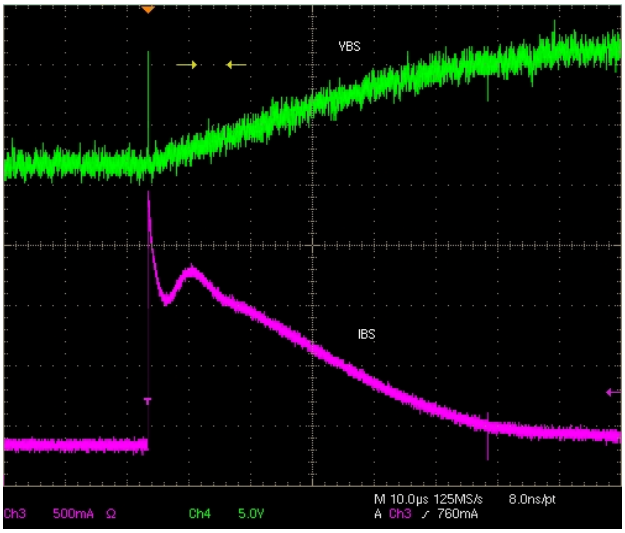


**Figure 3. Bootstrap inrush current (Ch3) and $V_{BS}$ (Ch4) with $C_B$ = 10µF**

## Gate Component Selection

The most crucial time in the gate drive is the turn on and turn off of the MOSFET, and performing this function quickly, but with minimal noise and ringing is key. Too fast a rise/fall time can cause unnecessary ringing and poor EMI, and too slow a rise/fall time will increase switching losses in the MOSFET.

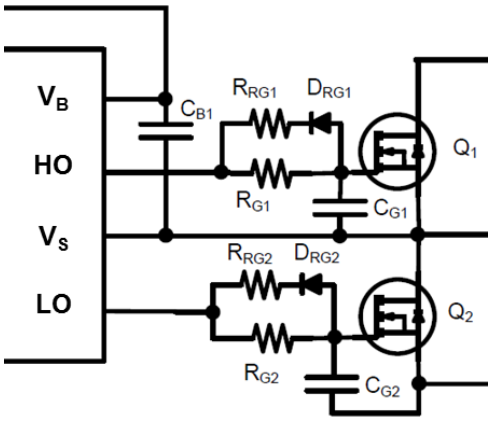


**Figure 4. Gate Driver High-Side and Low-Side components for DGD05473**

Considering the Gate Driver components for DGD05473/07A in Figure 4, with the careful selection of $R_{G1}$ and $R_{RG1}$, it is possible to selectively control the rise time and fall time of the gate drive to the MOSFET. For turn on, all current will go from the IC through $R_{G1}$ and charge the MOSFET gate capacitance, hence increasing or decreasing $R_{G1}$ will increase or decrease rise time in the application. With the addition of $D_{RG1}$, the fall time can be separately controlled as the turn off current flows from the MOSFET gate capacitance, through $R_{RG1}$ and $D_{RG1}$ to the driver in the IC to $V_S$ for High-Side and COM for Low-Side. So, increasing or decreasing $R_{RG1}$ will increase or decrease the fall time. Sometimes finer control is not needed and only $R_{G1}$ and $R_{G2}$ is used.

Increasing turn on and turn off has the effect of limiting ringing and noise due to parasitic inductances, hence with a noisy environment, it may be necessary to increase the gate resistors. Gate component selection is a compromise of faster rise time with more ringing, and a poorer EMI but better efficiency, contrasted with a slower rise time with better EMI, better noise performance but poorer efficiency. The exact value depends on the parameters of the application and system requirements. $R_{G1}$ and $R_{G2}$ values are typically between 10Ω and 50Ω, optimal value decided by MOSFET gate capacitance and drive current of Gate Driver. Gate resistor values are increased to decrease system noise, minimize ringing, and hence lower EMI. $R_{RG1}$ and $R_{RG2}$ values are typically between 5Ω and 20Ω, optimal value decided by MOSFET gate capacitance and drive current of Gate Driver. Also, sink current gate resistor values are increased to decrease system noise, minimize ringing, and hence lower EMI.

To have equal switching times for High-Side and Low-Side, it is recommended that the Gate Driver components for High-Side and Low-Side are mirrored. For example, $R_{RG1}$=$R_{RG2}$, $D_{RG1}$=$D_{RG2}$ and $R_{G1}$=$R_{G2}$.

The gate to source capacitors, $C_{G1}$ and $C_{G2}$, are used to minimize unexpected shoot-through in the Half-Bridge and to improve system stability. The shoot-through can decrease efficiency or even damage the MOSFETs; this phenomenon is discussed further on page 6. If the Ciss of the MOSFET is small and there is instability in the system performance, add $C_{G1}$ and $C_{G2}$ to improve stability. To begin, $C_{G1}$=$C_{G2}$=1nF should improve system performance.

## VCC Decoupling Capacitors

For optimal operation, $V_{CC}$ decoupling is crucial for all Gate Driver ICs. With poor decoupling, larger $V_{CC}$ transients will occur at the IC when switching, and for greater and longer $V_{CC}$ drop the IC can go into UVLO.

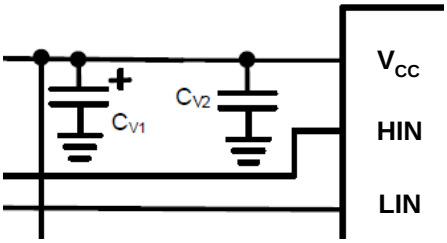


**Figure 5. Suggested $V_{CC}$ decoupling**

As shown in Figure 5, two decoupling capacitors are recommended $C_{V1}$ and $C_{V2}$. $C_{V1}$ can be a larger electrolytic capacitor, for example 47µF, 50V, used to dampen low frequency drains on supply; $C_{V1}$ does not need to be right next to the IC. But $C_{V2}$ is used to decouple faster edge

changes to $V_{CC}$ and should be a low ESR ceramic capacitor placed close to the $V_{CC}$ pin. This component provides stability when $V_{CC}$ is quickly pulled down with load from the IC; typical values are 0.1µF to 1µF.

For applications with multiple Gate Driver ICs (for example, a BLDC motor drive with 3 x Gate Drivers), one larger electrolytic capacitor ($C_{V1}$) can be used and the three ceramic caps ($C_{V2}$, $C_{V3}$, $C_{V4}$) should be used close to the $V_{CC}$ pin (see Layout section also).

## High Voltage Decoupling Capacitors

Considering the performance of the entire half-bridge, it is important to have appropriate high voltage decoupling capacitors (see $C_{HV1}$, $C_{HV2}$, and $C_{HV3}$ in Figure 1). For best stability (best high-frequency performance), $C_{HV2}$ and $C_{HV3}$ are smaller ceramic capacitors (say 1µF 100V) placed close to the drain of the MOSFETs at the Half-Bridge (less than 25mm); and then $C_{HV1}$ is the electrolytic bulk capacitor which is typically part of the on-board power supply. If the small decoupling capacitors ($C_{HV2}$ and $C_{HV3}$) are not used, then for optimal operation, the bulk capacitor ($C_{HV1}$) should be close to the drain of the MOSFETs (less than 25mm). For even further high frequency decoupling, many parallel ceramic capacitors can be used. For example, 1.0µF in parallel with 3 x 0.1µF capacitors.

## Start Up Sequence

To ensure that the Absolute Maximum Specifications for the inputs are met (see Figure 6), a correct start up sequence should be followed. The inputs cannot go above $V_{CC}$, hence $V_{CC}$ should be powered up first before any signal is applied to HIN, LIN and EN. To enable the outputs to follow the inputs at startup, $V_{CC}$ should be greater than UVLO+ (7.0V typ.) before any PWM signal is applied to the inputs.

In addition, to ensure stable performance of the high-side driver at start up, it is recommended that $V_{BS}$ should be greater than $V_{BS}$ UVLO+ (7.0V typ.) before any signal is applied to HIN and EN. If $V_S$ is floating at startup, it may be necessary to pull $V_S$ to 0V (turn on the low-side first, allowing $C_B$ to fully charge) before applying signal to HIN and EN

| | | | |
|---|---|---|---|
| Logic Input Voltage (HIN, LIN and EN) | $V_{IN}$ | -0.3 to $V_{CC}$+0.3 | V |

**Figure 6. Absolute Maximum Specification for input pins**

## Input Resistors

The IC PWM inputs, HIN, LIN, and EN, are very high impedance inputs with pull-down resistors. The pull-down resistors on HIN, LIN, and EN have an approximate value of 100kΩ.

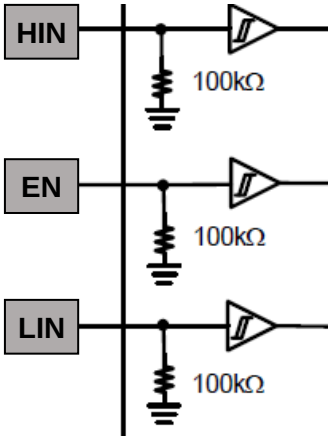


**Figure 7. Input logic for the DGD05473**

## Differences between DGD05473 and DGD0507A

The minimum allowed $V_{CC}$ operating condition is the main difference between the DGD05473 and the DGD0507A. Hence the $V_{CC}$ Recommended Operating Voltage and UVLO (both $V_{CC}$ and $V_{BS}$) are the main specifications where the two devices differ.

| | | | | |
|---|---|---|---|---|
| Logic and Low Side Fixed Supply Voltage | $V_{CC}$ | 4.5 (Note 8) | 14 | V |
| High-Side Floating Supply | $V_B$ | $V_S$ + 4.2 | $V_S$ + 14 | V |

**Figure 8. Recommended operating voltages for the DGD05473**

| | | | | | | |
|---|---|---|---|---|---|---|
| $V_{CC}$ Supply Undervoltage Positive Going Threshold | $V_{CCUV+}$ | 3.3 | 3.8 | 4.2 | V | — |
| $V_{CC}$ Supply Undervoltage Negative Going Threshold | $V_{CCUV-}$ | 2.9 | 3.3 | 3.9 | V | — |

**Figure 9. $V_{CC}$ UVLO for the DGD05473 ($V_{BS}$ UVLO is the same)**

| | | | | |
|---|---|---|---|---|
| Logic and Low Side Fixed Supply Voltage | $V_{CC}$ | 8 | 14 | V |
| High-Side Floating Supply | $V_B$ | $V_S$ + 8 | $V_S$ + 14 | V |

**Figure 10. Recommended operating voltages for the DGD0507A**

| | | | | | | |
|---|---|---|---|---|---|---|
| $V_{CC}$ Supply Undervoltage Positive Going Threshold | $V_{CCUV+}$ | 6.0 | 7.0 | 8.0 | V | – |
| $V_{CC}$ Supply Undervoltage Negative Going Threshold | $V_{CCUV-}$ | 5.6 | 6.6 | 7.6 | V | – |

**Figure 11. $V_{CC}$ UVLO for the DGD0507A ($V_{BS}$ UVLO is the same)**

## Suggestions for $V_{CC}$ = 5V operation using the DGD05473

Due to the performance of the Gate Driver outputs at low voltages, the minimal operating voltage level on $V_B$=4.3V. For $V_{CC}$=5V operation, this is not a concern for Low-Side operation as it is operating at $V_{CC}$, but the High-Side output driver is operating at a diode drop from internal bootstrap diode; hence when $V_{CC}$=5V, $V_{BS}$=4.3V, which would be ok. However, for a system operating at $V_{CC}$=5V, it is typical to require $V_{CC}$=4.5V to 5.5V, and when $V_{CC}$=4.5V, $V_B$ will be below the Recommended Operating Condition. Hence, when wanting to use $V_{CC}$ = 4.5V to 4.9V operation it is required to use an external Schottky diode (see Figure 12).

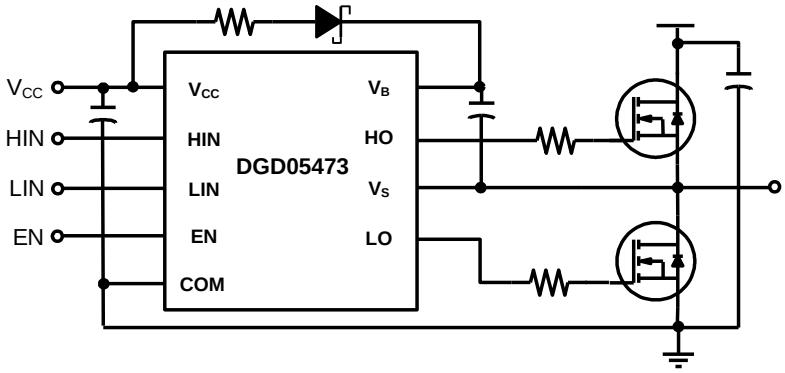


**Figure 12. Typical application necessary for $V_{CC}$ = 4.5V to 4.9V, an external bootstrap Schottky will turn on before internal $D_{BS}$**

## Matching Gate Driver with MOSFET

### IC drive current and MOSFET gate charge

Gate Driver ICs are defined by their output drive current, its ability to source current to the gate of the MOSFET at turn on and to sink current from the gate of the MOSFET at turn off. For the DGD05473 the drive current is IO+ = 1.5A typical and IO- = 2.5A typical.

For a given MOSFET, with the known drive current of the DGD05473, you can estimate how long it will take to turn on/off the MOSFET with the equation:

$t = Q_g / I$

$Q_g$ = total charge of the MOSFET as provided by the datasheet
I = sink/source capability of the Gate Driver IC
t = calculated rise/fall time with the given charge and drive current

For example, with the Diodes Incorporated's (Diodes) DMN6017SK3, 60V 43A, $Q_g$ = 55nC; and with the DGD05473 IO+/IO, the calculated rise and fall times are tr = 37ns and tf = 22ns respectively. These are estimates as the total charge given in the datasheet may not be the same conditions in the application. An addition of a gate resistor will increase the tr and tf.

## Unexpected shoot-through with $dV_{DS}/dt$

Unwanted MOSFET turn-on, caused by $C_{GD}$ x $dV_{DS}/dt$ (see Figure 13) is often the cause of unexplained shoot through in the half-bridge circuit. Depending on the ratio of the $C_{GS}/C_{GD}$, when the $dV_{DS}/dt$ across Low-Side MOSFET (Q2) occurs (i.e when High-Side MOSFET turns on), there can be a voltage applied to the gate of the Q2 MOSFET, turning on Q2 and causing shoot through. In effect a gate bouncing occurs causing a ringing on the $V_S$ line and the power ground.

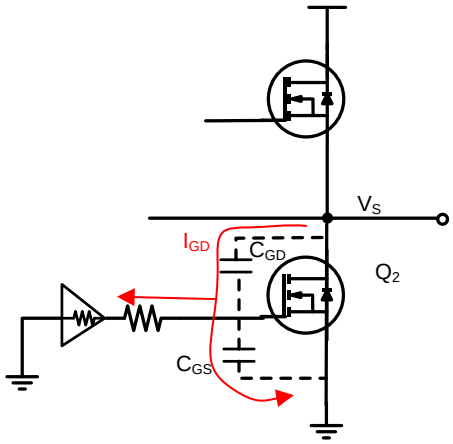


**Figure 13. Unexpected shoot through with $dV_{DS}/dt$**

Considering Figure 13:

$I_{GD} = C_{GD} \times dV_{DS}/dt$

$I_{GD}$ will flow towards the resistive load (and small inductive due to parasitics) of the Gate Driver and the $C_{GS}$ of the MOSFET. Hence, this unwanted condition may be minimized by looking at the Ciss/Cres in the MOSFET datasheet (Ciss/Cres gives an indication of $C_{GS}$/ $C_{GD}$); having a Ciss/Cres as large as possible will minimize this phenomenon. An external capacitor can be added to the gate-source of the MOSFET (for example 1nF) which will increase $C_{GS}/C_{GD}$.

## Minimum Pulse Operation

The DGD05473 has an RC filter on the input lines to be more resilient in noisy environments. During typical operation, the DGD05473 will respond to an input pulse greater than about 40ns. Hence for an input pulse greater than 40ns approximately, the IC will follow the pulse as expected; and for an input pulse less than 40ns, there will be no response from the IC.

## PCB layout suggestions

Layout also plays a considerable role since unwanted noise coupling, unpredicted glitches and abnormal operation could arise due to poor layout of the associated components. Figure 14 shows the schematic with parasitic inductances in the high current path ($L_{P1}$, $L_{P2}$, $L_{P3}$, $L_{P4}$) which would be caused by inductance in the metal of the trace. Considering Figure 14, the length of the tracks in red should be minimized and the bootstrap capacitor ($C_B$) and decoupling capacitor ($C_D$) should be placed as close to the IC as possible, and should use low ESR ceramic capacitors. Finally, the gate resistors ($R_{GH}$ and $R_{GL}$) and the sense resistor ($R_S$) should be surface mount devices. These suggestions will reduce the parasitics due to the PCB traces.

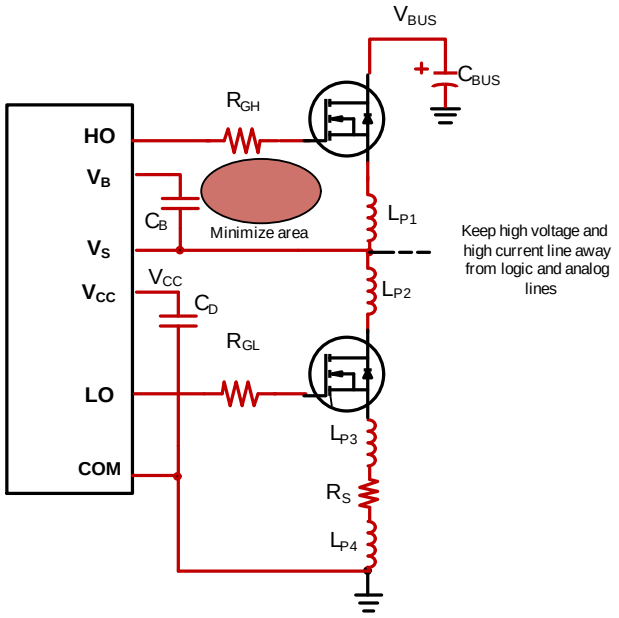


**Figure 14. Layout suggestions for DGD05473/07A in a half-bridge, lines in red should be as short as possible**

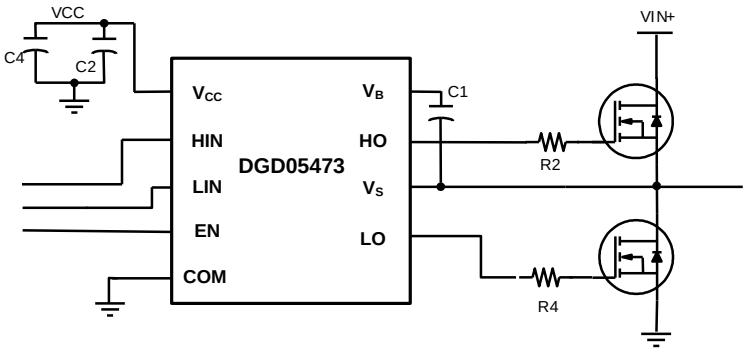


**Figure 15. Schematic for layout example shown in Figure 16**

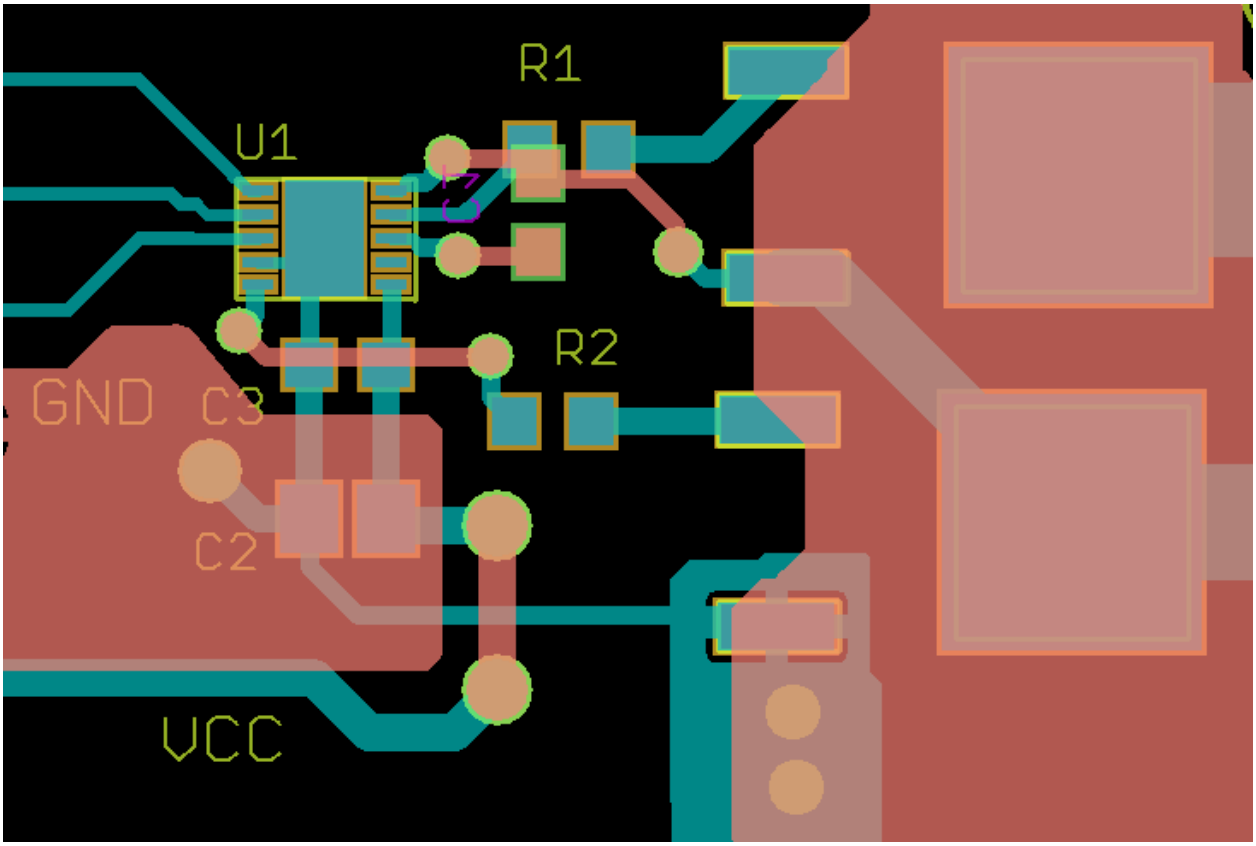


**Figure 16. Suggested layout of the schematic shown in Figure 15, DGD05473 in DFN3030-10**

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