# The Pericom Universal Level Shifter
## Application Note

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## 1. Introduction

- In order to link between the 3.3V chipset A and the 1.8V chipset B in Figure 1, a voltage level shifter is needed (depicted as U1 in the figure).
- A tradition voltage level shifter (such as the one in Figure 1) requests a “DIR” signal to indicate U1 the bus direction as A-to-B or B-to-A.
- However, most of the bi-directional bus protocols do not offer the “DIR” signal.
- Therefore, traditional voltage level shifters do not satisfy the needs of most of the bi-directional bus protocols, such as the SD application.

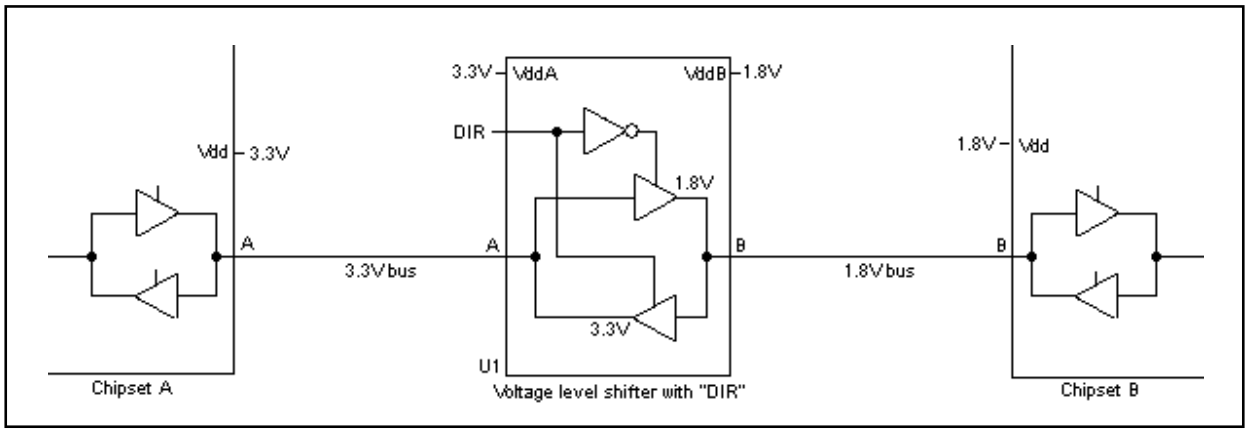


**Figure 1: Tradition Voltage Level Shifter Needs a DIR Control Signal**

## 2. The Concept and Mechanism of the Pericom Universal Level shifter

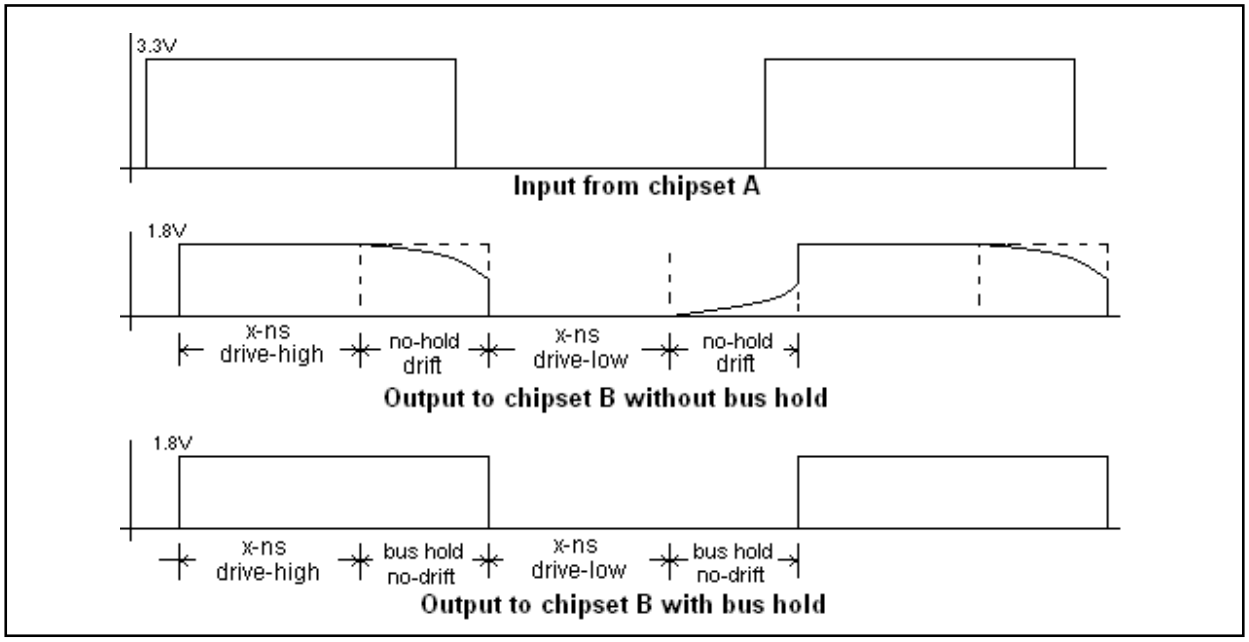


**Figure 2: Concept and the Mechanism of the Pericom Universal Level Shifter**

Figure 2 depicts that the Pericom Universal Level Shifter (USL) only drives the output bit for few nano-second (x-ns), and then uses the bus-hold to keep the rest of the bit, as illustrated in Figure 3.

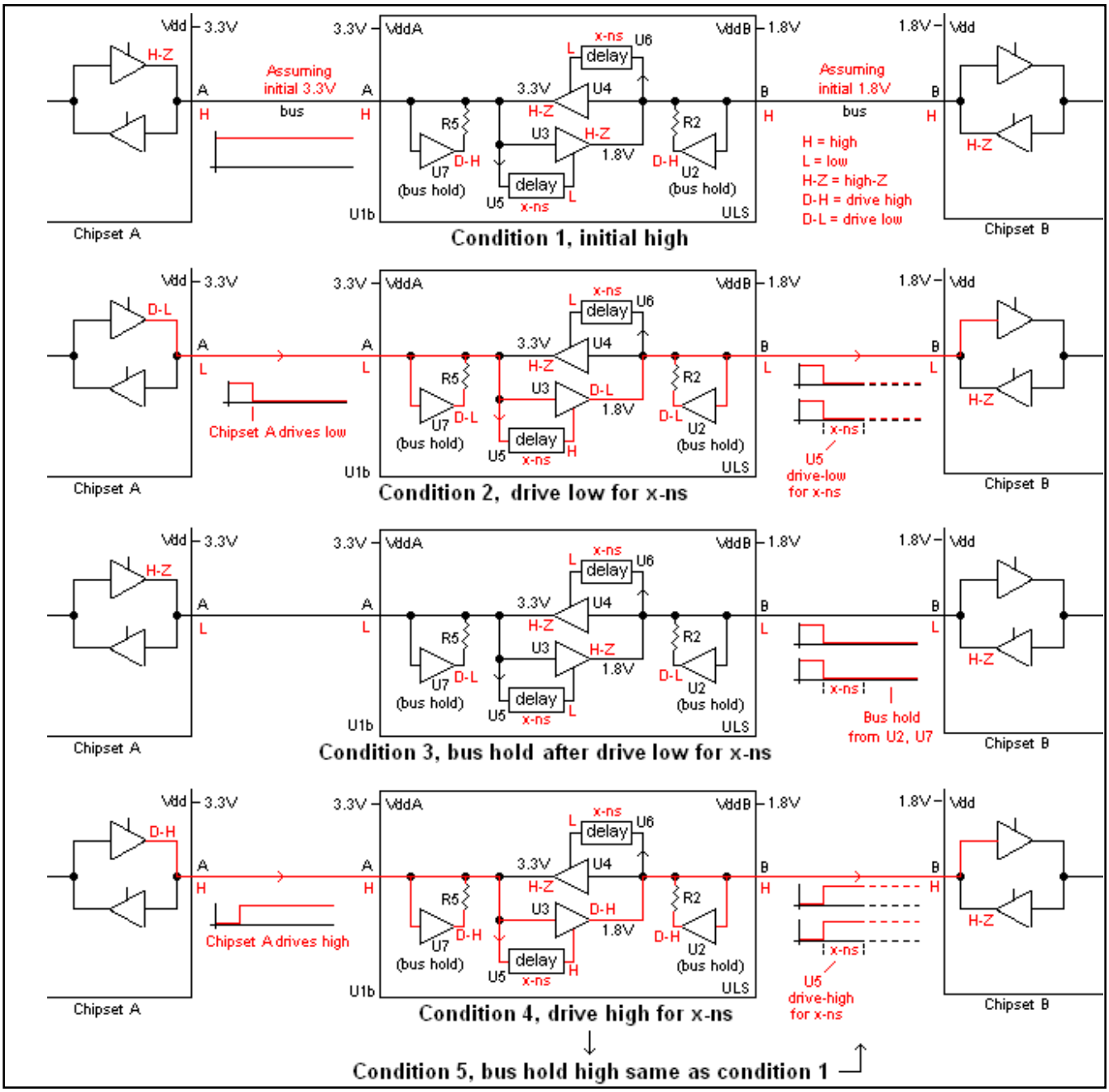


**Figure 3: Concept and the Mechanism of the Pericom Universal Level Shifter**

Figure 3 shows the transients of the ULS from chipset A to B (chipset B to A is identical):

- Condition 1, assuming the initial IO to ULS is logic-high (it can be low)
  - Chipset A and B: idle.
  - U5 and U6 (delay): output low to disable U3 and U4 (normal CMOS driver) with output high-Z
  - U2 and U7: hold the bus high.
- Condition 2, condition 3
  - Chipset A drives low and overcomes bus-hold U2 and U7 to output-low.
  - U5 (delay) enables U3 to output low for x-ns, then high-Z.
  - U2 and U7: hold the bus low.
- Condition 4, condition 5 (same as condition 1)
  - Chipset A drives high overcomes bus-hold U2 and U7 to output-high.
  - U5 (delay) enables U3 to output high for x-ns, then high-Z.
  - U2 and U7: hold the bus high.

## 3. Application Conditions of Universal Level shifter

- ULS devices can only work with normal CMOS or TTL push-pull drivers that have push-pull output impedance less than 80ohm.
  - Due to the fact that the bus-hold in ULS needs a COMS-TTL driver to overcome, a normal CMOS or TTL driver should have the push-pull output impedance less than 65ohm to match the single-ended trace impedance in the range of 50-65ohm.
- ULS devices can not work with open-drain drivers or other drivers with push-pull output impedance higher than 100ohm.
- During power-up, the ULS devices latch (as in the initial stage) the pull-up or pull-down state of the connected signals. Otherwise, the initial logic states from chipset A or B are latched.

## 4. Applications Using Pericom Universal Level Shifter

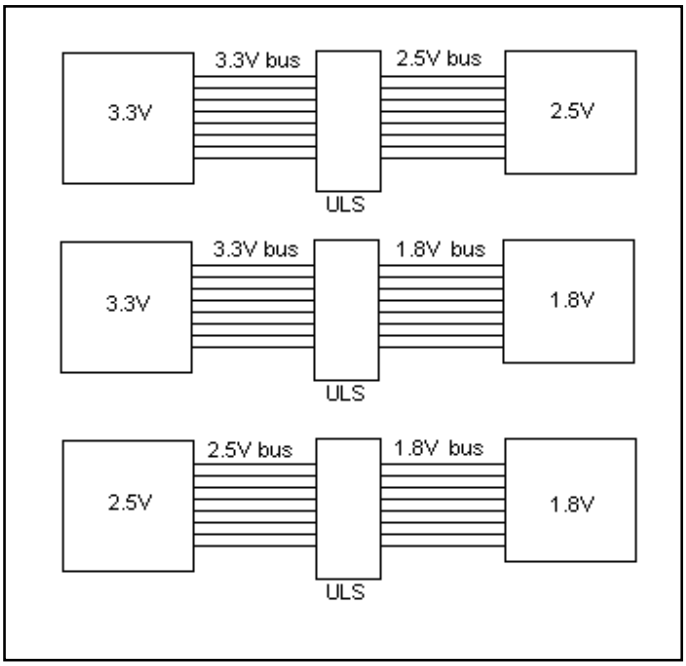


**Figure 4: Voltage Level Shifting Between Various Bus Voltages**

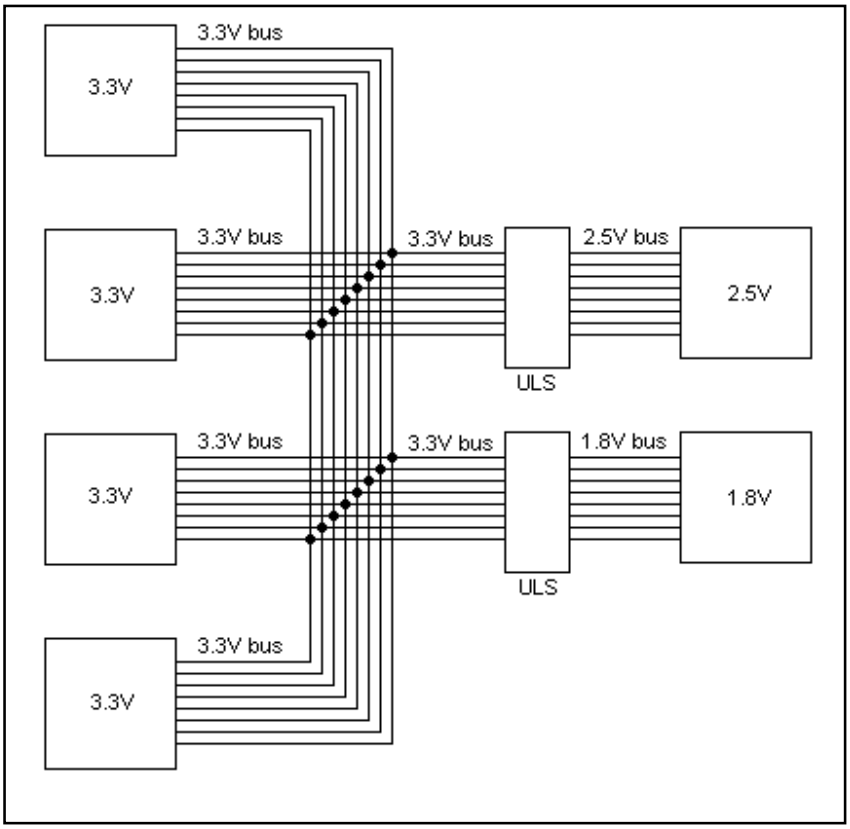


**Figure 5: Connecting Devices with Different Voltages**

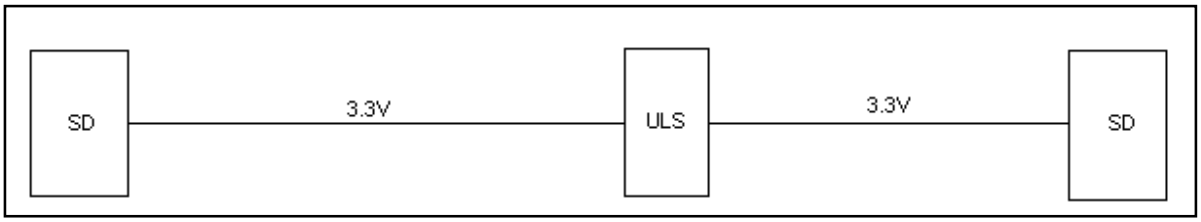


**Figure 6: Extend SD Devices with a Long Trace and/or Cable**

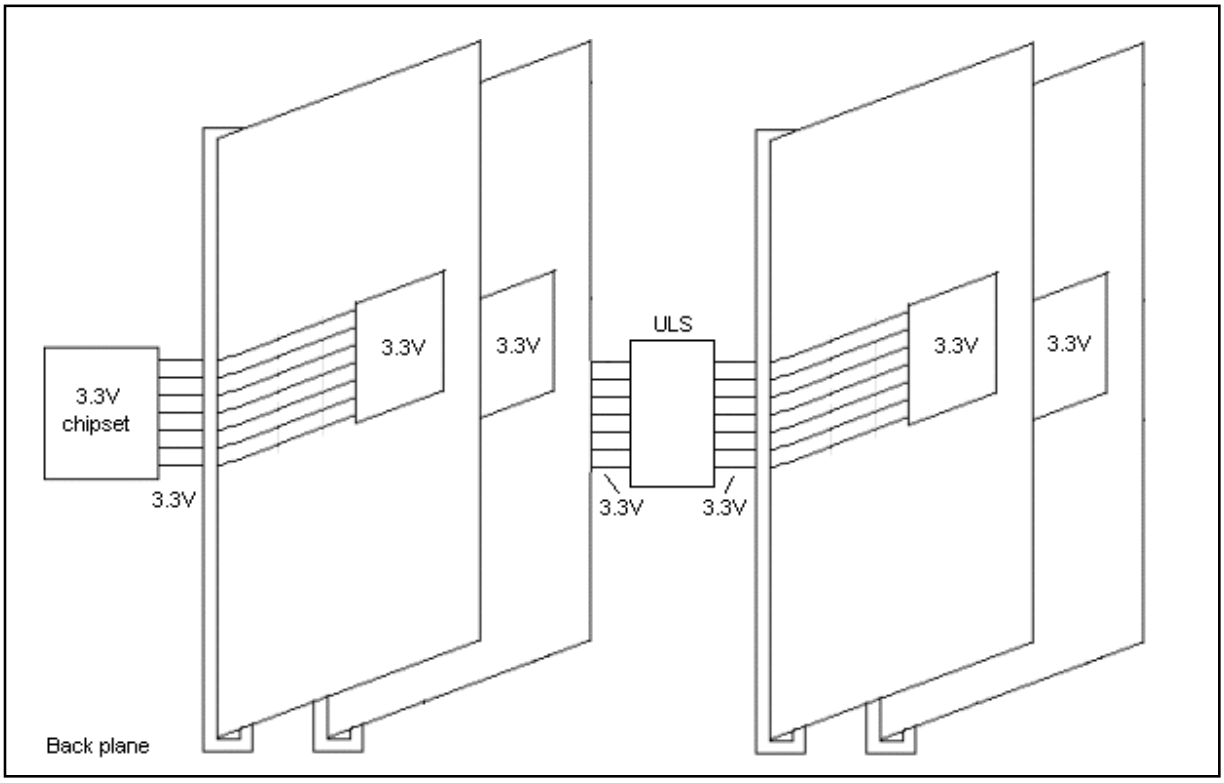


**Figure 7: Extend More Loads in a Back Plane**