PI3EQX6852BZDE
PI3EQX6852B SATA ReDriver Application Note
Nov. 2, 2011

Introduction

PI3EQX6852B SATA ReDriver™ is design to re-drive one full lane of SAS/SATA (up to 6Gbps) signal. The device features lower power consumption and excellent performance. Figure1 illustrates a typical application sample.

PI3EQX6852B has Termination Detect function for excellent lower power when HDD is unplugged.

Packaging: 20-contact TQFN (4x4mm)

Main Application:
- ✓ *Notebook*
- ✓ *Docking*
- ✓ *Desktop/Storage/Server*

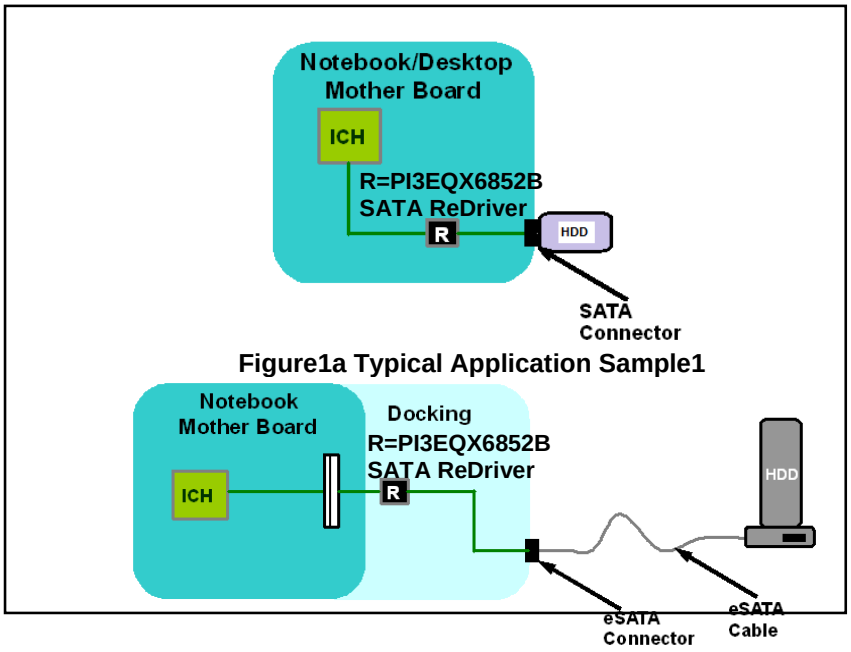


Figure 1: Examples of Typical Application

PI3EQX6852B Control Pins

PI3EQX6852B's control pins include EN, OOB, TDet_EN# AB/BB, and A_EQ/B_EQ. Table1 is the selection setting for various applications.

Pins	Function Description	Setting Selection
EN	Chip Enable Function w/ internal 200k pull-up resistor	High: Normal Operation (default) Low: Power-down mode
OOB	Signal detect threshold Selection w/ internal 200k pull-down resistor	High: 200mV Threshold Detect Low: 120mV Threshold Detect (default)
TDet_EN#	Termination Detect Enable w/ internal 200k pull-down resistor	High: Disable Termination Detect Function Low: Enable Termination Detect (default)
AB/BB	Output Swing Adjustment w/ internal 200k pull-down resistor	High: 1200mVppd Output Swing (for SAS application) Low: 600mVppd Output Swing (default) (SATA application)
A_EQ/B_EQ	Input Equalizer Adjustment Tri-level control	A_EQ/B_EQ: 0 — 6Gb/s: 8 dB — Various Applications: for 12~24 inch input trace A_EQ/B_EQ: $V_{DD}/2$ — 6Gb/s: 4 dB (Default) — Various Applications: for less than 12 inch input trace A_EQ/B_EQ: 1 — 6Gb/s: 16 dB — Various Applications: for 18~30 inch input trace

Note: All the NC pins are NO INTERNAL Connection.

External Component Requirement

PI3EQX6852BZDE requires AC coupling capacitors for all redriver outputs. High-quality, low-ESR, X7R, 10nF, 0402-sized capacitors are recommended.

Layout Design Guide

Layout Considerations for Differential Pairs

- The trace length miss-matching shall be less than 5 mils for the "+" and "–" traces in the same pairs
- Use wider trace width, with 100ohm differential impedance, to minimize the loss for long routes
- Target differential Zo of 100ohm ±20%
- More pair-to-pair spacing for minimal crosstalk coupling, it is recommended to have >3X gap spacing between differential pairs.
- It is preferable to route differential lines exclusively on one layer of the board, particularly for the input traces
- The use of vias should be avoided if possible, if vias must be used, they should be used sparingly and must be placed symmetrically for each side of a given differential pair.
- Route the differential signals away from other signals and noise sources on the printed circuit board

PCB Layout Trace Routings

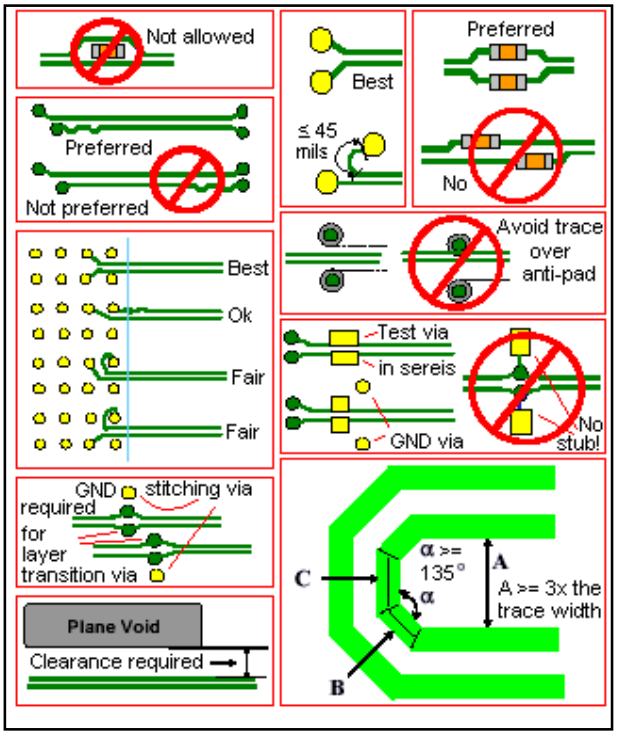


Figure 2: Layout Sample for Trace Routings

Power-Supply Bypass

Designers must pay attention and be careful with the details associated with high-speed design as well as providing a clean power supply; there are some approaches that are recommended.

- The supply (VDD) and ground (GND) pins should be connected to power planes routed on adjacent layers of the printed circuit board. The distance to plane should be <50mil.
- The layer thickness of the dielectric should be minimized so that the VDD and GND planes create a low inductance supply with distributed capacitance.
- Careful attention to supply bypassing through the proper use of bypass capacitors is required. A low-ESR 0.01uF bypass capacitor should be connected to each VDD pin such that the capacitor is placed as close as possible to PIxEQX6741SxZDE. Smaller body size capacitors can help facilitate proper component placement.
- The distance of capacitors to IC body should be <100mil.
- One capacitor with capacitance in the range of 1uF to 10uF should be incorporated in the power supply bypassing design as well. It is can be either tantalum or an ultra-low ESR ceramic.

Power Supply Sequencing

Proper power supply sequencing is recommended for all devices. Always apply GND and VDD before applying signals, especially if the signal is not current limited.

Caution: Do NOT exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the device.

Equalization and Pre-emphasis Setting

Various Input Traces and Eye Tests with different EQ settings

Figure 3 shows PI3EQX6852BZDE test setup in different EQ settings. TDet_EN#=High. R in the figure represents PI3EQX6852BZDE.

Signal Source: PRBS2^7-1 pattern, Differential Voltage is 600mV,

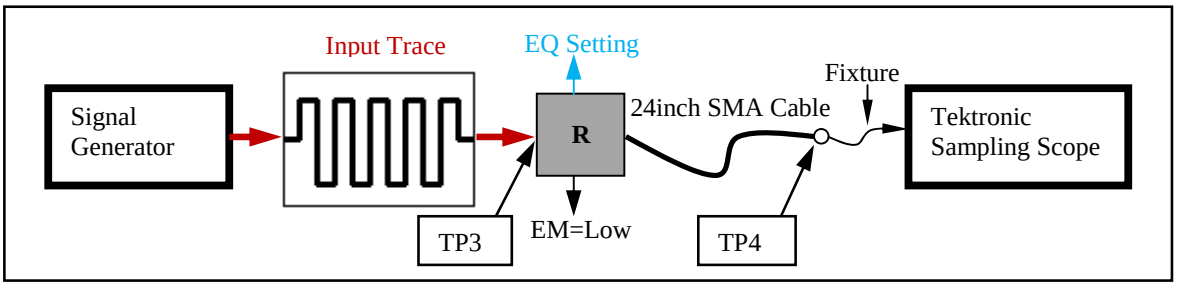


Figure 3: EQ Setting Test Setup for PI3EQX6852BZDE

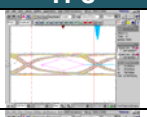
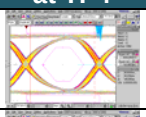
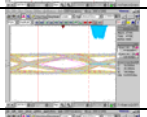
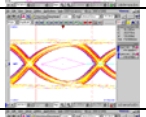
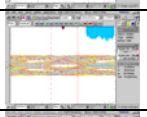
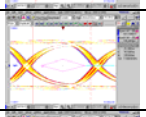
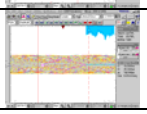
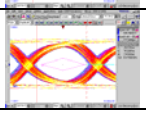
Input Trace Length	EQ Setting	Input Eye at TP3	Output Eye at TP4
6 inch FR4 Lab trace (-2dB loss at 3GHz)	4dB (A_EQ or B_EQ =Open)		
18 inch FR4 Lab trace (-6dB loss at 3GHz)	8dB (A_EQ or B_EQ =Low)		
30 inch FR4 Lab trace (-10dB at 3GHz)	16dB (A_EQ or B_EQ =High)		
48 inch FR4 Lab trace (-16dB loss at 3GHz)	16dB (A_EQ or B_EQ =High)		

Table 2: Eye Diagram vs. Input FR4 trace and EQ Setting at 6Gb/s

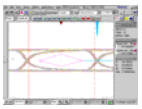
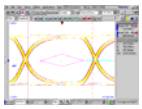
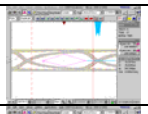
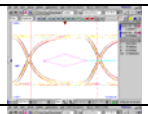
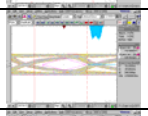
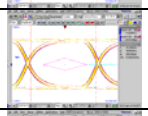
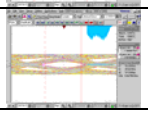
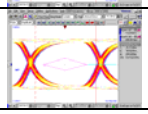
Input Trace Length	EQ Setting	Input Eye at TP3	Output Eye at TP4
6 inch FR4 Lab trace (-1.2dB loss at 1.5GHz)	4dB (A_EQ or B_EQ =Open)		
18 inch FR4 Lab trace (-3dB loss at 1.5GHz)	8dB (A_EQ or B_EQ =Low)		
30 inch FR4 Lab trace (-5dB loss at 1.5GHz)	16dB (A_EQ or B_EQ =High)		
48 inch FR4 Lab trace (-9dB loss at 1.5GHz)	16dB (A_EQ or B_EQ =High)		

Table 3: Eye Diagram vs. Input FR4 trace and EQ Setting at 3Gb/s

Eye Test with Different Swing Setting

Figure 4 shows PI3EQX6852BZDE test setup for different swing settings. TDet_EN#=High. R in the figure represents PI3EQX6852BZDE.

Signal Source: PRBS2^7-1 pattern, Differential Voltage is 600mV, Equalization is 4dB

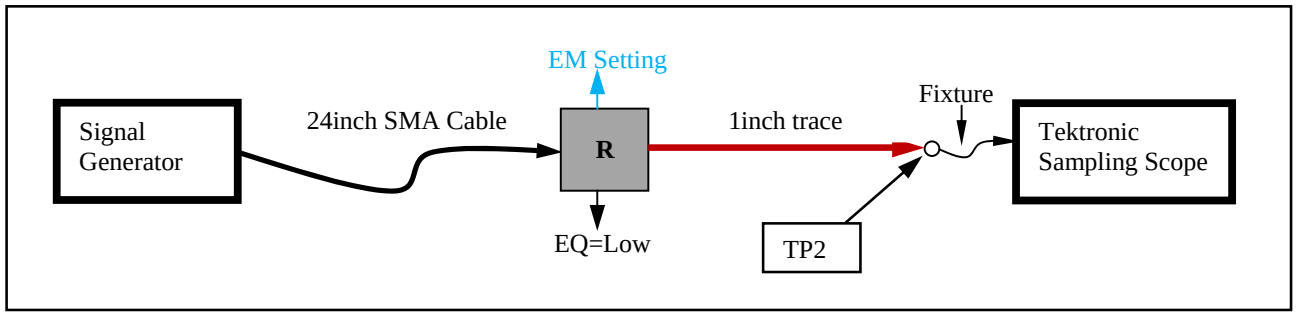


Figure 4: EM Setting Test Setup for PI3EQX6852BZDE

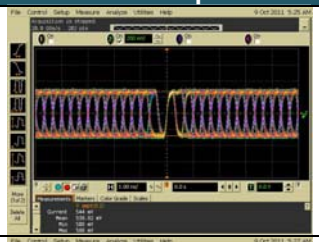
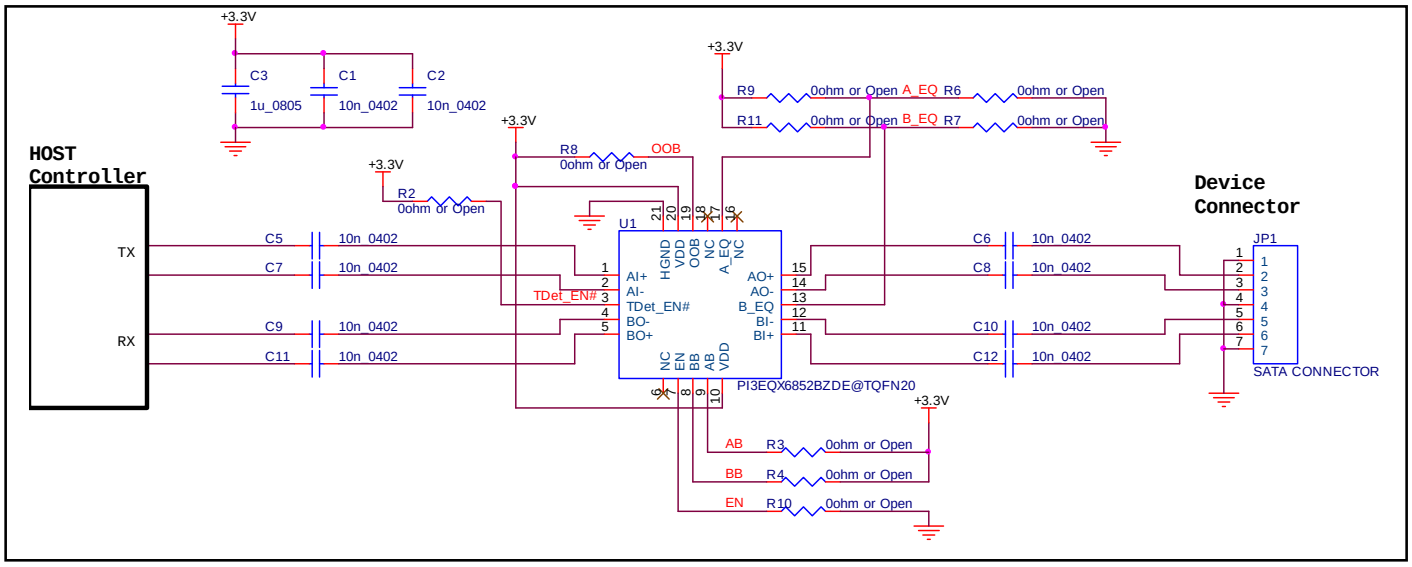
SW Setting	Eye Diagram at 3.0Gbps	Eye Diagram at 6.0Gbps
AB or BB =low		
AB or BB =High		

Table 5: Eye Diagram vs. Swing Setting at 3.0G/s and 6Gb/s

Typical application circuit

Figure 6 shows typical application circuit of PI3EQX6852BZDE.



RESISTOR CONFIGURATION

PIN NAME	PIN FUNCTION DESCRIPTION	RESISTOR CONFIGURATION
EN	With Internal 200k-ohm pull-up resistor Low: Power down mode High: Normal Operation	R10=Open, Normal Operation R10=0ohm, Power down Mode
A_EQ B_EQ	Tri-level input with internal pull-up resistor and pull-down resistor	Equalization is controled by R9&R6 for Channel A, R11&R7 for Channel B. Resistor: Ch A: R6=0ohm,R9=Open / Ch B: R7=0ohm,R11=Open → Input Equalization for Channel A&B 6Gb/s: 8.0dB Ch A: R6=Open,R9=Open / Ch B: R7=Open,R11=Open → 4.0dB Ch A: R6=Open,R9=0ohm / Ch B: R7=Open,R11=0ohm → 16.0dB
AB BB	Output Swing Adjustment it is digital control with internal 200kohm pull-down resistor	Output Swing is controlled by R3 for Channel A, R4 for Channel B. R3&R4: Open → Emphasis/Swing for Channel A&B 6Gb/s: 600mVpp R3&R4: 0ohm → 1200mVpp
TDet_EN#	With Internal 200k-ohm pull-down resistor Low: Enable termination detect function High: Disable termination detect function	R2=Open, Enable termination detect function R2=0ohm, Disable termination detect function
OOB	Signal Detect Threhold Selection it is digital control with internal 200kohm pull-down resistor	Signal Threhold is controlled by R8. R8: Open → Signal Detect Threhold Selection: 120mVppd R8: 0ohm → 200mVppd

Figure 6: Typical Application Circuit of PI3EQX6852BZDE

PCB Layout Sample

Figure 7 shows typical layout routing of PI3EQX6852BZDE.

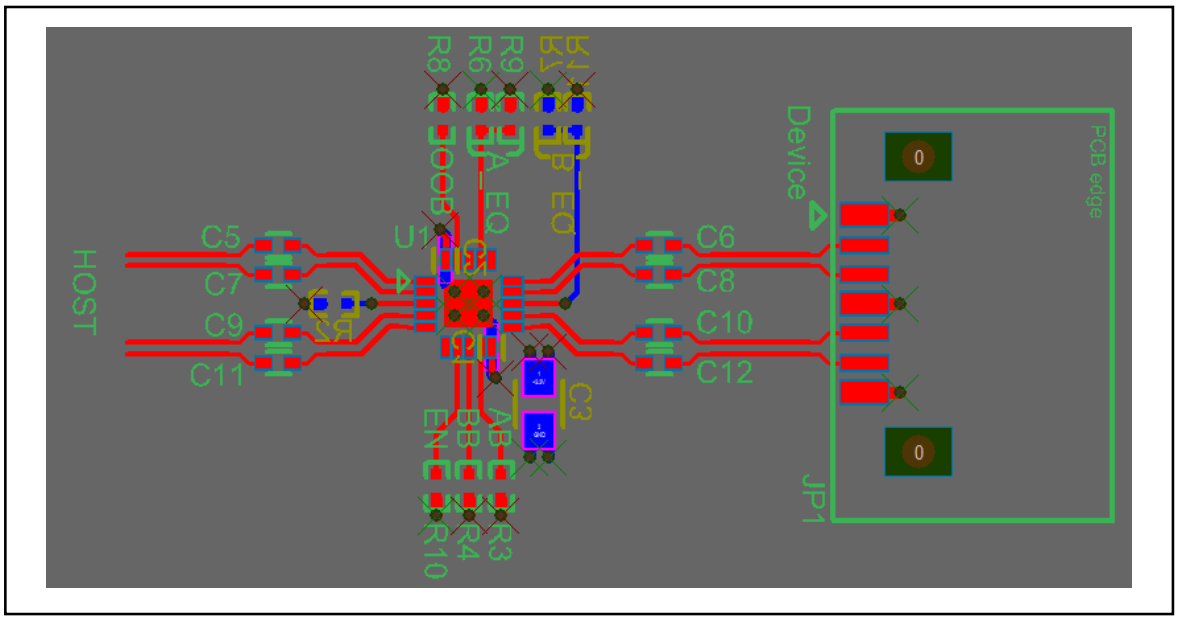


Figure 7: Typical Layout Routing of PI3EQX6852BZDE

History

Version 1.0	Original Version	Nov. 2, 2011