PI3EQX7701 SuperSpeed USB Source Application

by Noyes Mok

Introduction

SuperSpeed USB (USB 3.0) delivering data rates up to 5Gbps which is ten times faster than Hi-Speed USB (USB 2.0) with optimized power efficiency. At these high transmission rates, signal integrity issues become increasingly restrictive on PCB trace and cable lengths, and on design implementation and features. Poor signal quality can significantly impact system performance and reliability.
Pericom's PI3EQX7701 is a low power, high performance 5.0Gbps signal ReDriver™ designed specifically for the USB 3.0 protocol. It provides programmable equalization, de-emphasis and the input threshold controls to optimize performance over a variety of physical mediums by reducing Inter-symbol interference (ISI). PI3EQX7701 also have the automatic receiver detection and auto power down feature that selectively puts the device into a low power state on a channel by channel basis. Schematic and layout guidelines are provided in this application note.

- **SuperSpeed ReDriver in Source Application**
- **PI3EQX7701 control pin setting**
- **SuperSpeed USB Layout Guideline**

SuperSpeed (USB 3.0) ReDriver in Source Application

PI3EQX7701 is a dual channel (TX± and RX±), single lane USB3.0 redriver which use in source application such as Notebooks, Desktops, Docking Station, Backplane and Cabling. Each channel offers selectable equalization setting to compensate the different input trace loss. The block diagram below shows the application on notebook with docking.

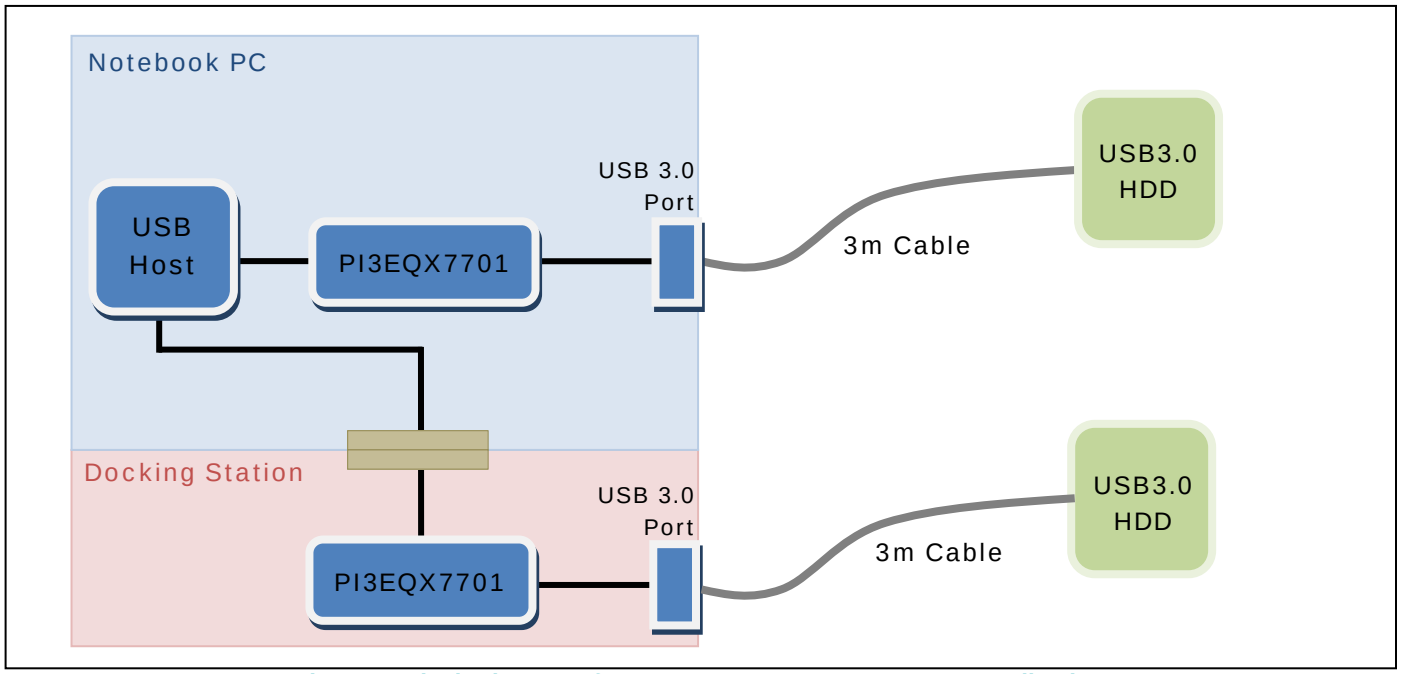


Figure 1: Block Diagram of PI3EQX7701 on USB 3.0 Source Application

Reference Design for Source Application

Below is a reference design of PI3EQX7701 in source application.

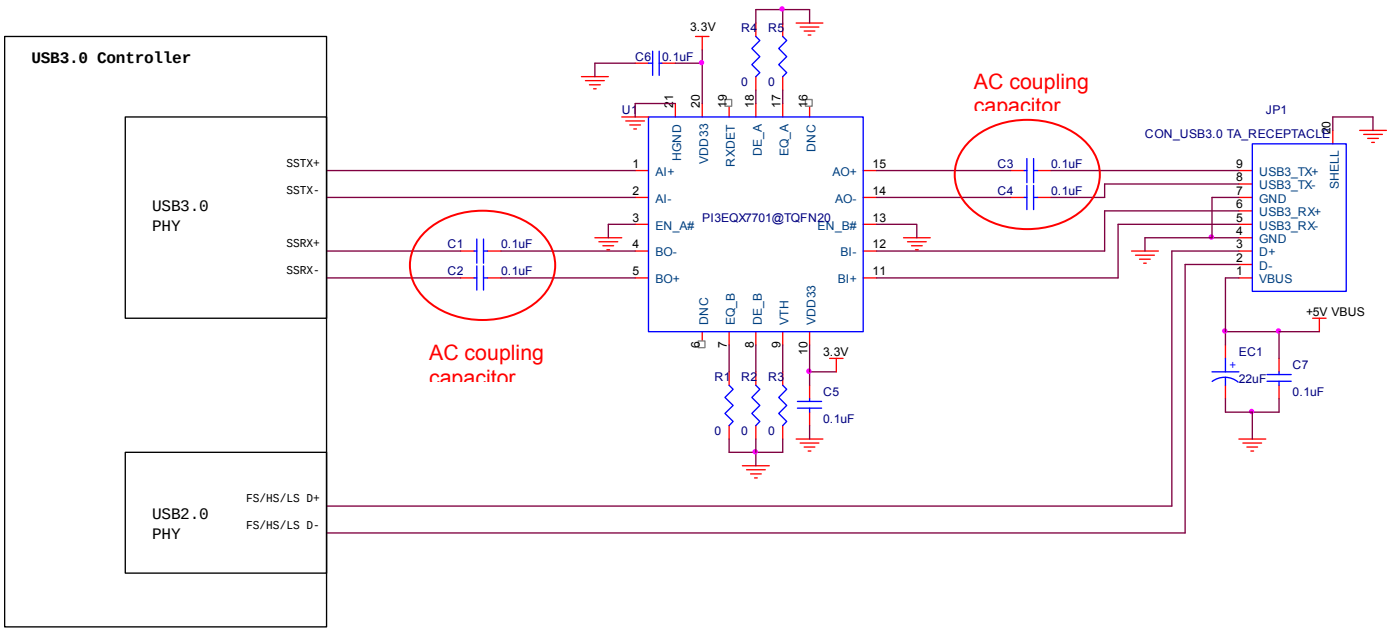


Figure 2: Reference Schematic of PI3EQX7701 USB3.0 Host Application

According to Universal Serial Bus 3.0 Specification, all transmitters shall be AC coupled. The AC coupling capacitor value should be within 75nF and 200nF.

PI3EQX7701 control pin setting

A. RxDet and EN_x# setting

RxDet pin (pin 19) is used to enable the programmable receiver detect function. When RxDet pin is set to high and either channels signal detector is idle for longer than 330ms, the automatic receiver detection will be active and the device will move to power down mode due to inactivity.

EN_A# (pin 3) and EN_B# (pin 13) is used to enable channel A/B of PI3EQX7701. When EN_A/B# is set to low, channel A/B is in normal operation.
As

EN_A/B#	RxDet	Function	Input R	Output R
1	X	Channel Disable if both EN_A/B# are high, Chip Power Down	Hi-Z	Hi-Z
0	0	Chip and channel A/B enabled, receiver detect is not active	50Ω	50Ω
0	1	Chip and channel A/B enabled, receiver detect is active	50Ω / Hi-Z	50Ω / Hi-Z

Table 1: EN_A/B and RxDet truth table of PI3EQX7701

As 100kΩ internal pull-down resistors are implemented in EN pins of PI3EQX7701, leave the pins floating to enable the channel. The RxDet pin with 100kΩ internal pull up resistor, only external pull-down resistor is required to adjust the receiver detection setting.

B. VTH Setting

VTH pin (pin 9) is used to set the threshold voltage of the signal detector for both channel A and channel B. If the input signal level of the channel falls below the active threshold level, the outputs are driven to the common mode voltage.
The threshold setting of the signal detector is based on the level of input signal (the income signal). The default setting on VTH = 100mV which is according to the Receiver Normative Electrical Parameters in Universal Serial Bus 3.0 specification (Revision 1.0).
VTH = 70mV is used when the income signal is not good enough and the signal level is between 70mV and 100mV. However, this will also increase the chance on the noise detection.

Recommended threshold setting of signal detector	VTH
70mV	0
100mV (default)	1

Table 2: VTH Threshold of signal detector truth table of PI3EQX7701

As 100kΩ internal pull-up resistor is implemented in VTH pins of PI3EQX7701, only external pull-down resistor is required to adjust the threshold setting of signal detector.

C. EQ Settings

Equalization feature offers compensation of deterministic jitter introduced by impedance mismatch. PI3EQX7701 offers 2 equalization levels on channel A and channel B for different input trace lengths which can be selected by EQ_A (pin 17) and EQ_B (pin 7) pins.

Input PCB Trace Length	Recommended EQ	EQ_A/EQ_B
4 – 12 inch FR4 (6-mil trace)	5dB	0
8 – 20 inch FR4 (6-mil trace)	11dB	1

Table 3: EQ setting of channel A and B

As 100kΩ internal pull-up resistors are implemented in EQ pins of PI3EQX7701, only external pull-down resistors are required to adjust the equalization setting.

Remark: It's suggested to disable the de-emphasis function at the USB3.0 host output if redriver is used. De-emphasis setting will decrease the swing level which may introduce the jitter and noise to the redriver input.

D. DE_x Settings

Selectable de-emphasis is provided to compensate the distortion on USB3.0 signal at differential outputs. The de-emphasis level will depend on the cable length and can be selected by DE_A (pin 18) and DE_B (pin 6) pins.

Output PCB Trace Length (before the USB connector)	Recommended DE	DE_A/DE_B
1 – 2 inch FR4 (6-mil trace)	0dB	0
3 – 4 inch FR4 (6-mil trace)	-3.5dB	1

Table 4: DE setting of channel A and B

As 100kΩ internal pull-up resistors are implemented in DE pins of PI3EQX7701, only external pull-down resistors are required to adjust the de-emphasis setting.

SuperSpeed USB Layout Guideline

A. Decoupling capacitor of VDD

It is recommended to put 0.1uF decoupling capacitor at each VDD pin of Pericom IC. Below is a layout reference of decoupling capacitor placement on a PI3EQX7701 demo board. Four decoupling capacitors circled in pink below are located next to the four VDD pins (pins 6, 10, 16 and 20) of PI3EQX7701.

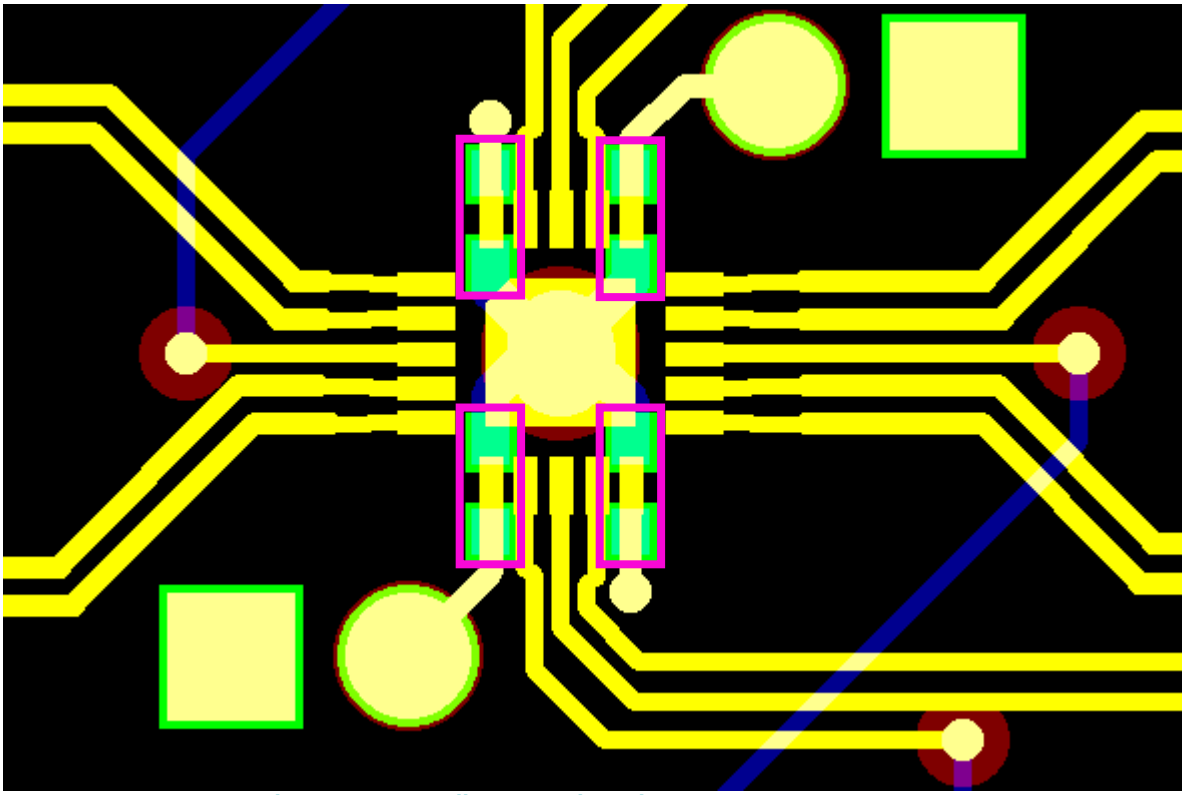


Figure 3: Decoupling Capacitor Placement on PI3EQX7701

B. PCB layers

Recommend to use at least four layers PCB for SuperSpeed USB design. Every data signal trace should be routed entirely over the ground plane on an adjacent layer.

Recommendation on 4-layer PCB setting:

Layer	Setting 1	Setting 2
Top	Data signal, Clock	Power, Control Signal
2nd	GND	Power, GND
3rd	Power, GND	GND
Bottom	Power, Control signal	Data signal, Clock

C. Routing around the USB connector

On the host design, USB receptacle connector is used on the PCB. For the Vbus trace, it's suggested to insert a ferrite bead. For the shielding of USB connector (shielding of USB cables), AC isolation to the ground (such as proper value of inductor, instead of connecting the cable shield directly to the PCB ground plane).

For the SuperSpeed signal trace, the impedance should be maintained. Avoiding any stubs and removing any routing that cause signal discontinuity and severe EMC noise issue. Also, do not put any metal between all SuperSpeed signal pair pins on every layer when using receptacles with pins stabbing the PCB.

Crosstalk between the signal trace

There are 3 pairs of signal (SSTX± /SSRX±/ D±) for USB3.0 and these signal pairs will cause three typical type near-end crosstalk:

i. SSTX± to D± in RX mode
ii. SSTX± to SSRX±
iii. D± to SSRX± in TX mode

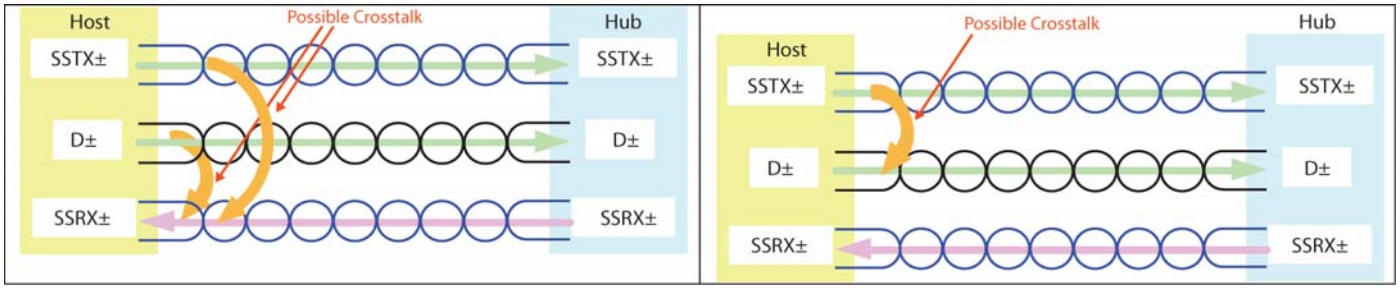
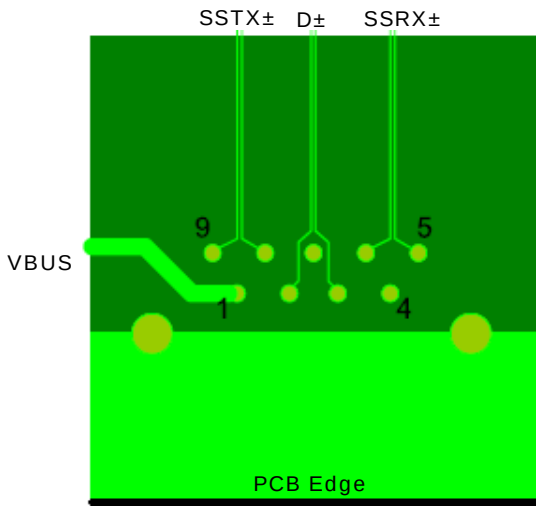


Figure 11: Crosstalk between SS and HS signal trace

In order to minimize the crosstalk issue, the routing of the signal trace between SSTX±/ SSRX± and D± pairs should not be closed to each other.

For Standard-A receptacles:

Example 1:



Example 2:

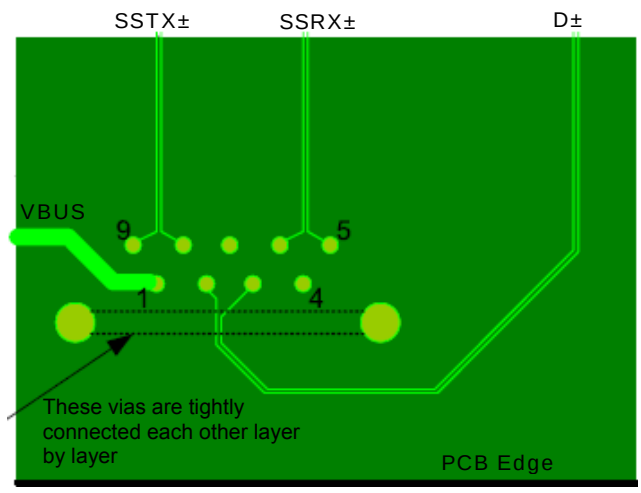


Figure 12: Example of routing on Standard-A receptacle connector

For Standard-B receptacles:

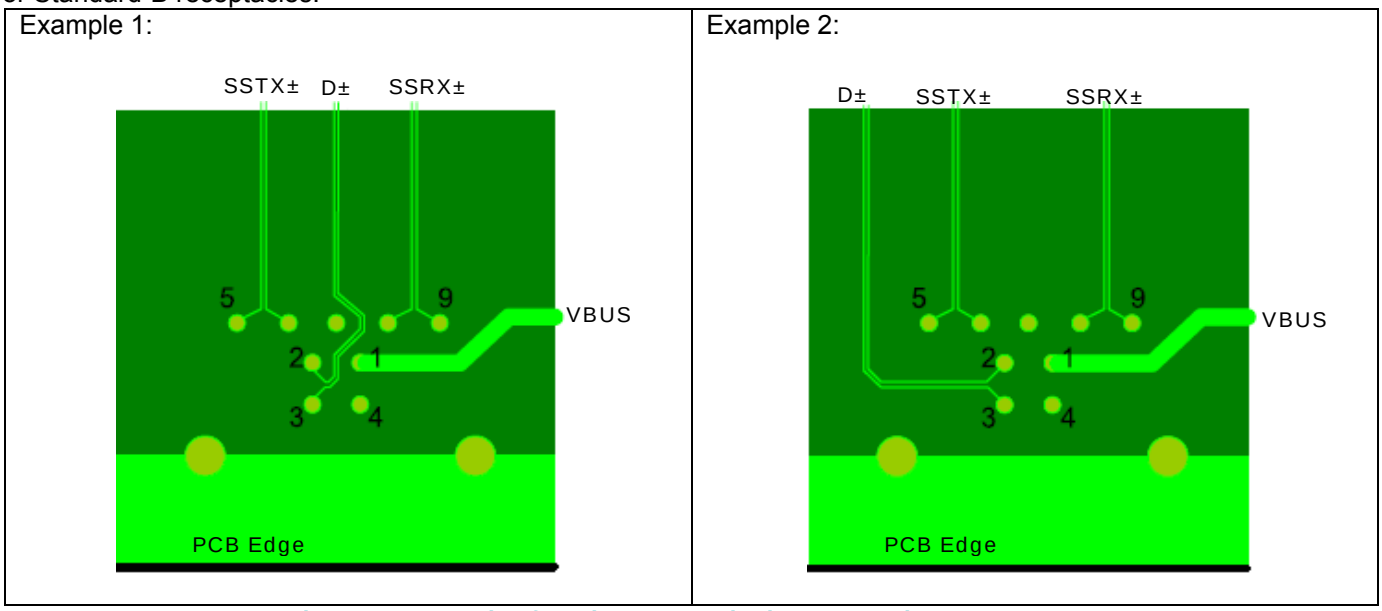


Figure 13: Example of routing on Standard-B receptacle connector

For Standard-A double-stack receptacles:

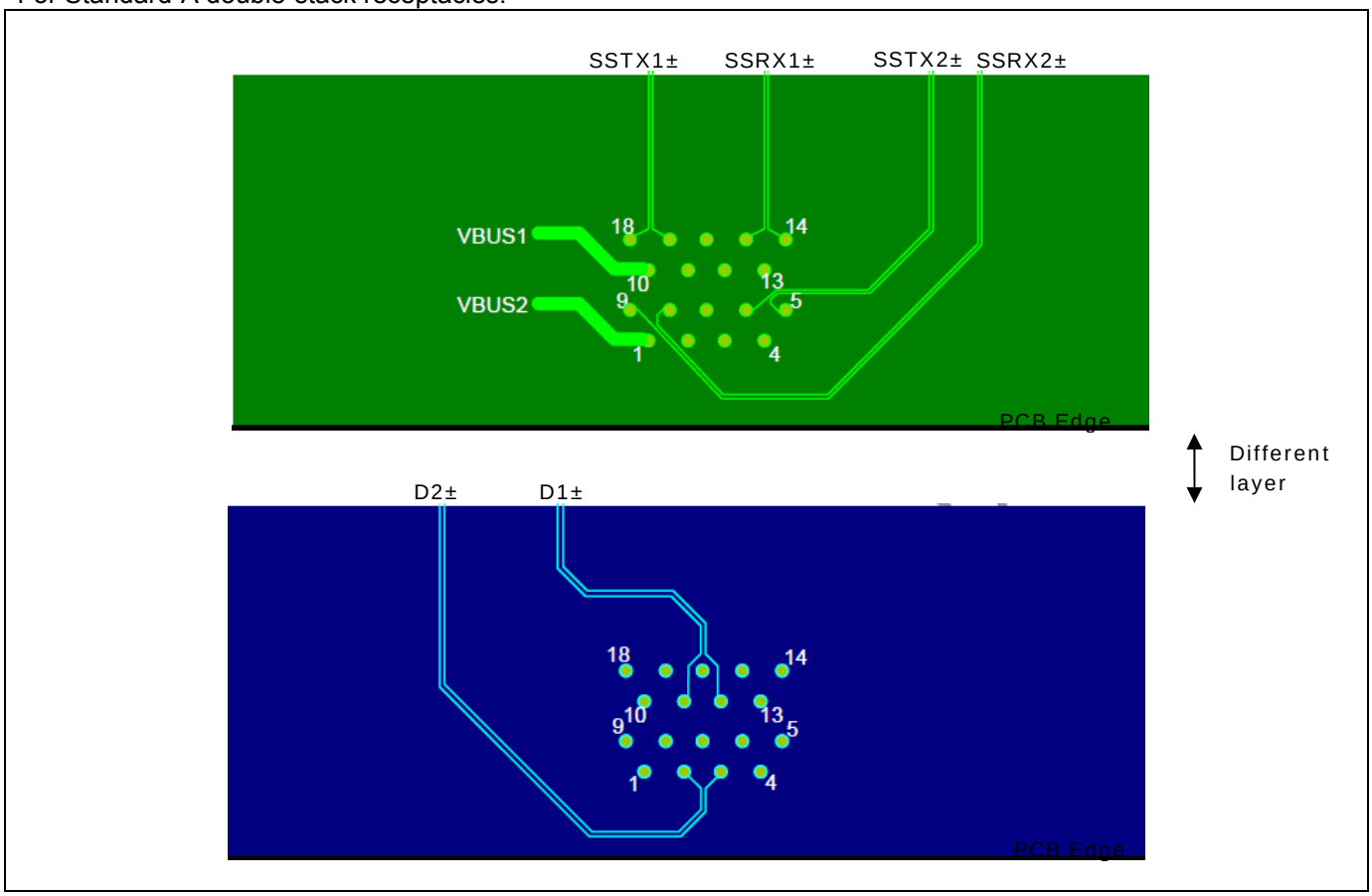


Figure 14: Example of routing on Standard-A double-stack connector

SuperSpeed signal trace impedance

The layout around USB3.0 receptacle connector was routed as one or more large metal planes in specific layer (such as GND layer). In order to maintain the differential impedance of any SuperSpeed signal trace, make sure there is no metal between pins for any differential pair.

For Standard-A receptacles:

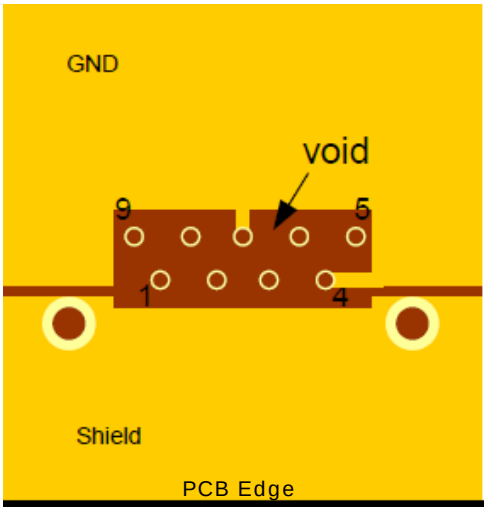
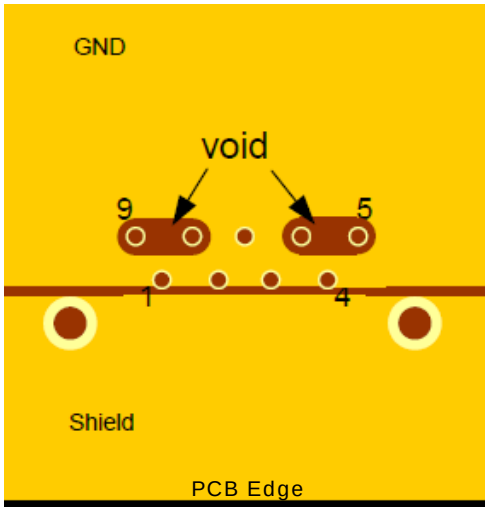
Example 1: Void at whole area around pins	Example 2: Void around SuperSpeed related pins
	

Figure 15: Example of the ground routing at GND layer with Standard-A receptacle connector

For Standard-B receptacles:

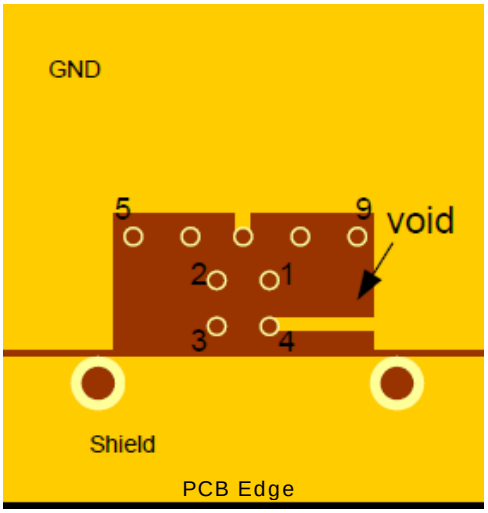
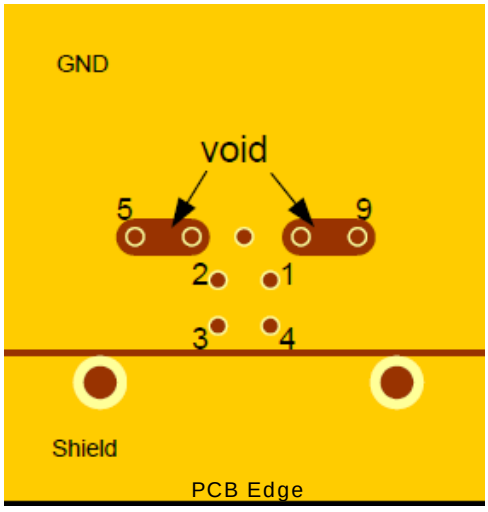
Example 1: Void at whole area around pins	Example 2: Void around SuperSpeed related pins
	

Figure 16: Example of the ground routing at GND layer with Standard-B receptacle connector

Stub on SuperSpeed trace

The pin on USB3.0 receptacle connector become an open stub if the SS signal trace pair is designed on the top layer which will cause the signal discontinuity issue.

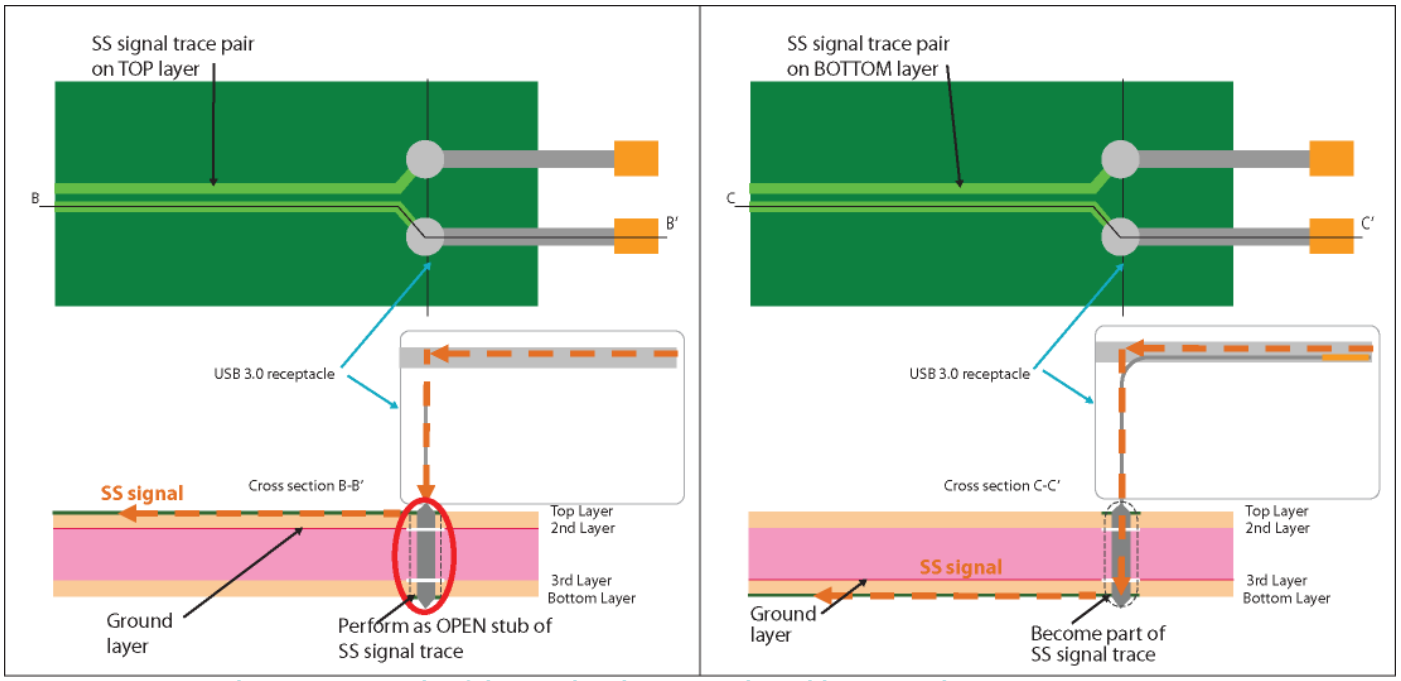


Figure 17: Example of the SS signal trace routing with receptacle connector

D. Routing around the USB Controller

As high speed signal is sensitive to power signal, therefore the routing on power and ground design of USB controller need to be careful. Same as section (A), the decoupling cap is need for each power pin and it should be place as close as the power pad of USB controller. As USB controller contains both analog and digital section, analog power and digital power is required. In order to avoid the interference from the digital signal cause the malfunction on the analog circuit, the routing between analog power and digital signal trace should be placed as far as possible (including the signal trace). For the same voltage level's analog power and digital power, a ferrite bead should be added in between for noise filtering.

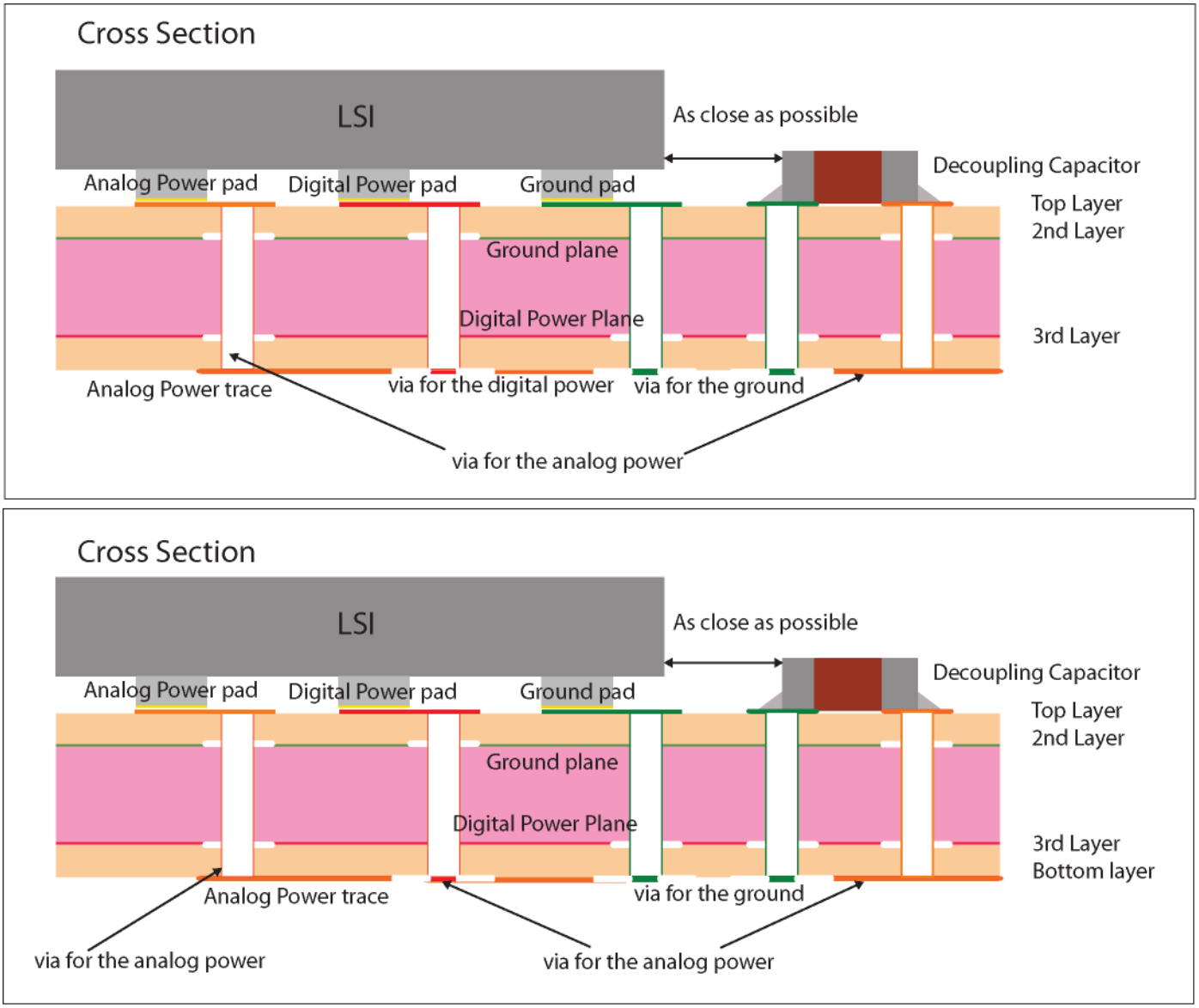


Figure 18: Placement of decoupling capacitor at USB Host controller

For the differential signal layout design, please refer to **"High Speed Signal layout guideline"**